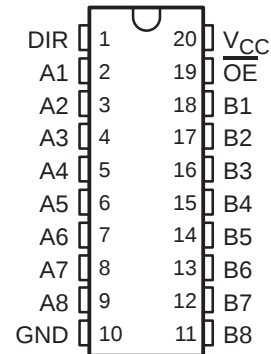


- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltages With $3.3\text{-}V_{V_{CC}}$)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors**
- **Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVCH245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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TEXAS
INSTRUMENTS

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The logic diagram shows the internal structure of the 74VHC147 decoder. It features two 3-input AND gates at the top and two 2-input inverters below them. The inputs are DIR (pin 1), A1 (pin 2), and OE (pin 19). The outputs are B1 (pin 18) and a group of outputs connected to seven other channels. The diagram illustrates the internal logic of the decoder, showing how the inputs are combined to produce the outputs.

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage data inputs		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3 state	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		-12	mA
		$V_{CC} = 3\text{ V}$		-24	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		12	mA
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	MIN	TYP [‡]	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	MIN to MAX	$V_{CC}-0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2.2			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = 5.5\text{ V or GND}$	3.6 V			± 5	μA
$I_{I(\text{hold})}$	$V_I = 0.8\text{ V}$	3 V	75			μA
	$V_I = 2\text{ V}$	3 V	-75			
	$V_I = 0\text{ to }3.6\text{ V}$	3.6 V			± 500	
$I_{OZ}^\S$	$V_O = V_{CC}\text{ or GND}$	MIN to MAX			± 10	μA
	$V_O = 3.6\text{ V or }5.5\text{ V}$				± 50	
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V			500	μA
C_i	Control inputs	$V_I = V_{CC}\text{ or GND}$	3.3 V	3.3		pF
C_{iO}	A or B ports	$V_O = V_{CC}\text{ or GND}$	3.3 V	5.4		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are measured at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74LVCH245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	7	8		ns
t_{en}	$\overline{OE}$	A or B	1.5	8.5	9.5		ns
t_{dis}	$\overline{OE}$	A or B	1.5	7.5	8.5		ns
$t_{sk(o)}^\dagger$				1			ns

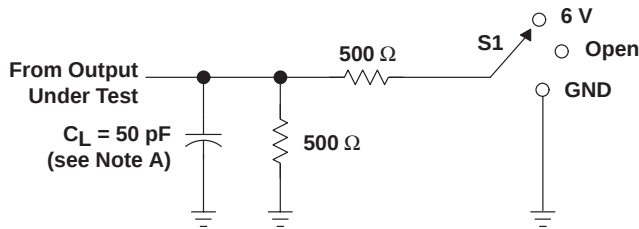
[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	36	pF
	Outputs disabled		2	

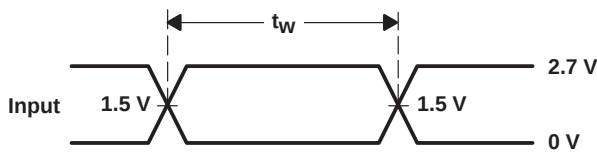


PARAMETER MEASUREMENT INFORMATION

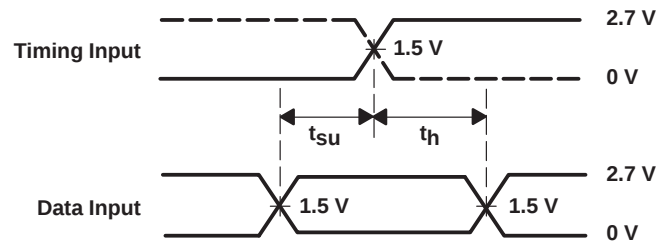


LOAD CIRCUIT FOR OUTPUTS

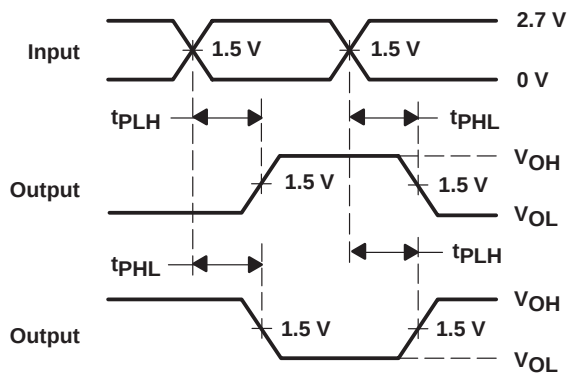
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



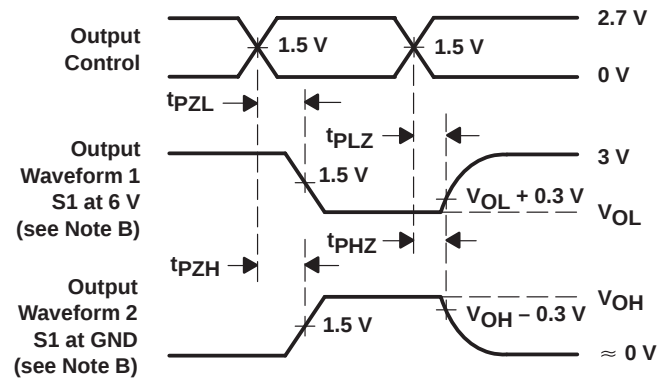
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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