



# TDF8530

I<sup>2</sup>C-bus controlled quad channel 45 W/2  $\Omega$  class-D power amplifier with full diagnostics

Rev. 3 — 20 October 2011

Product short data sheet

## 1. General description

The TDF8530 is a quad Bridge-Tied Load (BTL) car audio amplifier comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. Low power dissipation enables the TDF8530 high-efficiency, class-D amplifier to be used with a smaller heat sink than those normally used with standard class-AB amplifiers.

The TDF8530 can operate in either non-I<sup>2</sup>C-bus mode or I<sup>2</sup>C-bus mode. When in I<sup>2</sup>C-bus mode, DC load detection results and fault conditions can be easily read back from the device. Up to 12 I<sup>2</sup>C-bus addresses can be selected depending on the value of the external resistors connected to pins ADS and MOD.

When pin ADS is short circuited to ground, the TDF8530 operates in non-I<sup>2</sup>C-bus mode. Switching between Operating mode and Mute mode in non-I<sup>2</sup>C-bus mode is only possible using pins EN and SEL\_MUTE.

## 2. Features and benefits

- High-efficiency
- Low quiescent current
- Operating voltage from 6 V to 24 V
- 4  $\Omega$  or 2  $\Omega$  capable BTL channels
- Fast-mode I<sup>2</sup>C-bus
- I<sup>2</sup>C-bus mode with 12 I<sup>2</sup>C-bus addresses or non-I<sup>2</sup>C-bus mode operation
- Clip detect selectable at 0.2 % or 10 % THD
- Independent short-circuit protection for each channel
- Advanced short-circuit protection for load, GND and supply
- Load dump protection to 50 V
- Thermal foldback and thermal protection
- DC offset protection
- Selectable AD or BD modulation
- Advanced clocking:
  - ◆ Switchable oscillator clock source: internal for Master mode or external for Slave mode
  - ◆ Spread spectrum mode
  - ◆ Phase staggering
  - ◆ Frequency hopping
- No 'pop noise' caused by DC output offset voltage
- I<sup>2</sup>C-bus mode:



- ◆ Load diagnostics
  - Speaker load, open load and shorted load
  - Amplifier output to ground and to supply shorts
  - Tweeter detection
- ◆ Thermal pre-warning diagnostic level setting
- ◆ Identification of activated protections or warnings
- ◆ Selectable diagnostic information available using DIAG pin
- Qualified in accordance with AEC-Q100

### 3. Applications

- Car audio
- Audio entertainment systems

### 4. Quick reference data

Table 1. Quick reference data

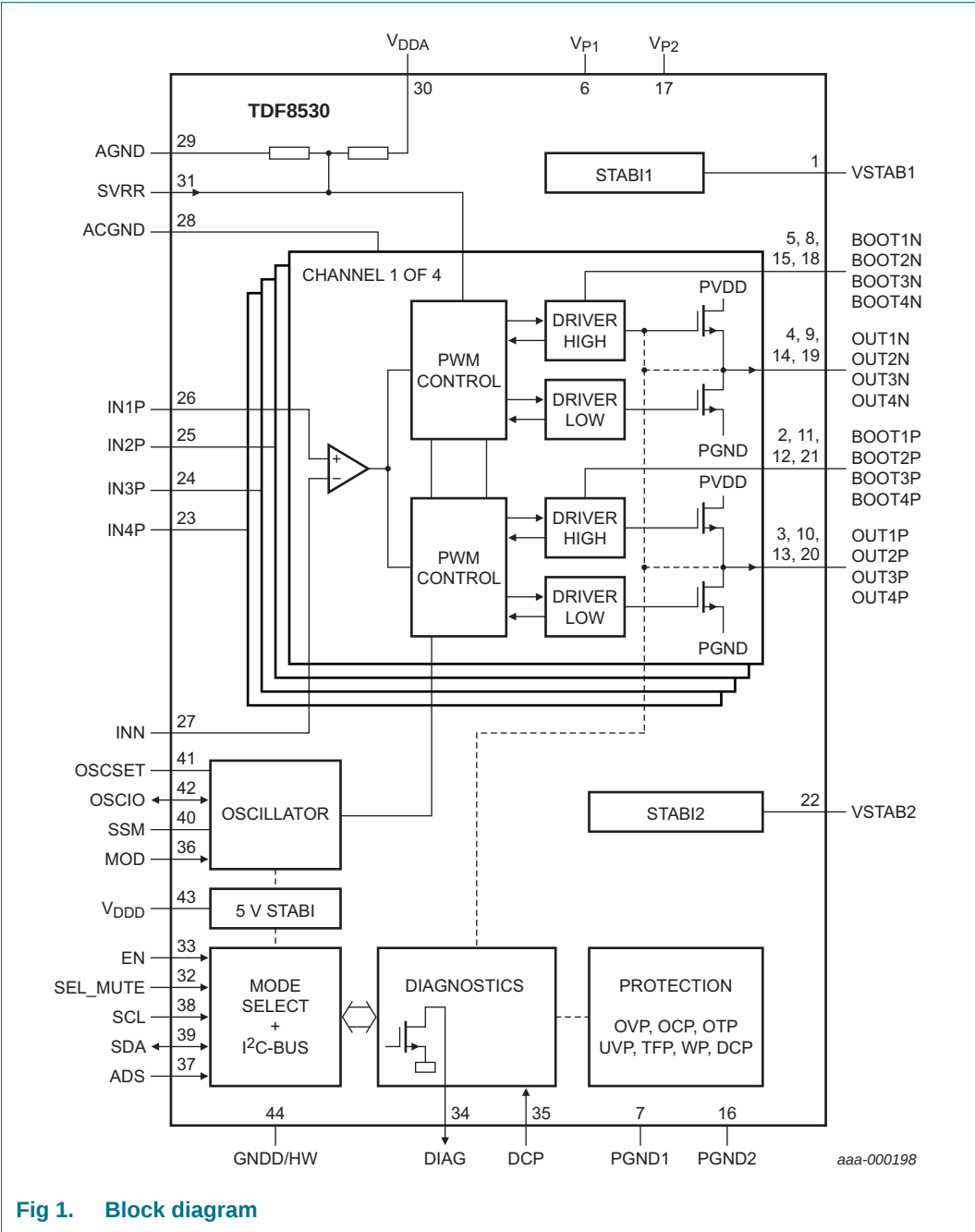
| Symbol                                    | Parameter         | Conditions                                    | Min | Typ  | Max | Unit |
|-------------------------------------------|-------------------|-----------------------------------------------|-----|------|-----|------|
| General; V <sub>P</sub> = 14.4 V          |                   |                                               |     |      |     |      |
| V <sub>P</sub>                            | supply voltage    |                                               | 6   | 14.4 | 24  | V    |
| I <sub>P</sub>                            | supply current    | off state; V <sub>EN</sub> < 0.8 V            | -   | 2    | 10  | μA   |
| I <sub>q</sub>                            | quiescent current | no load, snubbers and output filter connected | -   | 185  | 200 | mA   |
| Quad BTL channel; V <sub>P</sub> = 14.4 V |                   |                                               |     |      |     |      |
| P <sub>o</sub>                            | output power      | R <sub>L</sub> = 4 Ω; THD = 10 %              | 24  | 26   | -   | W    |
|                                           |                   | R <sub>L</sub> = 2 Ω; THD = 10 %              | 39  | 45   | -   | W    |
| Quad BTL channel; V <sub>P</sub> = 24 V   |                   |                                               |     |      |     |      |
| P <sub>o</sub>                            | output power      | R <sub>L</sub> = 4 Ω; THD = 10 %              | -   | 70   | -   | W    |
|                                           |                   | R <sub>L</sub> = 2 Ω; THD = 10 %              | -   | 100  | -   | W    |

### 5. Ordering information

Table 2. Ordering information

| Type number | Package |                                                                         |           |
|-------------|---------|-------------------------------------------------------------------------|-----------|
|             | Name    | Description                                                             | Version   |
| TDF8530TH   | HSOP44  | plastic, heatsink small outline package; 44 leads; low stand-off height | SOT1131-1 |

6. Block diagram



## 7. Pinning information

### 7.1 Pinning

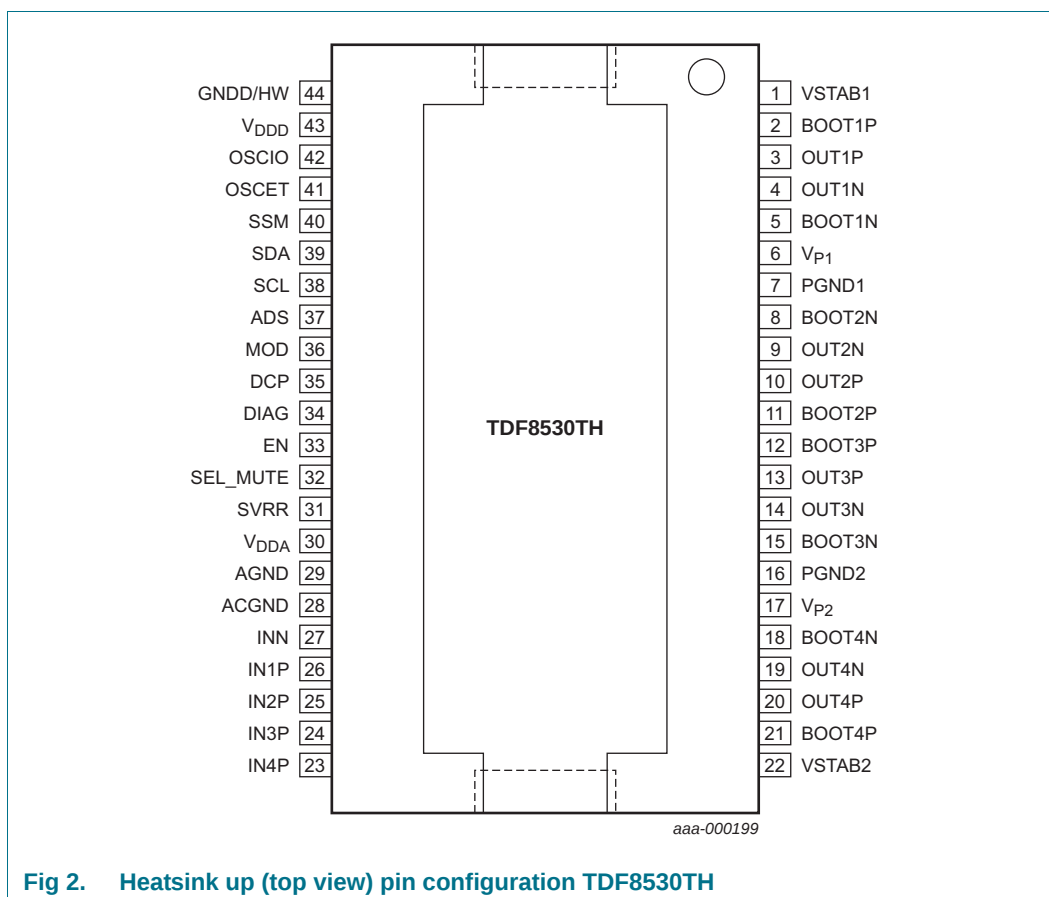


Fig 2. Heatsink up (top view) pin configuration TDF8530TH

### 7.2 Pin description

Table 3. Pin description

| Symbol          | Pin | Type <sup>[1]</sup> | Description                                        |
|-----------------|-----|---------------------|----------------------------------------------------|
| VSTAB1          | 1   |                     | decoupling internal stabilizer 1 for DMOST drivers |
| BOOT1P          | 2   |                     | bootstrap capacitor for channel 1 positive         |
| OUT1P           | 3   | O                   | channel 1 positive PWM output                      |
| OUT1N           | 4   | O                   | channel 1 negative PWM output                      |
| BOOT1N          | 5   |                     | bootstrap capacitor for channel 1 negative         |
| V <sub>P1</sub> | 6   | P                   | channel 1 power supply voltage                     |
| PGND1           | 7   | G                   | channel 1 power ground                             |
| BOOT2N          | 8   |                     | bootstrap capacitor for channel 2 negative         |
| OUT2N           | 9   | O                   | channel 2 negative PWM output                      |
| OUT2P           | 10  | O                   | channel 2 positive PWM output                      |
| BOOT2P          | 11  |                     | bootstrap capacitor for channel 2 positive         |
| BOOT3P          | 12  |                     | bootstrap capacitor for channel 3 positive         |

Table 3. Pin description ...continued

| Symbol           | Pin | Type <sup>[1]</sup> | Description                                                                                                                         |
|------------------|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| OUT3P            | 13  | O                   | channel 3 positive PWM output                                                                                                       |
| OUT3N            | 14  | O                   | channel 3 negative PWM output                                                                                                       |
| BOOT3N           | 15  |                     | bootstrap capacitor for channel 3 negative                                                                                          |
| PGND2            | 16  | G                   | channel 2 power ground                                                                                                              |
| V <sub>P2</sub>  | 17  | P                   | channel 2 power supply voltage                                                                                                      |
| BOOT4N           | 18  |                     | bootstrap capacitor for channel 4 negative                                                                                          |
| OUT4N            | 19  | O                   | channel 4 negative PWM output                                                                                                       |
| OUT4P            | 20  | O                   | channel 4 positive PWM output                                                                                                       |
| BOOT4P           | 21  |                     | bootstrap capacitor for channel 4 positive                                                                                          |
| VSTAB2           | 22  |                     | decoupling internal stabilizer 2 for DMOST drivers                                                                                  |
| IN4P             | 23  | I                   | channel 4 positive audio input                                                                                                      |
| IN3P             | 24  | I                   | channel 3 positive audio input                                                                                                      |
| IN2P             | 25  | I                   | channel 2 positive audio input                                                                                                      |
| IN1P             | 26  | I                   | channel 1 positive audio input                                                                                                      |
| INN              | 27  | I                   | common negative audio input                                                                                                         |
| ACGND            | 28  | I                   | decoupling for input reference voltage                                                                                              |
| AGND             | 29  | G                   | analog supply ground                                                                                                                |
| V <sub>DDA</sub> | 30  | P                   | analog supply voltage                                                                                                               |
| SVRR             | 31  | I                   | decoupling for internal half supply reference voltage                                                                               |
| SEL_MUTE         | 32  | I                   | select mute or unmute                                                                                                               |
| EN               | 33  | I                   | enable input:<br>non-I <sup>2</sup> C-bus mode: switch between off and Mute mode<br>I <sup>2</sup> C-bus mode: off and Standby mode |
| DIAG             | 34  | O                   | diagnostic output; open-drain                                                                                                       |
| DCP              | 35  | I                   | DC protection input for the filtered output voltages                                                                                |
| MOD              | 36  | I                   | modulation mode and phase shift select                                                                                              |
| ADS              | 37  | I                   | non-I <sup>2</sup> C-bus mode: connected to ground<br>I <sup>2</sup> C-bus mode: selection and address selection pin                |
| SCL              | 38  | I                   | I <sup>2</sup> C-bus clock input                                                                                                    |
| SDA              | 39  | I/O                 | I <sup>2</sup> C-bus data input and output                                                                                          |
| SSM              | 40  |                     | master setting: Spread spectrum mode frequency<br>slave setting: phase lock operation                                               |
| OSCSET           | 41  |                     | master/slave oscillator setting<br>master only setting: set internal oscillator frequency                                           |
| OSCIO            | 42  | I/O                 | external oscillator slave setting: input<br>internal oscillator master setting: output                                              |
| V <sub>DDD</sub> | 43  |                     | decoupling of the internal 5 V logic supply                                                                                         |
| GNDD/HW          | 44  | G                   | ground digital supply voltage and handle wafer connection                                                                           |

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] In this data sheet supply voltage V<sub>P</sub> describes V<sub>P1</sub>, V<sub>P2</sub> and V<sub>DDA</sub>.

## 8. Functional description

### 8.1 Master and slave mode selection

In a master and slave configuration, multiple TDF8530 devices are daisy-chained together in one audio application with a single device providing the clock frequency signal for all other devices. In this situation, it is recommended that the oscillators of all devices are synchronized for optimum EMI behavior as follows:

All OSCIO pins are connected together and one TDF8530 in the application is configured as the clock-master. All other TDF8530 devices are configured as clock-slaves.

- The clock-master pin OSCIO is configured as the oscillator output. When a resistor ( $R_{osc}$ ) is connected between pins OSCSET and AGND, the TDF8530 is in Master mode.
- The clock-slave pins OSCIO are configured as the oscillator inputs. When pin OSCSET is directly connected to pin AGND, the TDF8530 is in Slave mode.

See [Table 4](#) for all oscillator modes. IB3[D2] = 0 in non-I<sup>2</sup>C-bus mode.

**Table 4. Oscillator modes**

| OSCSET pin                    | OSCIO pin | SSM pin                         | IB3[D2] | Oscillator modes                                                           |
|-------------------------------|-----------|---------------------------------|---------|----------------------------------------------------------------------------|
| $R_{osc} > 22\text{ k}\Omega$ | output    | $C_{SSM}$ to pin AGND           | 0       | master, spread spectrum <sup>[1]</sup>                                     |
|                               |           |                                 | 1       | master, spread spectrum <sup>[2]</sup>                                     |
|                               |           | shorted to pin AGND             | 0       | master, no spread spectrum <sup>[1]</sup>                                  |
|                               |           |                                 | 1       | master, no spread spectrum <sup>[2]</sup>                                  |
| $R_{osc} = 0\ \Omega$         | input     | $C_{PLL} + R_{PLL}$ to pin AGND | 0       | slave, PLL enabled <sup>[1]</sup>                                          |
|                               |           |                                 | 1       | slave, PLL enabled <sup>[2]</sup>                                          |
|                               |           | shorted to pin AGND             | 0       | slave, PLL disabled <sup>[1]</sup><br>no $\frac{1}{2}\pi$ phase staggering |
|                               |           |                                 | 1       | slave, PLL disabled <sup>[2]</sup>                                         |

[1]  $f_{OSCIO} = f_{osc}$ .

[2]  $f_{OSCIO} = 2 \times f_{osc}$ .

### 8.2 Operation mode selection

Pin MOD is used to select specific operating modes. The resistor ( $R_{MOD}$ ) connected between pins MOD and AGND together with the non-I<sup>2</sup>C-bus/I<sup>2</sup>C-bus mode determine the operating mode (see [Table 5](#)). This in turn is determined by the resistor value connected between pins ADS and AGND.

In non-I<sup>2</sup>C-bus mode, pin MOD is used to select:

- AD or BD modulation (see [Section 8.2.1](#)).
- $\frac{2}{8}\pi$  phase shift when oscillator is used in Slave mode (see [Section 8.2.2](#)).

In I<sup>2</sup>C-bus mode, pin MOD can only select the I<sup>2</sup>C-bus address range. The modulation mode and phase shift are programmed using I<sup>2</sup>C-bus commands.

Table 5. Operation mode selection with the MOD pin

| R <sub>MOD</sub> (kΩ) | Non-I <sup>2</sup> C-bus mode <sup>[1]</sup>               |
|-----------------------|------------------------------------------------------------|
| 0 (short to AGND)     | AD modulation: no phase shift in Slave mode                |
| 6.8                   | BD modulation: no phase shift in Slave mode                |
| 33                    | AD modulation: $\frac{2}{8} \pi$ phase shift in Slave mode |
| 100                   | BD modulation: $\frac{2}{8} \pi$ phase shift in Slave mode |

[1] R<sub>ADS</sub> = 0 Ω; pin ADS is short circuited to pin AGND.

### 8.2.1 Modulation mode

In non-I<sup>2</sup>C-bus mode, pin MOD is used to select either AD or BD modulation mode (see [Table 5](#)). In I<sup>2</sup>C-bus mode, the modulation mode is selected using I<sup>2</sup>C-bus command IB3[D0].

- AD modulation mode: the bridge halves switch in opposite phase.
- BD modulation mode: the bridge halves switch in phase.

[Figure 4](#) and [Figure 5](#) show simplified representations of AD and BD modulation.

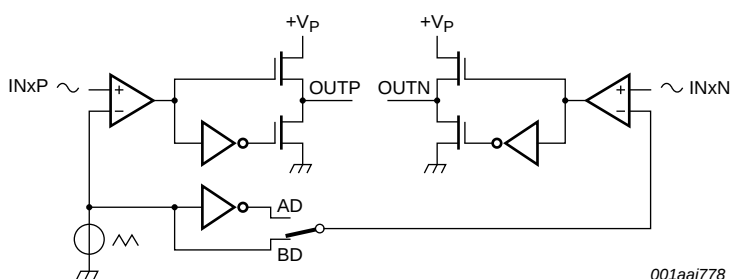
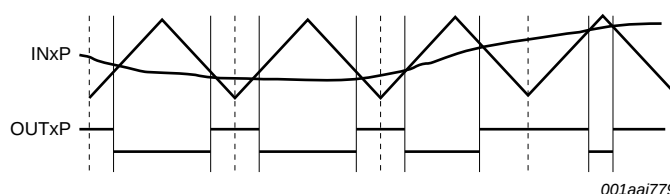
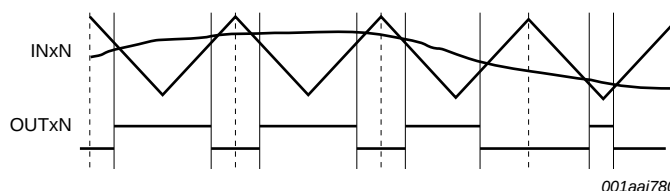


Fig 3. AD/BD modulation switching circuit

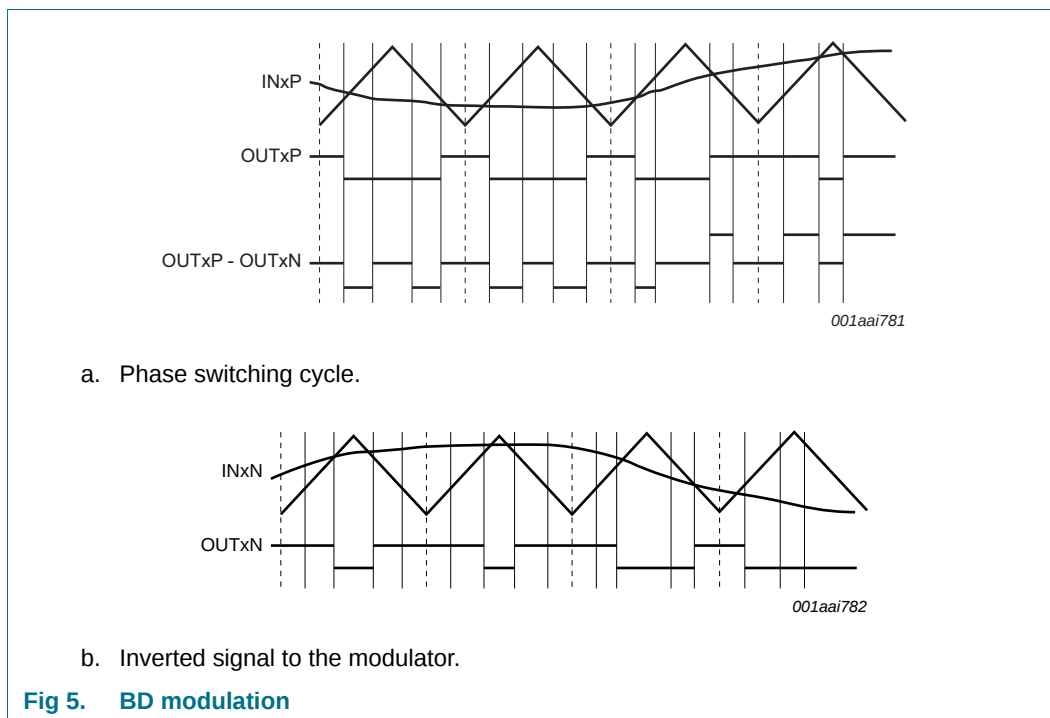


a. Bridge half 1.



b. Bridge half 2 switched in the opposite phase to bridge half 1.

Fig 4. AD modulation

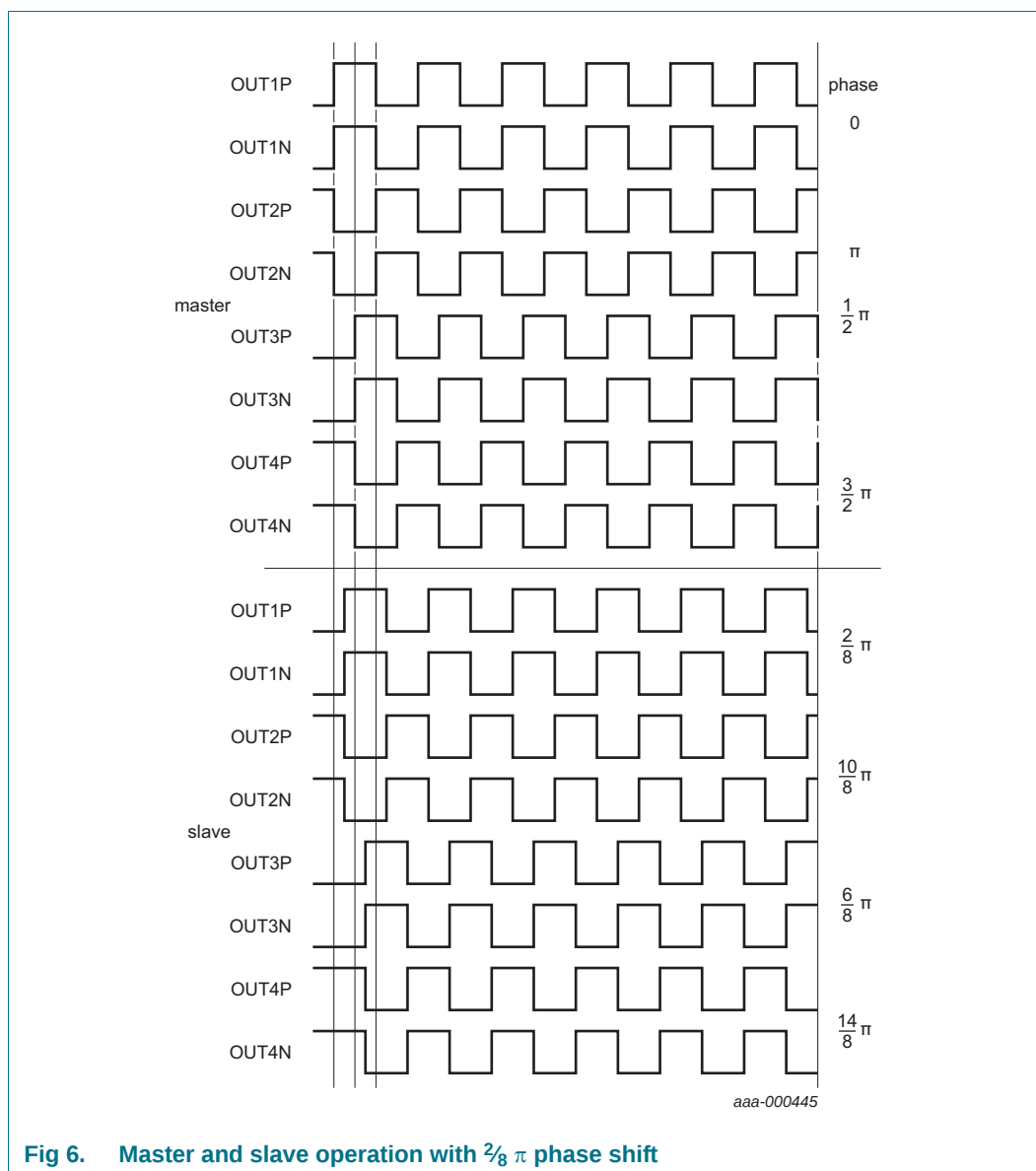


### 8.2.2 Phase staggering (Slave mode)

In Slave mode with phase lock operation enabled, a phase shift with respect to the incoming clock signal can be selected to distribute the switching moments over time in multi-amplifier applications. In non-I<sup>2</sup>C-bus mode,  $\frac{2}{8}\pi$  phase shift can be programmed using pin MOD. In I<sup>2</sup>C-bus mode, three different phase shifts ( $\frac{1}{8}\pi$ ,  $\frac{2}{8}\pi$ ,  $\frac{3}{8}\pi$ ) can be selected using the I<sup>2</sup>C-bus bits (IB4[D2:D3]). See [Table 5](#) for selection of the phase shift in non-I<sup>2</sup>C-bus mode with pin MOD.

By default there is a  $\frac{1}{2}\pi$  phase staggering between channels 1 and 2 and channels 3 and 4 of the TDF8530 independent of Master or Slave mode. This  $\frac{1}{2}\pi$  phase staggering can be disabled using the I<sup>2</sup>C-bus bit IB4[D4] resulting in all channels switching at the same time.

[Figure 6](#) shows an example of the use of  $\frac{2}{8}\pi$  phase shift with BD modulation.



**Fig 6. Master and slave operation with  $\frac{2}{8}\pi$  phase shift**

### 8.3 Protection

The TDF8530 includes a range of built-in protection functions. All protections are asynchronous and do not need an (external) clock signal at pin OSCIO to be operational. How the TDF8530 manages the various possible fault conditions for each protection is described in the following sections:

**Table 6. Overview of protection types**

| Protection type  | Reference                     |
|------------------|-------------------------------|
| Thermal foldback | <a href="#">Section 8.3.1</a> |
| Overtemperature  | <a href="#">Section 8.3.2</a> |
| Overcurrent      | <a href="#">Section 8.3.3</a> |
| Window           | <a href="#">Section 8.3.4</a> |

Table 6. Overview of protection types ...continued

| Protection type | Reference                     |
|-----------------|-------------------------------|
| DC Offset       | <a href="#">Section 8.3.5</a> |
| Undervoltage    | <a href="#">Section 8.3.6</a> |
| Overvoltage     | <a href="#">Section 8.3.6</a> |

### 8.3.1 Thermal foldback

The TDF8530 has a built-in Thermal Foldback Protection (TFP) which is tripped when the average junction temperature exceeds the threshold level. TFP decreases amplifier gain such that the combination of power dissipation and  $R_{th(j-a)}$  create a junction temperature around the threshold level. The device will not completely switch off but remains operational at the lower output power levels. If the average junction temperature continues to increase, a second built-in temperature protection threshold level shuts down the amplifier completely.

### 8.3.2 Overtemperature protection

If the average junction temperature ( $T_j$ ) > 160 °C, OverTemperature Protection (OTP) is tripped and the power stages shut down immediately.

### 8.3.3 Overcurrent protection

OverCurrent Protection (OCP) is tripped when the output current exceeds the threshold. OCP regulates the output voltage such that the maximum output current is limited. The amplifier outputs keep switching and the amplifier is NOT shutdown completely. This is called current limiting.

OCP also detects when the loudspeaker terminals are short circuited or one of the amplifier's demodulated outputs is short circuited to one of the supply lines. In either case, the shorted channel(s) are switched off.

The amplifier can distinguish between loudspeaker impedance drops and a low-ohmic short across the load or one of the supply lines. This impedance threshold depends on the supply voltage used. When a short is made across the load causing the impedance to drop below the threshold level, the shorted channel(s) are switched off. They try to restart every 50 ms. If the short circuit condition is still present after 50 ms, the cycle repeats. The average power dissipation will be low because of this reduced duty cycle.

When a channel is switched off due to a short circuit on one of the supply lines, Window Protection (WP) is activated. WP ensures that the amplifier does not start up after 50 ms until the supply line short circuit is removed.

### 8.3.4 Window protection

Window Protection (WP) checks the PWM output voltage before switching from Standby mode to Mute mode (with both outputs switching) and is activated as follows:

- During the start-up sequence:
  - When the TDF8530 is switched from standby to mute ( $t_{d(stb-mute)}$ ). When a short circuit on one of the output terminals (to  $V_P$  or GND) is detected, the start-up procedure for that channel is interrupted and the TDF8530 waits for open circuit outputs. No large currents flow in the event of a short circuit to the supply lines because the check is performed before the power stages are enabled.

- During operation:
  - A short circuit to one of the supply lines trips OCP causing the amplifier channel to shut down. After 50 ms the amplifier channel restarts and WP is activated. However, the corresponding amplifier channel will not start up until the supply line short circuit has been removed.

### 8.3.5 DC offset protection

DC Protection (DCP) is activated (using IB1[D6] or IB2[D6]) when the DC content in the demodulated output voltage exceeds a set threshold (typically 2 V). DCP is active in both Mute mode and Operating mode. False triggering of the DCP by low frequencies in the audio signal is prevented by use of an external capacitor between pin DCP and pin AGND to generate a cut-off frequency. Connecting pin DCP to pin AGND disables DCP in both I<sup>2</sup>C-bus and non-I<sup>2</sup>C-bus modes. The DCP is always disabled when the supply voltage on pin V<sub>DDA</sub> drops below 8 V.

### 8.3.6 Supply voltage protection

UnderVoltage Protection (UVP) is activated when the supply voltage drops below the UVP threshold. UVP triggers the UVP circuit causing the system to first mute and then stop switching. The SVRR and SEL\_MUTE pin capacitors will discharge. The information on the MOD and ADS pins is latched while UVP is active. When the supply voltage rises above the UVP threshold level, the system restarts. The UVP threshold is set at 6 V minimum supply by default but can be changed to 8 V minimum supply using bit IB4[D7].

OverVoltage Protection (OVP) is activated when the supply voltage exceeds the OVP threshold. The OVP (or load dump) circuit is activated and the power stages are shut down. The SVRR and SEL\_MUTE pin capacitors will discharge. When the supply voltage drops below the OVP threshold level the system restarts.

## 8.4 Diagnostic output

### 8.4.1 Diagnostic table

The diagnostic information for I<sup>2</sup>C-bus mode and non-I<sup>2</sup>C-bus mode is shown in [Table 7](#). The instruction bitmap and data bytes are described in [Table 9](#) and [Table 11](#).

Pin DIAG has an open-drain output which must have an external pull-up resistor connected to an external voltage. Pin DIAG can show both fixed and I<sup>2</sup>C-bus selectable information.

Pin DIAG goes LOW when a short-circuit to one of the amplifier outputs occurs. The microprocessor reads the failure information using the I<sup>2</sup>C-bus. The I<sup>2</sup>C-bus bits are set for a short-circuit. These bits can be reset with the I<sup>2</sup>C-bus read command.

Even after the short circuit has been removed, the microprocessor knows what was wrong after reading the I<sup>2</sup>C-bus. Old information is read when a single I<sup>2</sup>C-bus read command is used. To read the current information, two read commands must be sent, one after another.

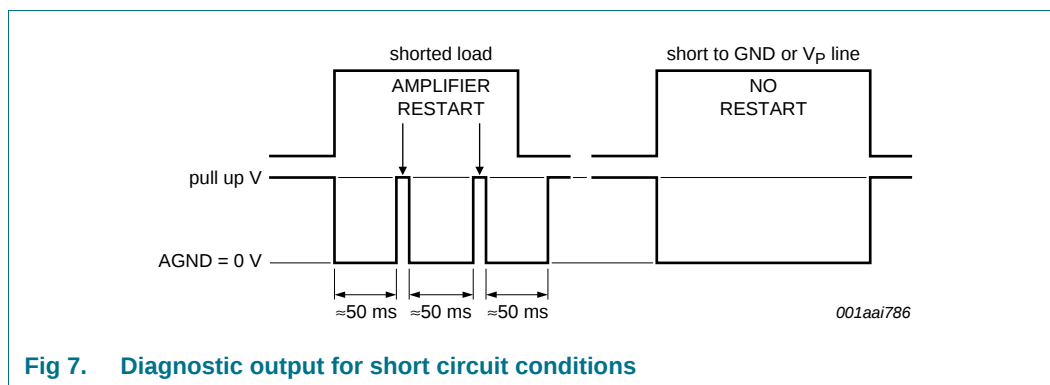
When selected, pin DIAG gives the current diagnostic information. Pin DIAG is released instantly when the failure is removed, independent of the I<sup>2</sup>C-bus latches.

In non-I<sup>2</sup>C-bus mode, pins SCL and SDA behave as open drain outputs showing clip detection diagnostics. Pin SCL shows clip diagnostics from channels 1 and 2. Pin SDA shows clip diagnostics from channels 3 and 4.

**Table 7. Available data on pins DIAG, SCL and SDA**

| Diagnostic                                             | I <sup>2</sup> C-bus mode | Non-I <sup>2</sup> C-bus mode |                  |                  |
|--------------------------------------------------------|---------------------------|-------------------------------|------------------|------------------|
|                                                        | Pin DIAG                  | Pin DIAG                      | Pin SCL          | Pin SDA          |
| Power-on reset                                         | yes                       | yes                           | no               | no               |
| UVP or OVP                                             | yes                       | yes                           | no               | no               |
| Clip detection                                         | selectable                | no                            | channels 1 and 2 | channels 3 and 4 |
| Temperature pre-warning                                | selectable                | yes                           | no               | no               |
| OCP/WP                                                 | yes                       | yes                           | no               | no               |
| DCP                                                    | selectable                | yes                           | no               | no               |
| OTP                                                    | yes                       | yes                           | no               | no               |
| Watchdog alarm                                         | yes                       | yes                           | no               | no               |
| AC load detection; see <a href="#">Section 8.4.2.2</a> | selectable                | no                            | no               | no               |

When OCP is triggered, the open-drain DIAG output is activated. The diagnostic output signal during different short circuit conditions is illustrated in [Figure 7](#).

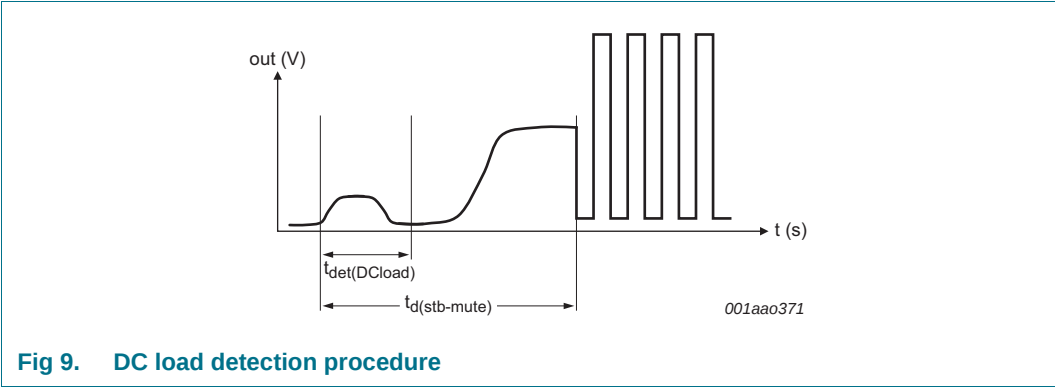
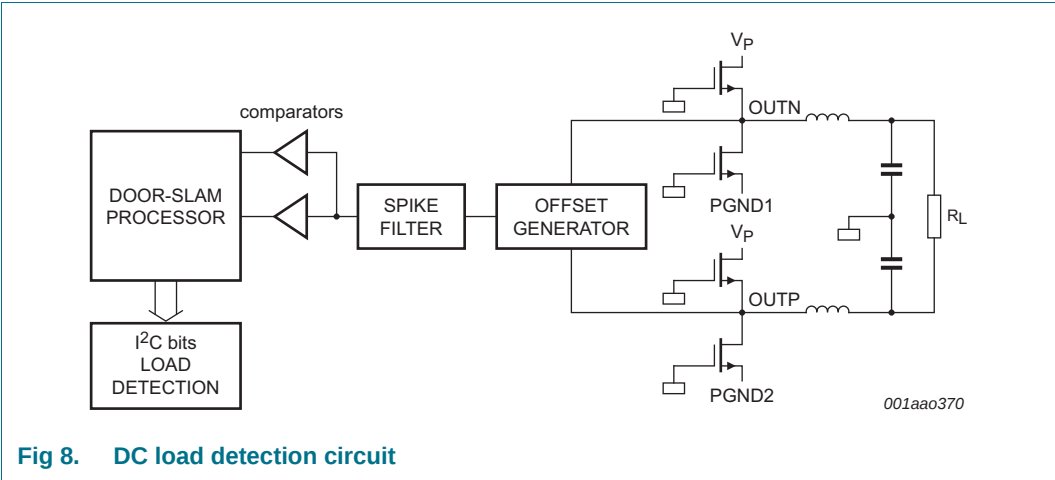


**Fig 7. Diagnostic output for short circuit conditions**

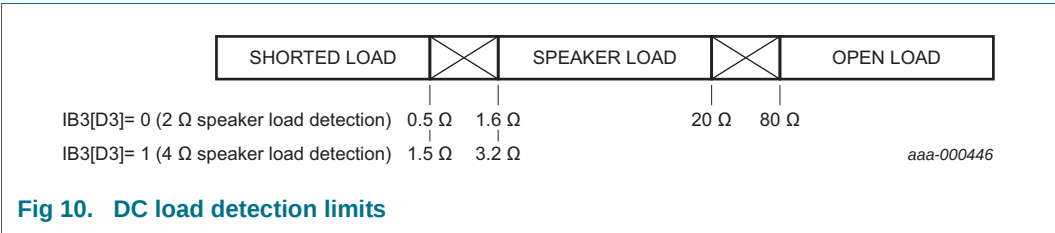
## 8.4.2 Load identification (I<sup>2</sup>C-bus mode only)

### 8.4.2.1 DC load detection

DC load detection is only available in I<sup>2</sup>C-bus mode and is controlled using bit IB2[D2]. The default setting is logic 0 for bit IB2[D2] which disables DC load detection. DC load detection is enabled when bit IB2[D2] = 1. Load detection takes place before the SVRR capacitor is charged and before the class-D amplifier output stage starts switching. The start-up time from Standby mode to Mute mode is increased by  $t_{\text{det(DCload)}}$  (see [Figure 8](#)).



An inaudible current test pulse is created between the amplifier outputs. The external capacitor connected to pin SEL\_MUTE is used for timing. Load diagnostics based on the voltage difference between pins OUTxP and OUTxN are shown in [Figure 8](#) and [Figure 9](#)



DC Load detection has built in spike filtering and a door-slam processor to remove disturbances caused by switching relays in the wiring harness, EMI or the closing of a car door. Reliable load detection is performed in one diagnostic cycle with these filter techniques.

8.4.2.2 AC load detection (tweeter detection)

AC load detection is only available in I<sup>2</sup>C-bus mode and is controlled using bit IB1[D2]. The default setting for bit IB1[D2] = 0 disables AC load detection. When AC load detection is enabled, the average amplifier load current is measured and compared with a reference level. Pin DIAG is activated when this threshold is reached. Using this information, AC load detection can be performed using a predetermined input signal frequency and level.

The frequency and signal level should be chosen so that the average load current exceeds the programmed current threshold when the AC coupled load (tweeter) is present.

### 8.4.3 Clip detection

Clip detection gives information for clip levels exceeding a threshold defined as the THD level of a sinusoidal output signal. The default value of this threshold is set at 0.2 %, but can be set to 10 % using IB3[D4] = 1.

In non-I<sup>2</sup>C-bus mode pins SCL and SDA behave as open drain outputs showing THD = 0.2 % clip detection diagnostics. Pin SCL shows clip diagnostics from channels 1 and 2. Pin SDA shows clip diagnostics from channels 3 and 4.

In I<sup>2</sup>C-bus mode pin DIAG is used as output of the clip detection circuitry for all channels. Setting bit IBx[D5] to logic 0 in I<sup>2</sup>C-bus mode defines which channel reports clip information on the DIAG pin. Clip detection is disabled when the AC load detection is active.

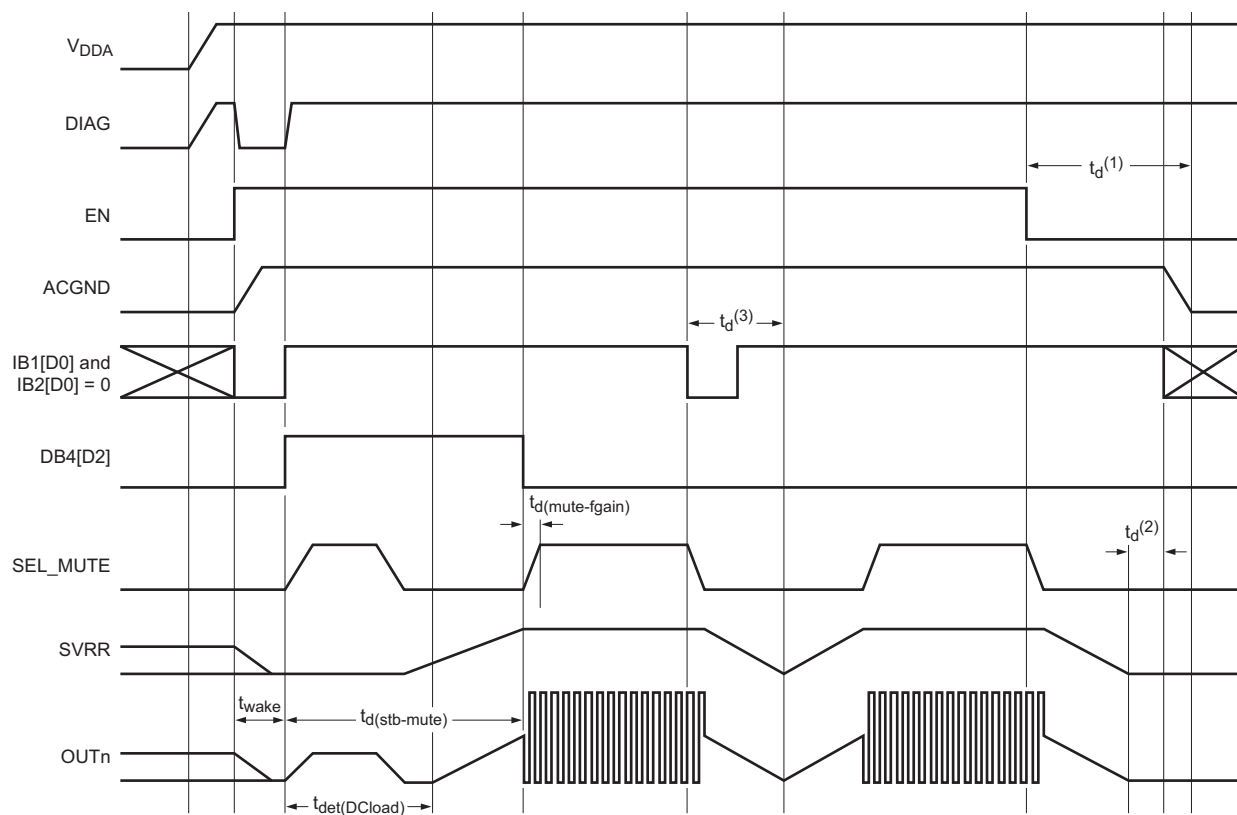
### 8.4.4 Start-up and shutdown sequence

To prevent switch on or switch off 'pop noises', a capacitor ( $C_{SVRR}$ ) connected to pin SVRR is used to smooth start-up and shutdown. During start-up and shutdown, the output voltage tracks the voltage on pin SVRR. Increasing  $C_{SVRR}$  results in a longer start-up and shutdown time. Enhanced pop noise performance is achieved by muting the amplifier until the SVRR voltage reaches its final value and the outputs start switching. The value of capacitor  $C_{ON}$  connected to pin SEL\_MUTE determines the unmute and mute timing. The voltage on pin SEL\_MUTE determines the amplifier gain. Increasing  $C_{ON}$  increases the unmute and mute times. In addition, a larger  $C_{ON}$  value increases the DC load detection cycle time.

When the amplifier is switched off with an I<sup>2</sup>C-bus command or by pulling pin EN LOW, the amplifier is first muted and then capacitor ( $C_{SVRR}$ ) is discharged.

In Slave mode, the device enters the off state immediately after capacitor ( $C_{SVRR}$ ) is discharged. In Master mode, the clock is kept active by an additional delay ( $t_d^{(2)}$ ) of approximately 50 ms to allow slave devices to enter the off state.

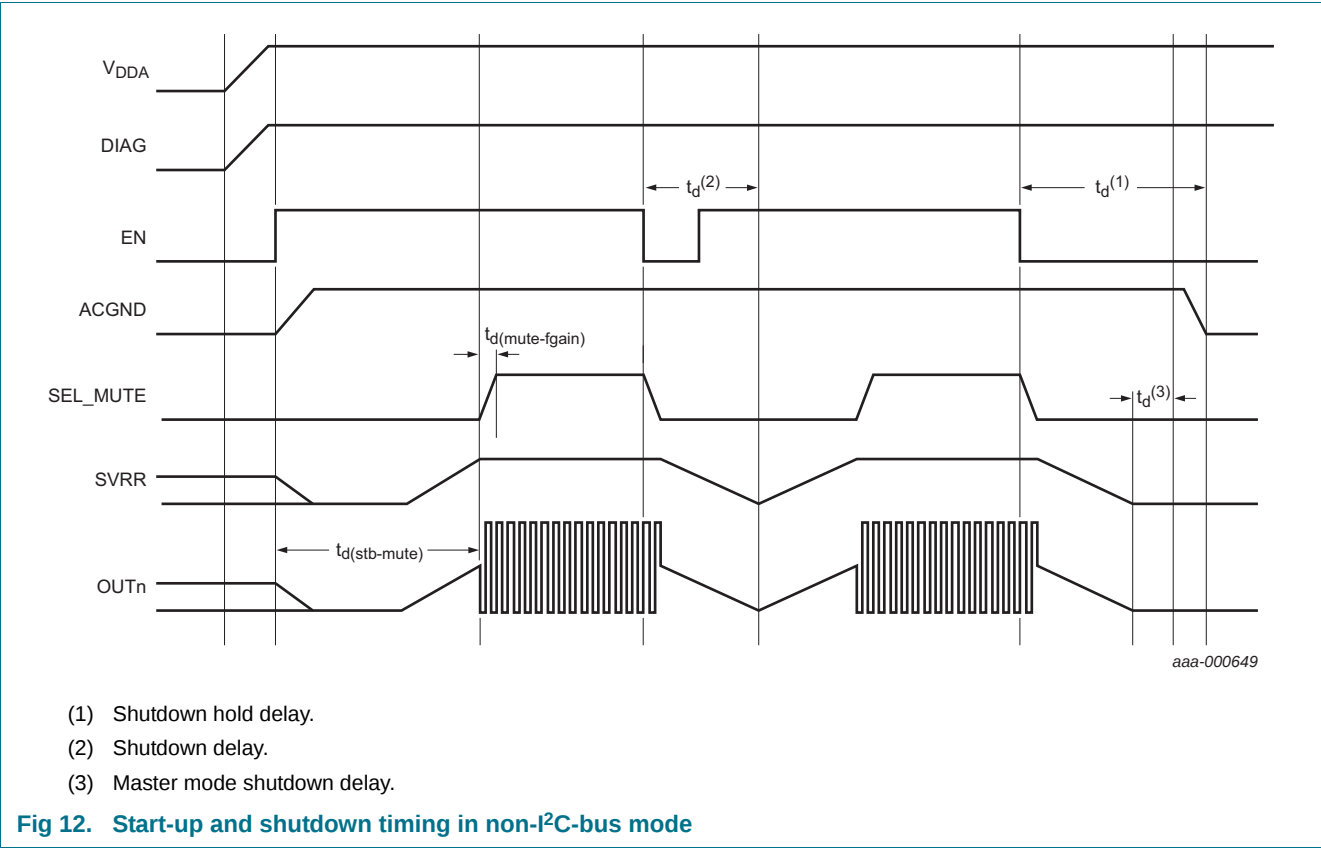
A clock signal is needed during the start-up and shutdown sequence. When an external clock is connected to pin OSCIO (in Slave mode), the clock must remain active during the shutdown sequence for delay ( $t_d^{(1)}$ ) to ensure that the slaved TDF8530 devices are able to enter the off state. A watchdog is added to protect against clock failure.



aaa-000447

- (1) Shutdown hold delay.
- (2) Master mode shutdown delay.
- (3) Shutdown delay.

**Fig 11. Start-up and shutdown timing in I<sup>2</sup>C-bus mode with DC load detection**



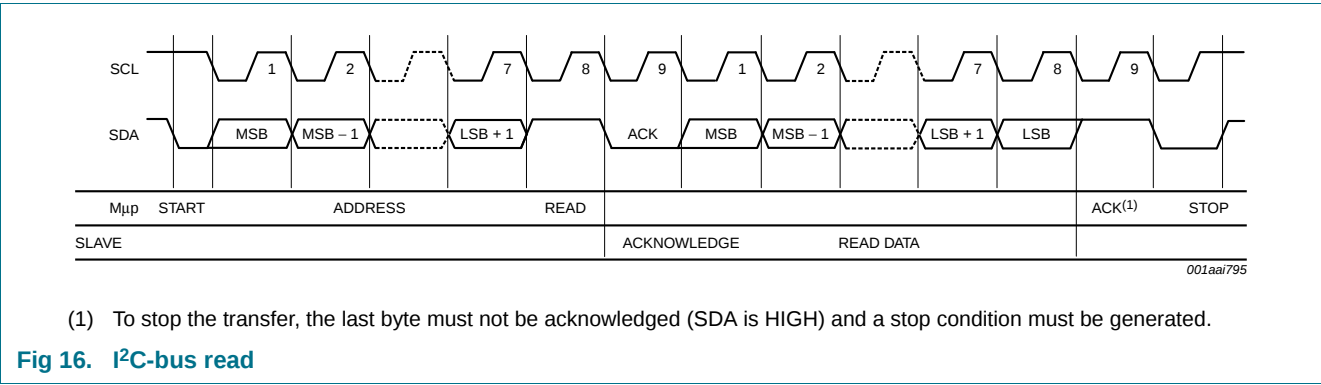
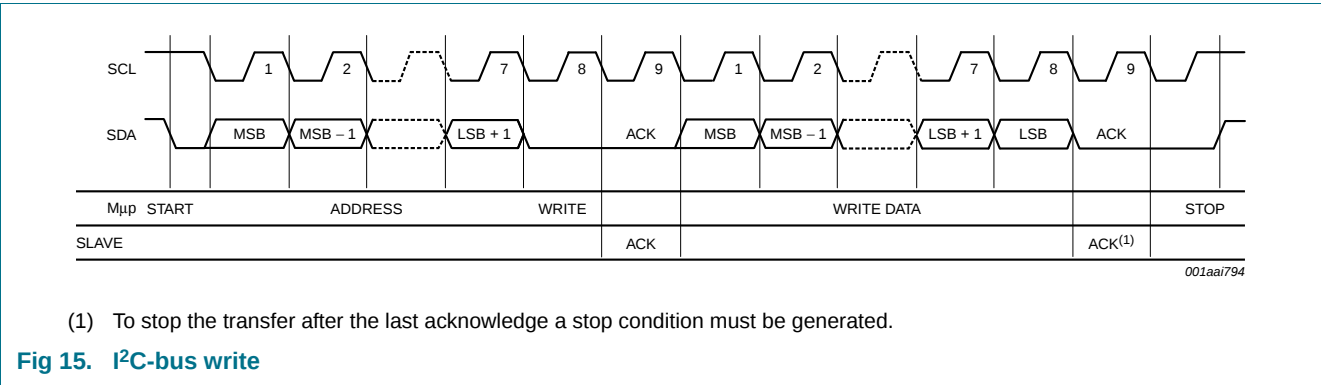
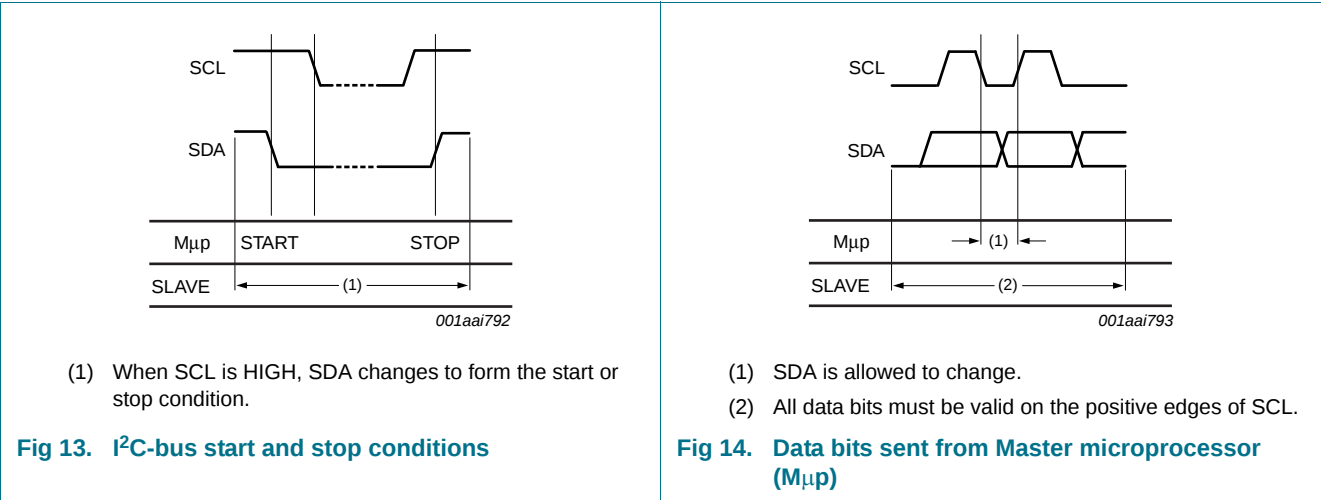
9. I<sup>2</sup>C-bus specification

TDF8530 address with hardware address select.

Table 8. I<sup>2</sup>C-bus write address selection using pins MOD and ADS

| R <sub>ADS</sub> (kΩ) | R <sub>MOD</sub> (kΩ)                |     |     |     | R/W                   |
|-----------------------|--------------------------------------|-----|-----|-----|-----------------------|
|                       | 0 <sup>[1]</sup>                     | 6.8 | 33  | 100 |                       |
| 100                   | 44h                                  | 54h | 64h | 74h | 1 = Read from TDF8530 |
| 33                    | 42h                                  | 52h | 62h | 72h | 0 = Write to TDF8530  |
| 6.8                   | 40h                                  | 50h | 60h | 70h |                       |
| 0 <sup>[1]</sup>      | non-I <sup>2</sup> C-bus mode select |     |     |     |                       |

[1] Short circuited to ground.



## 9.1 Instruction bytes

If R/W bit = 0, the TDF8530 expects four instruction bytes: IB1, IB2, IB3, and IB4. Reserved instruction bits must be programmed to zero. After a power-on reset, all instruction bits are set to zero.

**Table 9. Instruction byte descriptions**

| Bit | Value | Description                                              |                                      |                                                                           |                                                                                                                       |
|-----|-------|----------------------------------------------------------|--------------------------------------|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
|     |       | Instruction byte IB1                                     | Instruction byte IB2                 | Instruction byte IB3                                                      | Instruction byte IB4                                                                                                  |
| D7  | 0     | offset detection on pin DIAG                             | offset protection on                 | latch information on pins ADS and MOD when the amplifier starts switching | undervoltage protection threshold for 6 V minimum supply                                                              |
|     | 1     | no offset detection on pin DIAG                          | offset protection off                | latch information on pins ADS and MOD                                     | undervoltage protection threshold for 8 V minimum supply                                                              |
| D6  | 0     | channel 1 offset monitoring on                           | channel 2 offset monitoring on       | channel 3 offset monitoring on                                            | channel 4 offset monitoring on                                                                                        |
|     | 1     | channel 1 offset monitoring off                          | channel 2 offset monitoring off      | channel 3 offset monitoring off                                           | channel 4 offset monitoring off                                                                                       |
| D5  | 0     | channel 1 clip detect on pin DIAG                        | channel 2 clip detect on pin DIAG    | channel 3 clip detect on pin DIAG                                         | channel 4 clip detect on pin DIAG                                                                                     |
|     | 1     | channel 1 no clip detect on pin DIAG                     | channel 2 no clip detect on pin DIAG | channel 3 no clip detect on pin DIAG                                      | channel 4 no clip detect on pin DIAG                                                                                  |
| D4  | 0     | disable frequency hopping                                | thermal pre-warning on pin DIAG      | clip detection at THD = 0.2 %                                             | enable phase staggering between channels 1 and 2, and 3 and 4                                                         |
|     | 1     | enable frequency hopping <sup>[1]</sup>                  | no thermal pre-warning on pin DIAG   | clip detection at THD = 10 %                                              | no phase staggering between channels 1 and 2, and 3 and 4                                                             |
| D3  | 0     | oscillator frequency as set with R <sub>osc</sub> – 10 % | temperature pre-warning at 140 °C    | 1 Ω detection level for shorted load detection                            | phase shift in slave mode with respect to master clock, oscillator phase shift bits IB4[D3] to IB4[D2] <sup>[2]</sup> |
|     | 1     | oscillator frequency as set with R <sub>osc</sub> + 10 % | temperature pre-warning at 120 °C    | 2 Ω detection level for shorted load detection                            |                                                                                                                       |
| D2  | 0     | disable AC-load detection on pin DIAG                    | DC-load detection disabled           | f <sub>OSCIO</sub> = f <sub>osc</sub> <sup>[3]</sup>                      |                                                                                                                       |
|     | 1     | enable AC-load detection on pin DIAG                     | DC-load detection enabled            | f <sub>OSCIO</sub> = 2 × f <sub>osc</sub> <sup>[3]</sup>                  |                                                                                                                       |
| D1  | 0     | channel 1 enabled                                        | channel 2 enabled                    | channel 3 enabled                                                         | channel 4 enabled                                                                                                     |
|     | 1     | channel 1 disabled                                       | channel 2 disabled                   | channel 3 disabled                                                        | channel 4 disabled                                                                                                    |
| D0  | 0     | TDF8530 in Standby mode                                  | all channels operating               | AD modulation                                                             | oscillator watchdog enabled during amplifier shut down only                                                           |
|     | 1     | TDF8530 in Mute or Operating modes <sup>[4]</sup>        | all channels muted                   | BD modulation                                                             | oscillator watchdog enabled                                                                                           |

[1] See IB1[D3].

[2] See [Table 10 “Phase shift bit settings”](#) for information on IB4[D3] to IB4[D2].

[3] See [Table 4 “Oscillator modes”](#)

[4] See IB2[D0].

Table 10. Phase shift bit settings

| D3 | D2 | Phase             |
|----|----|-------------------|
| 0  | 0  | 0                 |
| 0  | 1  | $\frac{1}{8} \pi$ |
| 1  | 0  | $\frac{2}{8} \pi$ |
| 1  | 1  | $\frac{3}{8} \pi$ |

## 9.2 Data bytes

If R/W = 1, the TDF8530 sends four data bytes to the microprocessor (DB1, DB2, DB3 and DB4). All short diagnostic and offset protection bits and bits OTP, UVP and OVP are latched. In addition, all bits are reset after a read operation except the DC load detection bits (DBx[D3,D4], DB1[D6]). The default setting for all bits is logic 0.

Table 11. Description of data bytes

| Bit | Value | DB1 channel 1                                     | DB2 channel 2                           | DB3 channel 3                        | DB4 channel 4                        |
|-----|-------|---------------------------------------------------|-----------------------------------------|--------------------------------------|--------------------------------------|
| D7  | 0     | at least 1 instruction bit set to logic 1         | below maximum temperature               | reserved                             | reserved                             |
|     | 1     | all instruction bits are set to logic 0           | maximum temperature protection occurred | -                                    | -                                    |
| D6  | 0     | invalid DC load data                              | no temperature warning                  | reserved                             | reserved                             |
|     | 1     | valid DC load data                                | temperature pre-warning active          | -                                    | -                                    |
| D5  | 0     | no overvoltage                                    | no undervoltage                         | reserved                             | reserved                             |
|     | 1     | overvoltage protection occurred                   | undervoltage protection occurred        | -                                    | -                                    |
| D4  | 0     | speaker load channel 1                            | speaker load channel 2                  | speaker load channel 3               | speaker load channel 4               |
|     | 1     | open load channel 1                               | open load channel 2                     | open load channel 3                  | open load channel 4                  |
| D3  | 0     | no shorted load channel 1                         | no shorted load channel 2               | no shorted load channel 3            | no shorted load channel 4            |
|     | 1     | shorted load channel 1                            | shorted load channel 2                  | shorted load channel 3               | shorted load channel 4               |
| D2  | 0     | no offset                                         | PLL not locked (slave mode)             | clock running                        | start up diagnostics finished        |
|     | 1     | offset detected on channels selected with IBx[D6] | PLL locked (slave mode)                 | clock failure                        | start up diagnostics in progress     |
| D1  | 0     | no short to V <sub>P</sub> channel 1              | no short to V <sub>P</sub> channel 2    | no short to V <sub>P</sub> channel 3 | no short to V <sub>P</sub> channel 4 |
|     | 1     | short to V <sub>P</sub> channel 1                 | short to V <sub>P</sub> channel 2       | short to V <sub>P</sub> channel 3    | short to V <sub>P</sub> channel 4    |
| D0  | 0     | no short to ground channel 1                      | no short to ground channel 2            | no short to ground channel 3         | no short to ground channel 4         |
|     | 1     | short to ground channel 1                         | short to ground channel 2               | short to ground channel 3            | short to ground channel 4            |

Data byte DB1[D7] indicates whether the instruction bits have been set to logic 0. In principle, DB1[D7] is set after a POR or when all the instruction bits are programmed to logic 0. Pin DIAG is driven LOW when bit DB1[D7] = 1.

## 10. Limiting values

**Table 12. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol                 | Parameter                       | Conditions                                                                                   | Min    | Max            | Unit |
|------------------------|---------------------------------|----------------------------------------------------------------------------------------------|--------|----------------|------|
| V <sub>P</sub>         | supply voltage                  | Operating mode                                                                               | -      | 29             | V    |
|                        |                                 | off state                                                                                    | [1] -1 | +50            | V    |
|                        |                                 | load dump; duration<br>50 ms; t <sub>r</sub> > 2.5 ms                                        | -      | 50             | V    |
| I <sub>ORM</sub>       | repetitive peak output current  | maximum output current limiting                                                              | [2] 8  | -              | A    |
| I <sub>OM</sub>        | peak output current             | non-repetitive                                                                               | -      | 18             | A    |
| I <sub>sink(max)</sub> | maximum sink current            | pin DIAG                                                                                     | 0      | 5              | mA   |
| V <sub>i</sub>         | input voltage                   | referred to GNDD:<br>pins SCL, SDA and OSCIO                                                 | 0      | 5.5            | V    |
|                        |                                 | referred to AGND:<br>pins ADS, MOD, SSM,<br>EN and SEL_MUTE                                  | 0      | 5.5            | V    |
|                        |                                 | referred to AGND:<br>pins IN1P, IN2P, IN3P,<br>IN4P and INN                                  | 0      | 10             | V    |
| V <sub>o</sub>         | output voltage                  | referred to GNDD:<br>pin DIAG                                                                | 0      | 10             | V    |
| R <sub>ESR</sub>       | equivalent series resistance    | as seen between pins V <sub>P</sub><br>and PGNDx                                             | -      | 200            | mΩ   |
| T <sub>j</sub>         | junction temperature            |                                                                                              | -      | 150            | °C   |
| T <sub>stg</sub>       | storage temperature             |                                                                                              | -55    | +150           | °C   |
| T <sub>amb</sub>       | ambient temperature             |                                                                                              | -40    | +85            | °C   |
| V <sub>ESD</sub>       | electrostatic discharge voltage | HBM                                                                                          | [3]    |                |      |
|                        |                                 | C = 100 pF;<br>R <sub>s</sub> = 1.5 kΩ                                                       | -      | 2000           | V    |
|                        |                                 | CDM                                                                                          | [4]    |                |      |
|                        |                                 | non-corner pins<br>(except pin 30, V <sub>DDA</sub> )                                        | -      | 500            | V    |
|                        |                                 | pin 30, V <sub>DDA</sub>                                                                     | -      | 300            | V    |
|                        |                                 | corner pins                                                                                  | -      | 750            | V    |
| V <sub>(prot)</sub>    | protection voltage              | AC and DC short circuit<br>voltage of output pins<br>across load and to<br>supply and ground | [5] 0  | V <sub>P</sub> | V    |

[1] Floating condition assumed for outputs.

[2] Current limiting concept.

[3] Human Body Model (HBM).

[4] Charged-Device Model (CDM).

[5] The output pins are defined as the output pins of the filter connected between the TDF8530 output pins and the load.

## 11. Thermal characteristics

Table 13. Thermal characteristics

| Symbol        | Parameter                                   | Conditions  | Typ | Unit |
|---------------|---------------------------------------------|-------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 35  | K/W  |
| $R_{th(j-c)}$ | thermal resistance from junction to case    |             | 1   | K/W  |

## 12. Static characteristics

Table 14. Static characteristics

$V_P = 14.4\text{ V}$ ;  $f_{osc} = 315\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

| Symbol                                                 | Parameter                | Conditions                                                         | Min | Typ  | Max | Unit          |
|--------------------------------------------------------|--------------------------|--------------------------------------------------------------------|-----|------|-----|---------------|
| <b>Supply</b>                                          |                          |                                                                    |     |      |     |               |
| $V_P$                                                  | supply voltage           | Operating mode; on pins $V_{DDA}$ and $V_{P1}$ and $V_{P2}$        | 6   | 14.4 | 24  | V             |
| $I_P$                                                  | supply current           | off state; $T_j \leq 85\text{ °C}$ ; $V_P = 14.4\text{ V}$         | -   | 2    | 10  | $\mu\text{A}$ |
| $I_{q(tot)}$                                           | total quiescent current  | Operating mode; no load, no snubbers and no filter connected       | -   | 185  | 200 | mA            |
| <b>I<sup>2</sup>C-bus interface: pins SCL and SDA</b>  |                          |                                                                    |     |      |     |               |
| $V_{IL}$                                               | LOW-level input voltage  |                                                                    | 0   | -    | 1.5 | V             |
| $V_{IH}$                                               | HIGH-level input voltage |                                                                    | 2.3 | -    | 5.5 | V             |
| $V_{OL}$                                               | LOW-level output voltage | pin SDA; $I_{load} = 5\text{ mA}$                                  | 0   | -    | 0.4 | V             |
| <b>Enable and SEL_MUTE input: pins EN and SEL_MUTE</b> |                          |                                                                    |     |      |     |               |
| $V_i$                                                  | input voltage            | pin EN; off state                                                  | 0   | -    | 0.8 | V             |
|                                                        |                          | pin EN; Standby mode; I <sup>2</sup> C-bus mode                    | 2   | -    | 5   | V             |
|                                                        |                          | pin EN; Mute mode or Operating mode; non-I <sup>2</sup> C-bus mode | 2   | -    | 5   | V             |
|                                                        |                          | pin SEL_MUTE; Mute mode; voltage on pin EN > 2 V                   | 0   | -    | 0.8 | V             |
|                                                        |                          | pin SEL_MUTE; Operating mode; voltage on pin EN > 2 V              | 3   | -    | 5   | V             |
| $I_i$                                                  | input current            | pin EN; 2.5 V                                                      | -   | -    | 5   | $\mu\text{A}$ |
|                                                        |                          | pin SEL_MUTE; Operating mode; 0.8 V                                | -   | -    | 50  | $\mu\text{A}$ |

**Table 14. Static characteristics ...continued** $V_P = 14.4\text{ V}$ ;  $f_{osc} = 315\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

| Symbol                                                                            | Parameter                                      | Conditions                                                         | Min                   | Typ  | Max | Unit |
|-----------------------------------------------------------------------------------|------------------------------------------------|--------------------------------------------------------------------|-----------------------|------|-----|------|
| Diagnostic output                                                                 |                                                |                                                                    |                       |      |     |      |
| THD <sub>clip</sub>                                                               | total harmonic distortion clip detection level | IB3[D4] = 0                                                        | -                     | 0.2  | -   | %    |
|                                                                                   |                                                | IB3[D4] = 1                                                        | -                     | 10   | -   | %    |
| V <sub>th(offset)</sub>                                                           | threshold voltage for offset detection         | V <sub>DDA</sub> > 8 V                                             | <a href="#">[1]</a> 1 | 2    | 3   | V    |
| V <sub>OL</sub>                                                                   | LOW-level output voltage                       | DIAG, SCL or SDA pins; diagnostic activated; I <sub>o</sub> = 1 mA | -                     | -    | 0.3 | V    |
| I <sub>L</sub>                                                                    | leakage current                                | DIAG, SCL or SDA pins; diagnostic not activated                    | -                     | -    | 50  | μA   |
| Audio inputs; pins INN, IN1P, IN2P, IN3P and IN4P                                 |                                                |                                                                    |                       |      |     |      |
| V <sub>i</sub>                                                                    | input voltage                                  |                                                                    | -                     | 2.45 | -   | V    |
| SVRR voltage and ACGND input bias voltage in Mute and Operating modes             |                                                |                                                                    |                       |      |     |      |
| V <sub>ref</sub>                                                                  | reference voltage                              | input ACGND pin                                                    | -                     | 2.45 | -   | V    |
|                                                                                   |                                                | half supply reference SVRR pin                                     | -                     | 7.2  | -   | V    |
| Amplifier outputs; pins OUT1N, OUT1P, OUT2N, OUT2P, OUT3N, OUT3P, OUT4N and OUT4P |                                                |                                                                    |                       |      |     |      |
| V <sub>O(offset)</sub>                                                            | output offset voltage                          | Mute mode                                                          | -                     | -    | 25  | mV   |
|                                                                                   |                                                | Operating mode                                                     | <a href="#">[2]</a> - | -    | 70  | mV   |
| Stabilizer output; pins VSTAB1 and VSTAB2                                         |                                                |                                                                    |                       |      |     |      |
| V <sub>o</sub>                                                                    | output voltage                                 | stabilizer output in Mute mode and Operating mode                  | -                     | 11   | -   | V    |
| Voltage protections                                                               |                                                |                                                                    |                       |      |     |      |
| V <sub>(prot)</sub>                                                               | protection voltage                             | undervoltage protection level 1; falling supply; IB4[D7] = 0       | 5.5                   | 5.75 | 6   | V    |
|                                                                                   |                                                | undervoltage protection level 2; falling supply; IB4[D7] = 1       | 7.2                   | 7.6  | 8   | V    |
|                                                                                   |                                                | overvoltage protection level                                       | 26.2                  | 27   | -   | V    |
|                                                                                   |                                                | V <sub>P</sub> at which a POR occurs                               | -                     | 4.4  | -   | V    |
| Current protection                                                                |                                                |                                                                    |                       |      |     |      |
| I <sub>O(ocp)</sub>                                                               | overcurrent protection output current          | current limiting concept                                           | 8                     | 9    | -   | A    |
| Temperature protection                                                            |                                                |                                                                    |                       |      |     |      |
| T <sub>prot</sub>                                                                 | protection temperature                         |                                                                    | -                     | 152  | -   | °C   |
| T <sub>act(th_fold)</sub>                                                         | thermal foldback activation temperature        | gain = −1 dB                                                       | -                     | 145  | -   | °C   |
| T <sub>j(AV)(warn1)</sub>                                                         | average junction temperature for pre-warning 1 | IB2[D3] = 0; non-I <sup>2</sup> C-bus mode                         | -                     | 140  | -   | °C   |
| T <sub>j(AV)(warn2)</sub>                                                         | average junction temperature for pre-warning 2 | IB2[D3] = 1                                                        | -                     | 120  | -   | °C   |

**DC load detection levels: I<sup>2</sup>C-bus mode only**

I<sup>2</sup>C-bus controlled quad channel Class-D power amplifier**Table 14. Static characteristics ...continued** $V_P = 14.4\text{ V}$ ;  $f_{osc} = 315\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

| Symbol                                                   | Parameter                                  | Conditions                                                                                                                           | Min | Typ | Max | Unit     |
|----------------------------------------------------------|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|----------|
| $Z_{th(load)}$                                           | load detection threshold impedance         | for normal speaker load; IB3[D3] = 0; 1 $\Omega$ shorted load detection level                                                        | 1.6 | -   | 20  | $\Omega$ |
|                                                          |                                            | for normal speaker load; IB3[D3] = 1; 2 $\Omega$ shorted load detection level                                                        | 3.2 | -   | 20  | $\Omega$ |
| $Z_{th(open)}$                                           | open load detection threshold impedance    |                                                                                                                                      | 80  | -   | -   | $\Omega$ |
| $Z_{th(short)}$                                          | shorted load detection threshold impedance | for shorted speaker load; IB3[D3] = 0; 1 $\Omega$ shorted load detection level                                                       | -   | -   | 0.5 | $\Omega$ |
|                                                          |                                            | for shorted speaker load; IB3[D3] = 1; 2 $\Omega$ shorted load detection level                                                       | -   | -   | 1.5 | $\Omega$ |
| AC load detection levels: I <sup>2</sup> C-bus mode only |                                            |                                                                                                                                      |     |     |     |          |
| $I_{th(o)det(load)AC}$                                   | AC load detection output threshold current |                                                                                                                                      | -   | 500 | -   | mA       |
| Start-up/shut-down/mute timing                           |                                            |                                                                                                                                      |     |     |     |          |
| $t_{wake}$                                               | wake-up time                               | on pin EN before first I <sup>2</sup> C-bus transmission is recognized                                                               | [3] | -   | 500 | $\mu$ s  |
| $t_{det(DCload)}$                                        | DC load detection time                     | C <sub>ON</sub> = 470 nF                                                                                                             | [3] | -   | 320 | ms       |
| $t_{d(stb-mute)}$                                        | delay time from standby to mute            | measured from amplifier enabling to start of unmute (no DC load detection); C <sub>SVRR</sub> = 47 $\mu$ F                           | -   | 125 | -   | ms       |
| $t_{d(mute-fgain)}$                                      | mute to full gain delay time               | C <sub>ON</sub> = 470 nF                                                                                                             | [4] | -   | 50  | ms       |
| $t_d$                                                    | delay time                                 | shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 1 V; C <sub>SVRR</sub> = 47 $\mu$ F; C <sub>ON</sub> = 470 nF | 130 | 190 | 250 | ms       |
|                                                          |                                            | shutdown hold delay time from pin EN LOW to ACGND LOW; voltage on pin ACGND < 1 V; Master mode                                       | -   | 400 | -   | ms       |
|                                                          |                                            | hold delay in Master mode to allow slaved devices to shut down<br>f <sub>osc</sub> = 315 kHz                                         | -   | 50  | -   | ms       |

[1] Maximum leakage current from DCP pin to ground = 3  $\mu\text{A}$ .

[2] DC output offset voltage is applied to the output gradually during the transition between Mute mode and Operating mode.

[3] I<sup>2</sup>C-bus mode only.

[4] The transition time between Mute mode and Operating mode is determined by the time constant on the SEL\_MUTE pin.

## 12.1 Switching characteristics

**Table 15. Switching characteristics**

$V_P = 14.4\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                           | Parameter                      | Conditions                                                                                                                            | Min                     | Typ                     | Max  | Unit |
|----------------------------------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-------------------------|------|------|
| Internal oscillator              |                                |                                                                                                                                       |                         |                         |      |      |
| f <sub>PWM</sub>                 | PWM frequency                  | R <sub>OSC</sub> = 39 kΩ                                                                                                              | -                       | 315                     | -    | kHz  |
| f <sub>PWM(range)</sub>          | PWM frequency range            | typical fixed frequency and Spread spectrum mode frequency based on the resistor value connected to pin OSCSET for the master setting | -                       | 300 to 500              | -    | kHz  |
| Master/slave setting (OSCIO pin) |                                |                                                                                                                                       |                         |                         |      |      |
| R <sub>OSC</sub>                 | oscillator resistance          | resistor value on pin OSCSET; master setting                                                                                          | 22                      | 39                      | 49   | kΩ   |
| V <sub>OL</sub>                  | LOW-level output voltage       | output                                                                                                                                | -                       | -                       | 0.8  | V    |
| V <sub>OH</sub>                  | HIGH-level output voltage      | output                                                                                                                                | 4                       | -                       | -    | V    |
| f <sub>o</sub>                   | output frequency               | IB3[D2] = 0; R <sub>OSC</sub> = 49 kΩ                                                                                                 | 200                     | 250                     | 300  | kHz  |
|                                  |                                | IB3[D2] = 1; R <sub>OSC</sub> = 49 kΩ                                                                                                 | 400                     | 500                     | 600  | kHz  |
|                                  |                                | IB3[D2] = 0; R <sub>OSC</sub> = 22 kΩ                                                                                                 | 460                     | 500                     | 575  | kHz  |
|                                  |                                | IB3[D2] = 1; R <sub>OSC</sub> = 22 kΩ                                                                                                 | 920                     | 1050                    | 1150 | kHz  |
| V <sub>IL</sub>                  | LOW-level input voltage        | input                                                                                                                                 | -                       | -                       | 0.8  | V    |
| V <sub>IH</sub>                  | HIGH-level input voltage       | input                                                                                                                                 | 3                       | -                       | -    | V    |
| f <sub>i</sub>                   | input frequency                | IB3[D2] = 0                                                                                                                           | 300                     | -                       | 500  | kHz  |
|                                  |                                | IB3[D2] = 1                                                                                                                           | <a href="#">[1]</a> 600 | -                       | 1000 | kHz  |
| C <sub>OSCIO</sub>               | capacitance on pin OSCIO       | output, used by slave with PLL operation                                                                                              | -                       | -                       | 560  | pF   |
|                                  |                                | output, used by slave without PLL operation                                                                                           | -                       | -                       | 68   | pF   |
| Spread spectrum mode setting     |                                |                                                                                                                                       |                         |                         |      |      |
| Δf <sub>OSC</sub>                | oscillator frequency variation | between maximum and minimum values; Spread spectrum mode activated                                                                    | -                       | 10                      | -    | %    |
| f <sub>SW</sub>                  | switching frequency            | Spread spectrum mode activated; C <sub>SSM</sub> = 1 μF                                                                               | -                       | 7                       | -    | Hz   |
| Frequency hopping                |                                |                                                                                                                                       |                         |                         |      |      |
| f <sub>OSC(int)</sub>            | internal oscillator frequency  | change positive; IB1[D4] = 1; IB1[D3] = 1                                                                                             | -                       | f <sub>OSC</sub> + 10 % | -    | kHz  |
|                                  |                                | change negative; IB1[D4] = 1; IB1[D3] = 0                                                                                             | -                       | f <sub>OSC</sub> – 10 % | -    | kHz  |

[1] Amplifier output stage switching frequency is half the external oscillator frequency.

### 13. Dynamic characteristics

**Table 16. Dynamic characteristics**

$V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f_i = 1\text{ kHz}$ ;  $f_{osc} = 315\text{ kHz}$ ;  $R_{S(L)} < 0.04\ \Omega$  [1];  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

| Symbol             | Parameter                      | Conditions                                          | Min    | Typ  | Max | Unit          |
|--------------------|--------------------------------|-----------------------------------------------------|--------|------|-----|---------------|
| $P_o$              | output power                   | THD = 1 %; $R_L = 4\ \Omega$                        | [2] 18 | 20   | -   | W             |
|                    |                                | THD = 10 %; $R_L = 4\ \Omega$                       | 24     | 26   | -   | W             |
|                    |                                | square wave (EIAJ); $R_L = 4\ \Omega$               | -      | 40   | -   | W             |
|                    |                                | $V_P = 24\text{ V}$ ; THD = 10 %; $R_L = 4\ \Omega$ | -      | 70   | -   | W             |
|                    |                                | THD = 1 %; $R_L = 2\ \Omega$                        | 29     | 33   | -   | W             |
|                    |                                | THD = 10 %; $R_L = 2\ \Omega$                       | 39     | 45   | -   | W             |
|                    |                                | square wave (EIAJ); $R_L = 2\ \Omega$               | -      | 66   | -   | W             |
|                    |                                | $V_P = 24\text{ V}$ ; THD = 10 %; $R_L = 2\ \Omega$ | -      | 100  | -   | W             |
| THD                | total harmonic distortion      | $f_i = 1\text{ kHz}$ ; $P_o = 1\text{ W}$           | [3] -  | 0.02 | 0.1 | %             |
| $G_{V(cl)}$        | closed-loop voltage gain       |                                                     | 25     | 26   | 27  | dB            |
| $\alpha_{CS}$      | channel separation             | $f_i = 1\text{ kHz}$ ; $P_o = 1\text{ W}$           | 60     | 70   | -   | dB            |
| SVRR               | supply voltage rejection ratio | Operating mode                                      |        |      |     |               |
|                    |                                | BD mode; $f_{ripple} = 100\text{ Hz}$               | [4] -  | 70   | -   | dB            |
|                    |                                | BD mode; $f_{ripple} = 1\text{ kHz}$                | [4] -  | 70   | -   | dB            |
|                    |                                | Mute mode                                           |        |      |     |               |
|                    |                                | BD mode; $f_{ripple} = 1\text{ kHz}$                | [4] -  | 70   | -   | dB            |
|                    |                                | Off or Standby mode                                 |        |      |     |               |
|                    |                                | BD mode; $f_{ripple} = 1\text{ kHz}$                | [4] -  | 70   | -   | dB            |
| $ Z_{i(dif)} $     | differential input impedance   |                                                     | 30     | 50   | 75  | k $\Omega$    |
| $V_{n(o)}$         | output noise voltage           | Operating mode                                      |        |      |     |               |
|                    |                                | BD mode                                             | [5] -  | 60   | 77  | $\mu\text{V}$ |
|                    |                                | AD mode                                             | [5] -  | 100  | 140 | $\mu\text{V}$ |
|                    |                                | Mute mode                                           |        |      |     |               |
|                    |                                | BD mode                                             | [6] -  | 25   | 32  | $\mu\text{V}$ |
|                    |                                | AD mode                                             | [6] -  | 95   | 110 | $\mu\text{V}$ |
| $\alpha_{bal(ch)}$ | channel balance                |                                                     | -      | 0    | 1   | dB            |
| $\alpha_{mute}$    | mute attenuation               |                                                     | [7] 70 | -    | -   | dB            |
| CMRR               | common mode rejection ratio    | $V_{i(cm)} = 1\text{ V RMS}$                        | 65     | 80   | -   | dB            |
| $\eta_{po}$        | output power efficiency        | $P_o = 20\text{ W}$                                 | -      | 90   | -   | %             |

[1]  $R_{S(L)}$  is the sum of the inductor series resistance from the low-pass LC filter in the application together with all resistance from PCB traces or wiring between the output pin of the TDF8530 and the inductor to the measurement point. LC filter dimensioning is  $L = 10\ \mu\text{H}$ ,  $C = 1\ \mu\text{F}$  for  $4\ \Omega$  load and  $L = 5\ \mu\text{H}$ ,  $C = 2.2\ \mu\text{F}$  for  $2\ \Omega$  load.

[2] Output power is measured indirectly based on  $R_{DS(on)}$  measurement.

[3] Total harmonic distortion is measured at the bandwidth of 22 Hz to 20 kHz, AES brick wall. The maximum limit is guaranteed but may not be 100 % tested.

[4]  $V_{ripple} = V_{ripple(max)} = 1\text{ V (p-p)}$ ;  $R_S = 0\ \Omega$ .

[5]  $B = 22\text{ Hz to }20\text{ kHz}$ , AES brick wall,  $R_S = 0\ \Omega$ .

[6]  $B = 22\text{ Hz to }20\text{ kHz}$ , AES brick wall, independent of  $R_S$ .

[7]  $V_i = V_{i(max)} = 0.5\text{ V RMS}$ .

## 14. Application information

### 14.1 Output power estimation

The output power, just before clipping, can be estimated using [Equation 1](#):

$$P_{o(1)} = \frac{\left( \left( \frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)} \right) \times \left( 1 - t_{w(min)} \times \frac{f_{osc}}{2} \right) \times V_P \right)^2}{2 \times R_L} [W] \quad (1)$$

Where,

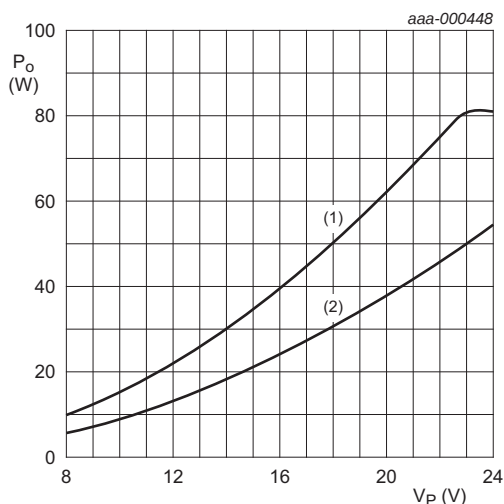
- $V_P$  = supply voltage (V)
- $R_L$  = load impedance ( $\Omega$ )
- $R_{DSon}$  = drain source on-state resistance ( $\Omega$ )
- $R_s$  = series resistance of the output inductor ( $\Omega$ )
- $t_{w(min)}$  = minimum pulse width(s) depending on output current
- $f_{osc}$  = oscillator frequency in Hz (typically 315 kHz)

The output power at 10 % THD can be estimated using [Equation 2](#):

$$P_{o(2)} = 1.25 \times P_{o(1)} \quad (2)$$

where  $P_{o(1)} = 0.5 \%$  and  $P_{o(2)} = 10 \%$

[Figure 17](#) and [Figure 18](#) show the estimated output power at THD = 0.5 % and THD = 10 % as a function of supply voltage for different load impedances.

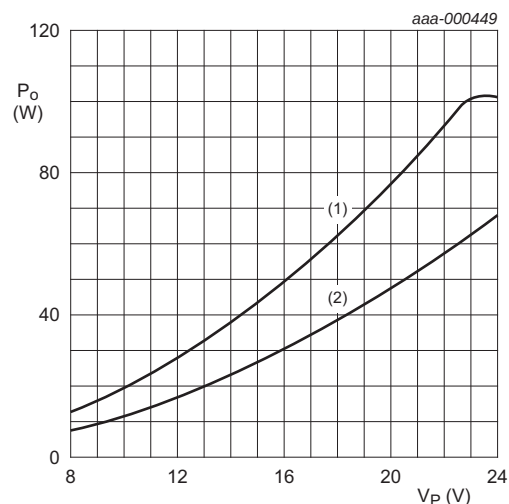


THD = 0.5 %.

$R_{DSon} = 0.190 \, \Omega$  (at  $T_j = 100 \, ^\circ\text{C}$ ),  $R_s = 0.05 \, \Omega$ ,  
 $t_{w(min)} = 150 \, \text{ns}$  and  $I_{O(ocp)} = 9 \, \text{A}$  (typical).

- (1)  $R_L = 2 \, \Omega$ .  
 (2)  $R_L = 4 \, \Omega$ .

Fig 17.  $P_o$  as a function of  $V_P$  with THD = 0.5 %



THD = 10 %.

$R_{DSon} = 0.190 \, \Omega$  (at  $T_j = 100 \, ^\circ\text{C}$ ),  $R_s = 0.05 \, \Omega$ ,  
 $t_{w(min)} = 150 \, \text{ns}$  and  $I_{O(ocp)} = 9 \, \text{A}$  (typical).

- (1)  $R_L = 2 \, \Omega$ .  
 (2)  $R_L = 4 \, \Omega$ .

Fig 18.  $P_o$  as a function of  $V_P$  with THD = 10 %

## 14.2 Output current limiting

The peak output current is internally limited to 8 A minimum. During normal operation, the output current should not exceed this threshold level otherwise the output signal will be distorted. The peak output current can be estimated using [Equation 3](#):

$$I_o \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 8 \, [\text{A}] \quad (3)$$

- $I_o$  = output current (A)
- $V_P$  = supply voltage (V)
- $R_L$  = load impedance ( $\Omega$ )
- $R_{DSon}$  = on-resistance of power switch ( $\Omega$ )
- $R_s$  = series resistance of output inductor ( $\Omega$ )

Example: A 2  $\Omega$  speaker can be used with a supply voltage of 22 V before current limiting is triggered.

Current limiting (clipping) avoids audio holes but causes distortion similar to voltage clipping.

## 14.3 Speaker configuration and impedance

A flat-frequency response (due to a 2<sup>nd</sup> order Butterworth filter) is obtained by changing the values of low-pass filter components ( $L_{LC}$ ,  $C_{LC}$ ) based on the speaker configuration and impedance. [Figure 19](#) shows the circuit and [Table 17](#) gives the required values.

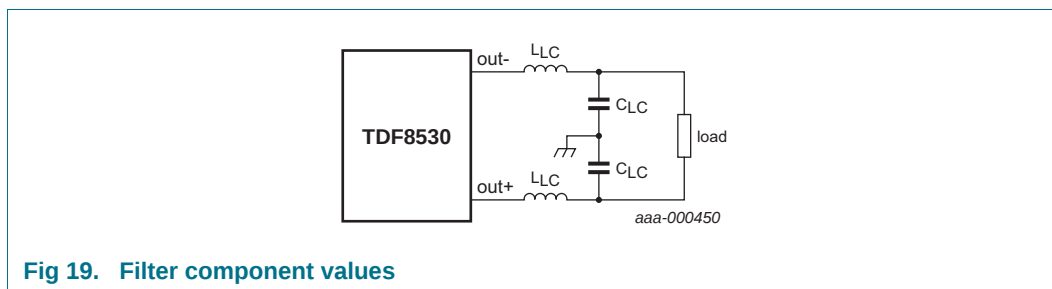


Table 17. Filter component values

| Load impedance ( $\Omega$ ) | $L_{LC}$ ( $\mu H$ ) | $C_{LC}$ ( $\mu F$ ) |
|-----------------------------|----------------------|----------------------|
| 2                           | 5                    | 2.2                  |
| 4                           | 10                   | 1                    |

#### 14.4 Heat sink requirements

In most applications, it is necessary to connect an external heat sink to the TDF8530. Thermal foldback activates at  $T_j = 140^\circ C$ . The expression in [Equation 4](#) shows the relationship between the maximum power dissipation before activation of thermal foldback and the total thermal resistance from junction to ambient:

$$R_{th(j-a)} = \frac{T_{j(max)} - T_{amb}}{P_{max}} [K/W] \quad (4)$$

$P_{max}$  is determined by the efficiency ( $\eta$ ) of the TDF8530. The efficiency measured as a function of output power is given in [Figure 25](#). The power dissipation can be derived as a function of output power (see [Figure 24](#)).

Example 1:

- $V_P = 14.4 V$
- $P_o = 4 \times 25 W$  into  $4 \Omega$  (THD = 10 % continuous)
- $T_{j(max)} = 140^\circ C$
- $T_{amb} = 25^\circ C$
- $P_{max} = 9.5 W$  (from [Figure 24](#))
- The required  $R_{th(j-a)} = 115^\circ C / 9.5 W = 12 K/W$

The total thermal resistance  $R_{th(j-a)}$  consists of:  $R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$

Where:

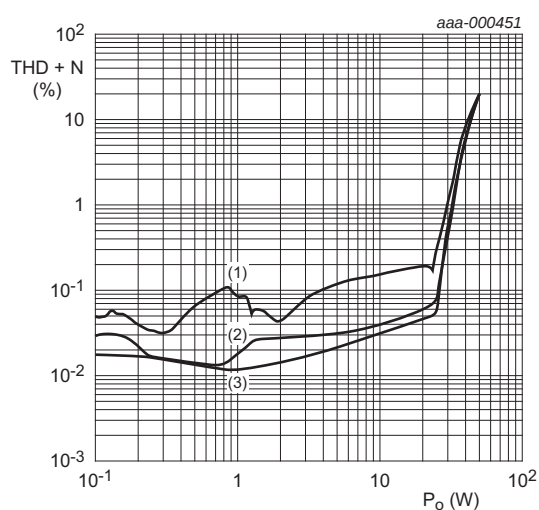
- Thermal resistance from junction to case ( $R_{th(j-c)} = 1 K/W$ )
- Thermal resistance from case to heat sink ( $R_{th(c-h)} = 0.5 K/W$  to  $1 K/W$  (depending on mounting))
- Thermal resistance from heat sink to ambient ( $R_{th(h-a)}$ ) would then be  $12 - (1 + 1) = 10 K/W$ .

If an audio signal has a crest factor of 10 (the ratio between peak power and average power = 10 dB) then  $T_j$  will be much lower.

Example 2:

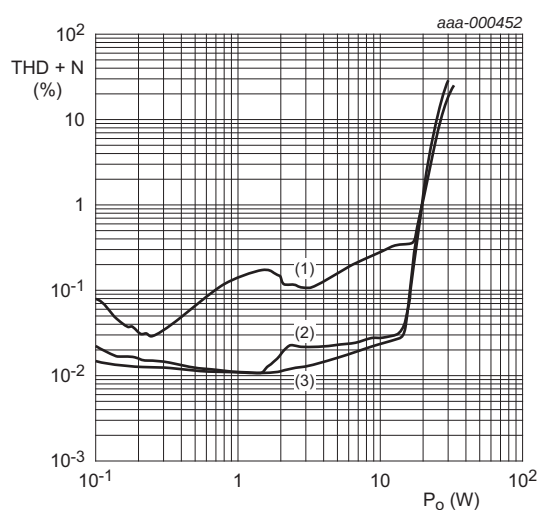
- $V_P = 14.4 \text{ V}$
- $P_O = 4 \times (25 \text{ W} / 10) = 4 \times 2.5 \text{ W}$  into  $4 \Omega$  (audio with crest factor of 10)
- $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
- $P_{\text{max}} = 4 \text{ W}$  (from [Figure 24](#))
- $R_{\text{th(j-a)}} = 12 \text{ K/W}$
- $T_{\text{j(max)}} = 25 \text{ }^\circ\text{C} + (4 \text{ W} \times 12 \text{ K/W}) = 73 \text{ }^\circ\text{C}$

## 14.5 Curves measured in reference design



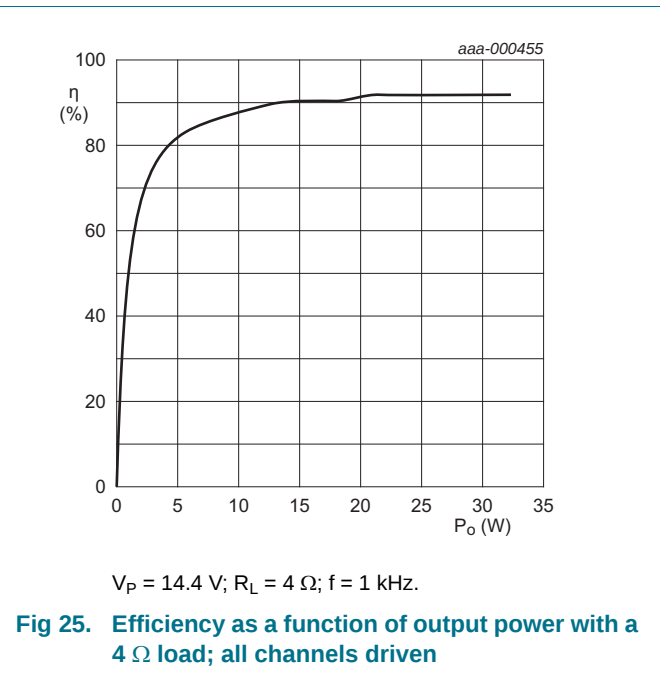
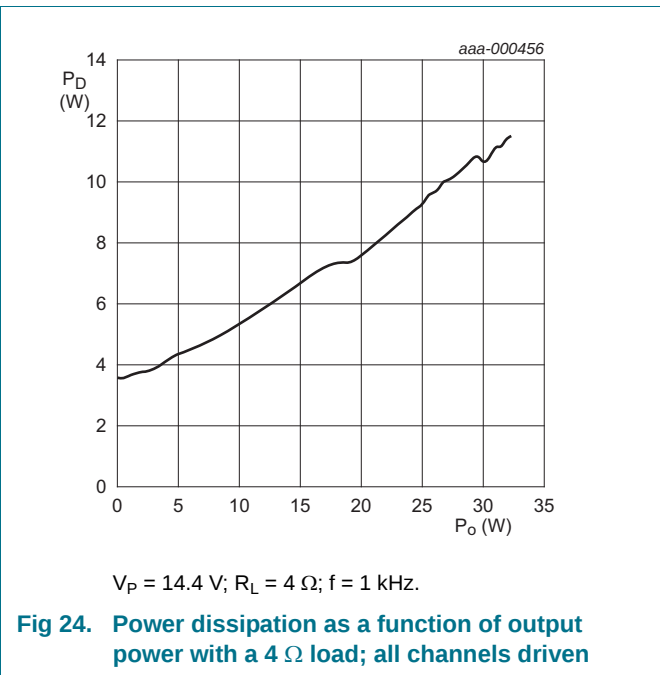
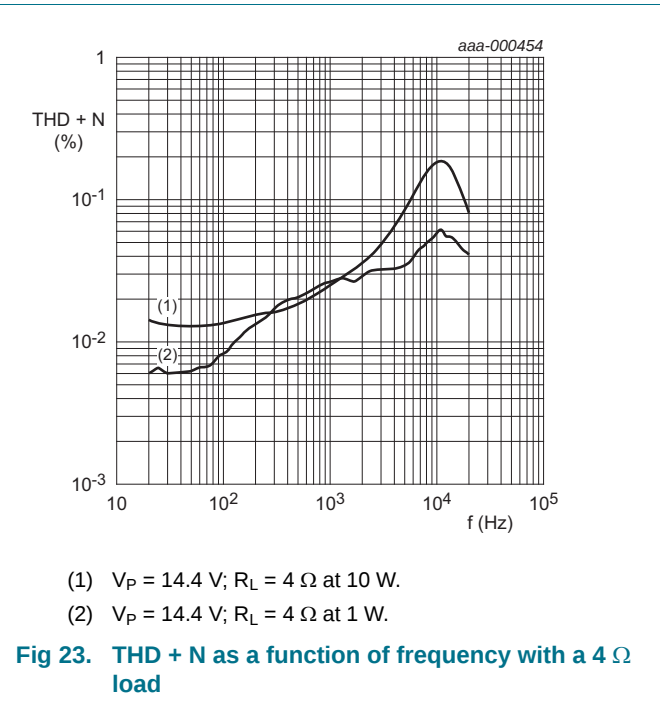
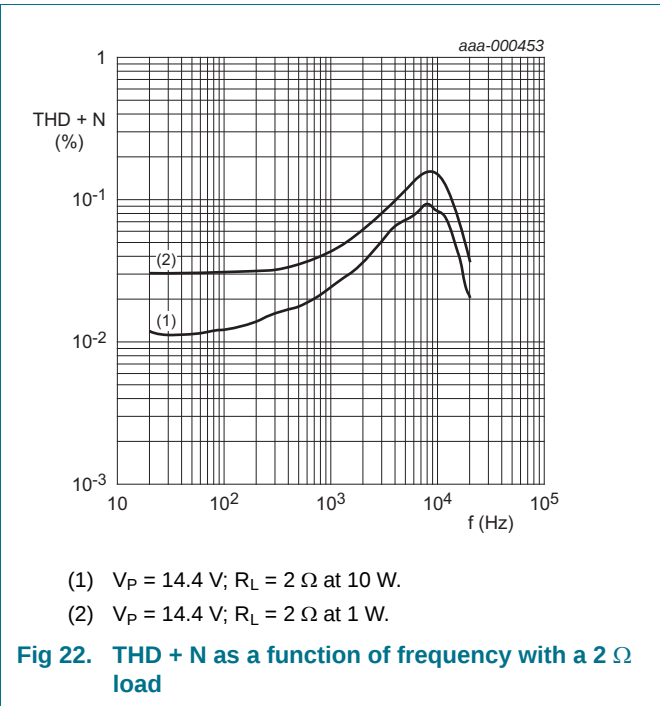
- (1)  $V_P = 14.4 \text{ V}$ ;  $R_L = 2 \Omega$  at 10 kHz.
- (2)  $V_P = 14.4 \text{ V}$ ;  $R_L = 2 \Omega$  at 1 kHz.
- (3)  $V_P = 14.4 \text{ V}$ ;  $R_L = 2 \Omega$  at 100 kHz.

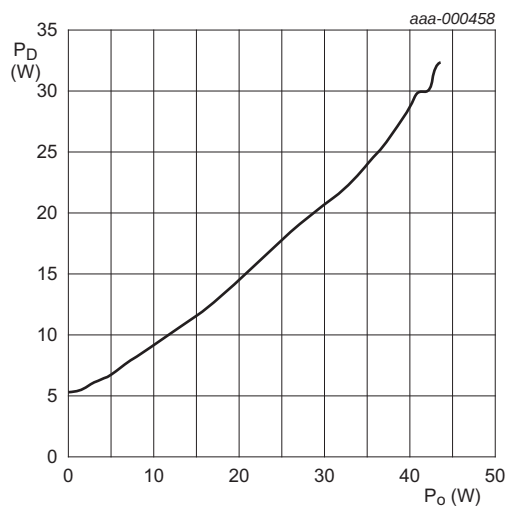
**Fig 20. THD + N as a function of output power with a 2 Ω load**



- (1)  $V_P = 14.4 \text{ V}$ ;  $R_L = 4 \Omega$  at 10 kHz.
- (2)  $V_P = 14.4 \text{ V}$ ;  $R_L = 4 \Omega$  at 1 kHz.
- (3)  $V_P = 14.4 \text{ V}$ ;  $R_L = 4 \Omega$  at 100 kHz.

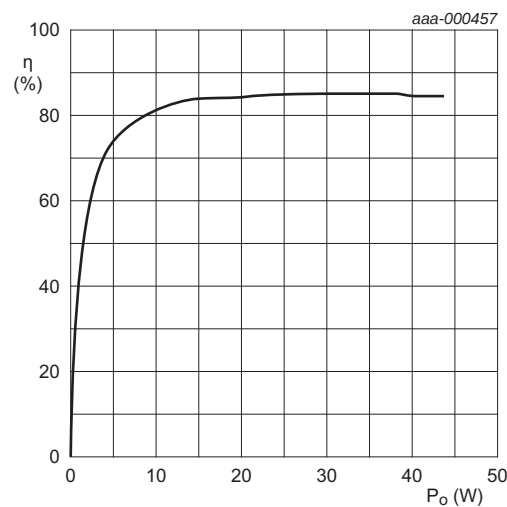
**Fig 21. THD + N as a function of output power with a 4 Ω load**





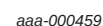
$V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ .

**Fig 26. Power dissipation as a function of output power with a 2  $\Omega$  load; all channels driven**



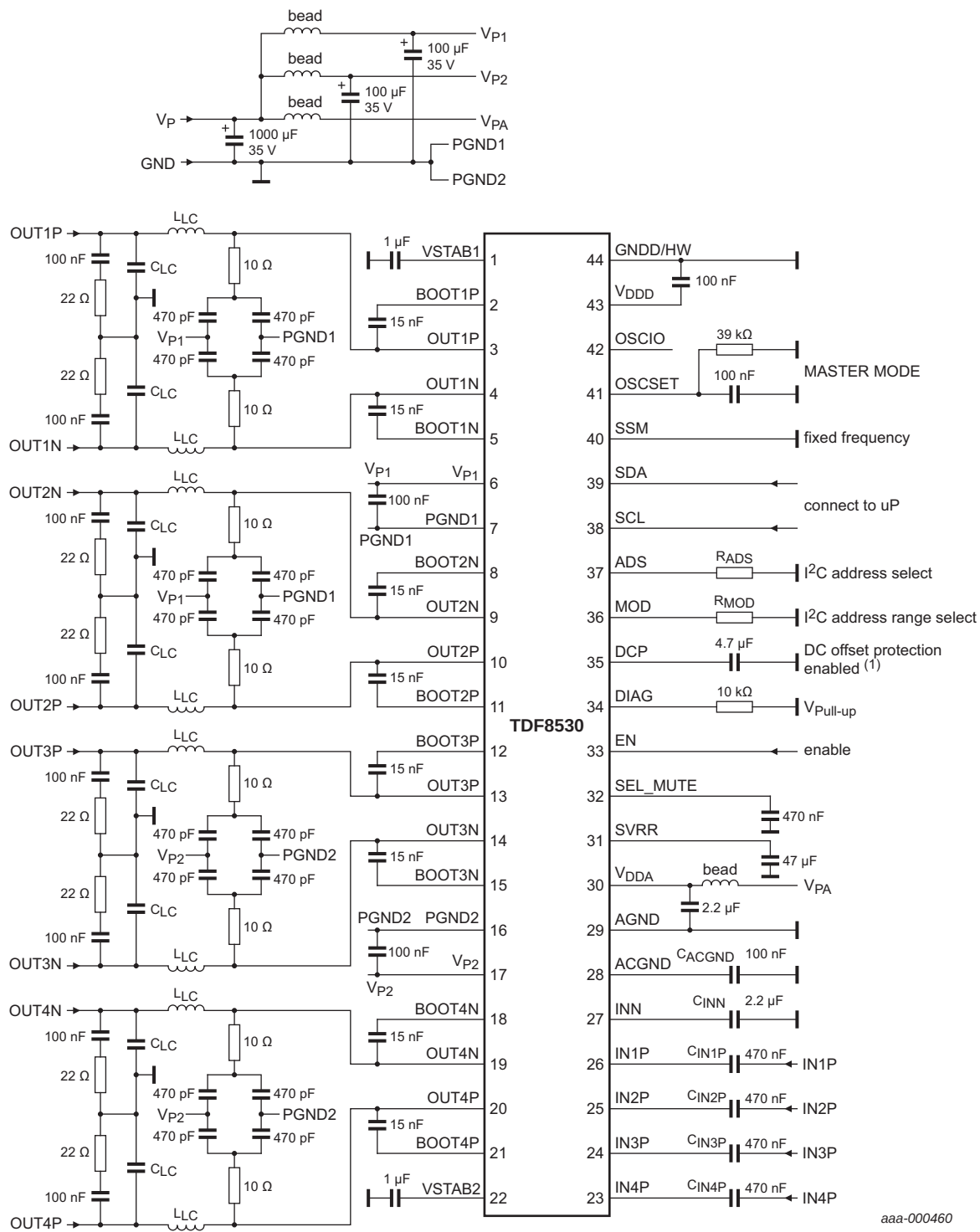
$V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ .

**Fig 27. Efficiency as a function of output power with a 2  $\Omega$  load; all channels driven**



(1) See [Section 8.3.5 on page 11](#) for detailed information on DC offset protection.

**Fig 28. Example application diagram 4 × BTL in non-I<sup>2</sup>C-bus mode**



15. Package outline

HSOP44: plastic, heatsink small outline package; 44 leads; low stand-off heightSOT1131-1

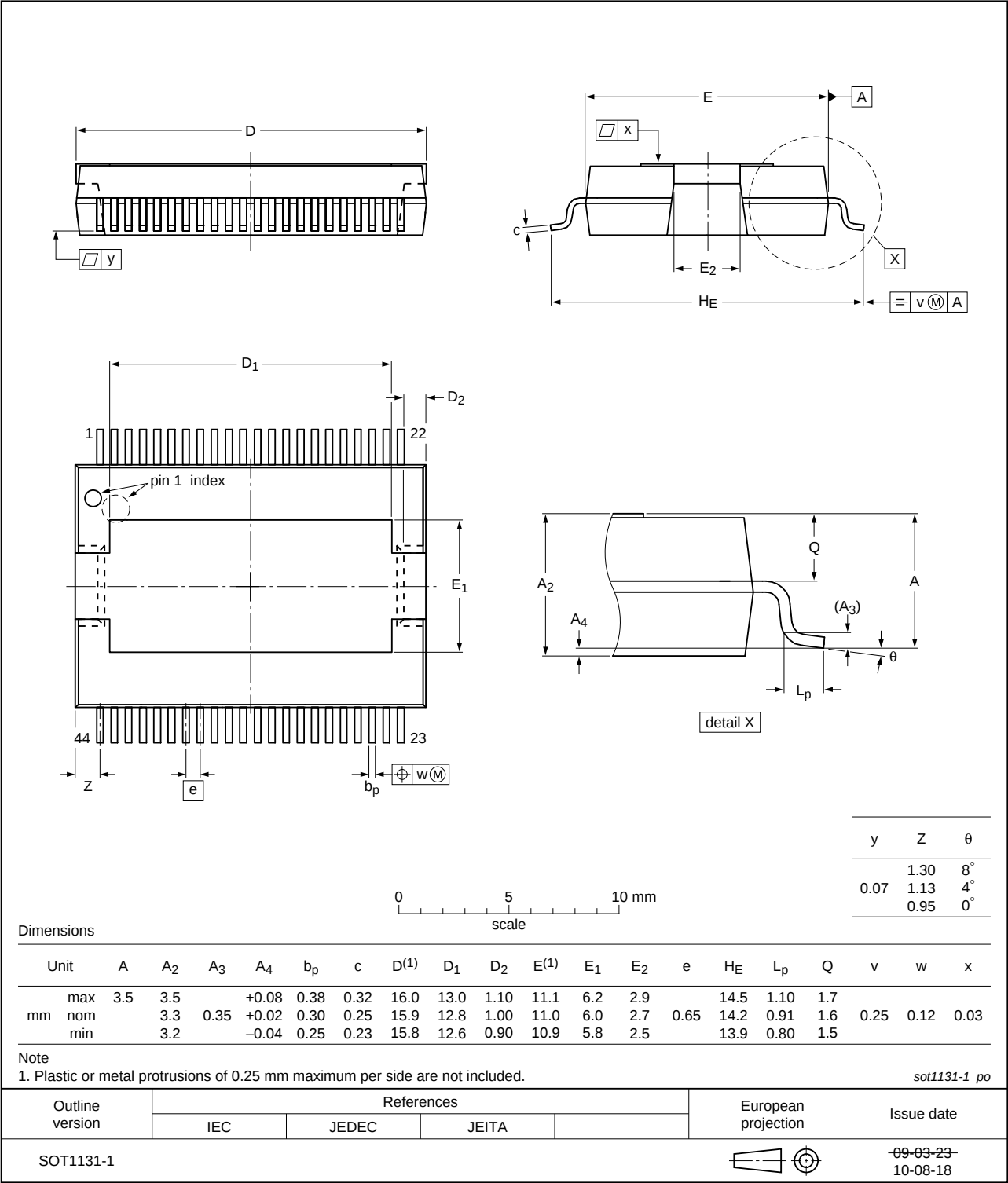


Fig 30. Package outline SOT1131-1 (HSOP44)

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 31](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

**Table 18. SnPb eutectic process (from J-STD-020C)**

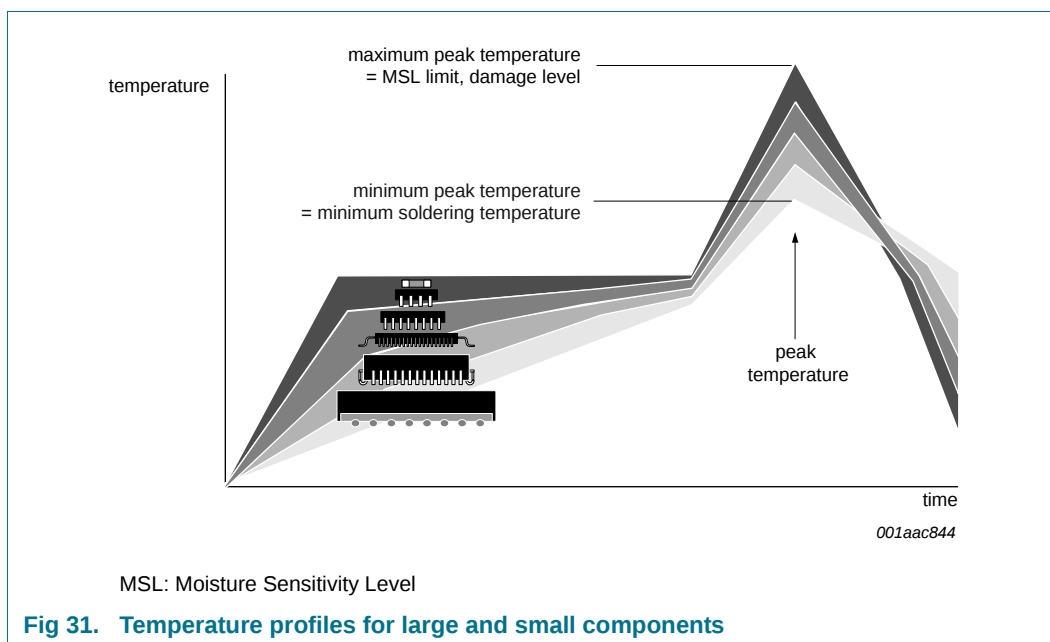
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 19. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 31](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 17. Abbreviations

**Table 20. Abbreviations**

| Abbreviation     | Description                                                         |
|------------------|---------------------------------------------------------------------|
| BCDMOS           | Bipolar Complementary and double Diffused Metal-Oxide Semiconductor |
| BTL              | Bridge-Tied Load                                                    |
| DCP              | DC offset Protection                                                |
| DMOST            | double Diffused Metal-Oxide Semiconductor Transistor                |
| EMI              | ElectroMagnetic Interference                                        |
| THD              | Total Harmonic Distortion                                           |
| I <sup>2</sup> C | Inter-Integrated Circuit                                            |
| LSB              | Least Significant Bit                                               |
| M $\mu$ p        | Master microprocessor                                               |
| MSB              | Most Significant Bit                                                |
| NDMOST           | N-type double Diffused Metal-Oxide Semiconductor Transistor         |
| OCP              | OverCurrent Protection                                              |
| OTP              | OverTemperature Protection                                          |
| OVP              | OverVoltage Protection                                              |
| PLL              | Phase-Locked Loop                                                   |
| POR              | Power-On Reset                                                      |
| PWM              | Pulse-Width Modulation                                              |
| SOI              | Silicon-On-Insulator                                                |

Table 20. Abbreviations ...continued

| Abbreviation | Description                 |
|--------------|-----------------------------|
| TFP          | Thermal Foldback Protection |
| UVP          | UnderVoltage Protection     |
| WP           | Window Protection           |

## 18. Revision history

Table 21. Revision history

| Document ID     | Release date                                                                                        | Data sheet status          | Change notice | Supersedes      |
|-----------------|-----------------------------------------------------------------------------------------------------|----------------------------|---------------|-----------------|
| TDF8530_SDS v.3 | 20111020                                                                                            | Product short data sheet   | -             | TDF8530_SDS v.2 |
| Modifications:  | • Data sheet status changed from Objective short data sheet to Product short data sheet.            |                            |               |                 |
| TDF8530_SDS v.2 | 20111014                                                                                            | Objective short data sheet | -             | TDF8530_SDS v.1 |
| Modifications:  | • Changed Table 15 on page 24: Changes to internal oscillator parameters and output frequency data. |                            |               |                 |
| TDF8530_SDS v.1 | 20111011                                                                                            | Objective short data sheet | -             | -               |

## 19. Legal information

### 19.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 20. Contact information

For more information, please visit: <http://www.nxp.com>

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