

1.2W Two Audio Inputs With Gain Control Power Amplifier with Standby Mode Active Low

- Operating from $V_{CC} = 2.8V$ to $5.5V$
- RAIL TO RAIL Input/Output
- 1.2W output power @ $V_{CC}=5V$, THD=1%, $F=1kHz$, with 8Ω load
- Ultra low consumption in standby mode (10nA)
- 53dB PSRR @ 217Hz from 2.8 to 5V
- Low distortion (0.5%)
- Gain settings pin: GS
- Unity gain stable
- Available in lead free flip-chip $9 \times 300\mu m$ bumps

Description

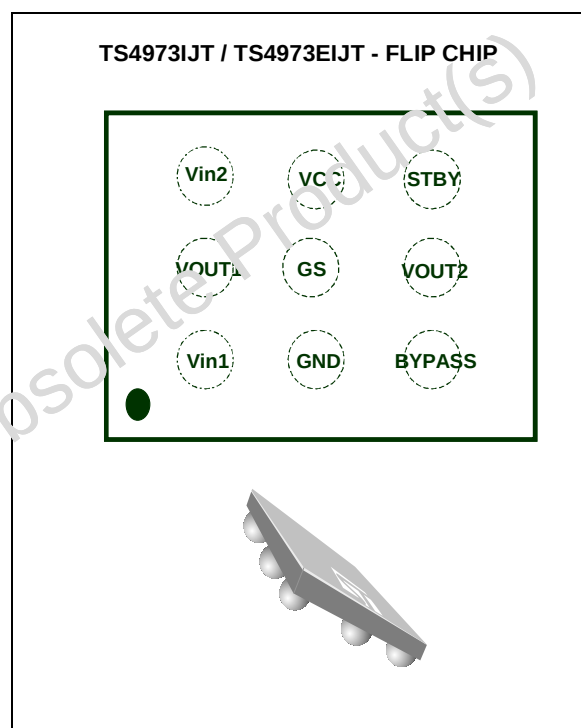
At 3.3v, the TS4973 is an Audio Power Amplifier capable of delivering 500mW of continuous RMS output power into a 8Ω bridged-tied loads with 1% THD+N, and 150mW of continuous average power into 32Ω . An external standby mode control reduces the supply current to less than 10nA. An internal over-temperature shutdown protection is provided.

The TS4973 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components. It has two inputs which can be used to switch the gain between 6dB (internal) or a user's adjustable gain setting with one external resistance.

Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop/Notebook computers
- Portable audio devices

Pin Connections (top view)



Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4973IJT	-40, +85°C	Flip-Chip9	Tape & Reel	A73
TS4973EIJT		Lead Free Flip-Chip		
TS4973EKIJT	-40, +85°C	FC + Back Coating	Tape & Reel	

1 Application Schematic

Figure 1: Typical application schematic

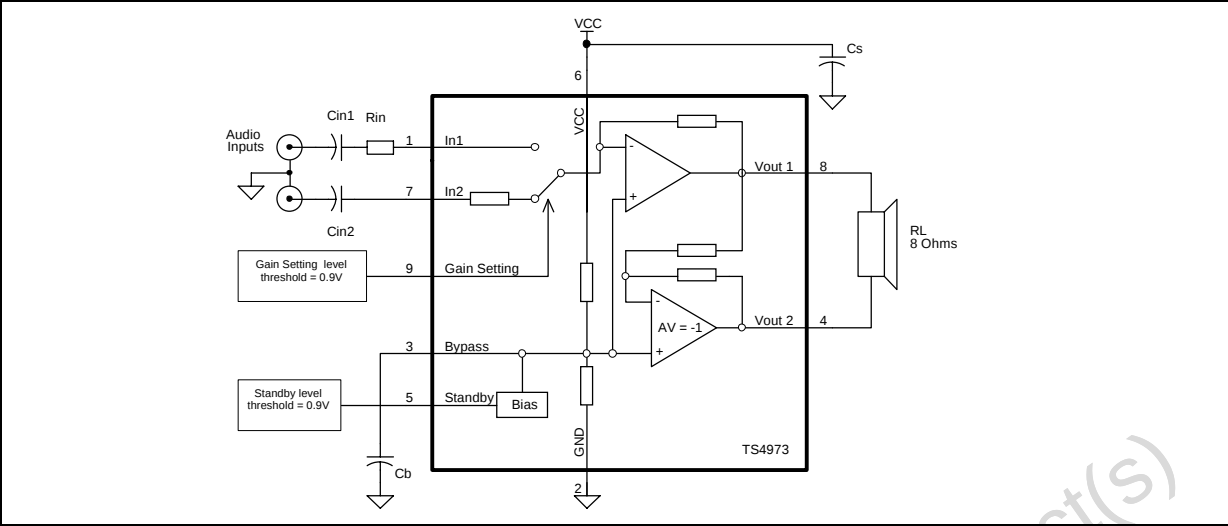


Table 1: Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage ¹	6	V
V _i	Input Voltage ²	G _{ND} to V _{CC}	V
T _{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
T _j	Maximum Junction Temperature	150	°C
R _{thja}	Thermal Resistance Junction to Ambient ³	200	°C/W
P _d	Power Dissipation	Internally Limited ⁴	
ESD	Human Body Model ⁵	1	kV
ESD	Machine Model (min. Value)	200	V
Latch-up	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C

- 1) All voltages values are measured with respect to the ground pin.
2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3) Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4) Exceeding the power derating curves during a long period, may involve abnormal operating condition.
5) Minimum value. Human body model, 100pF discharged through a 1.5kOhm resistor, into pin to Vcc device.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.8 to 5.5	V
VSTB	Standby Voltage Input: Device ON Device OFF	$1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
VGS	Gain Setting Voltage Input: External Gain (In1 Input) Internal Gain (In2 Input)	$1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
RL	Load Resistor	≥ 4	Ω
R _{thja}	Thermal Resistance Junction to Ambient ¹	90	°C/W

1) With Heat Sink Surface = 125mm²
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2 Electrical Characteristics

Table 3: Electrical Characteristics - $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{GS} = Gnd$, $V_{stdby} = Gnd$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	50	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$	0.85	1.2		W
BTL GAIN	GS = Low ($A_v = 2$) input signal $V_{in} = 100mV$ rms, No load	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise $P_O = 900mW$ rms, GS = Low ($A_v = 2$) $20Hz < F < 20kHz$, $R_L = 8\Omega$		0.5		%
PSRR	Power Supply Rejection Ratio ¹ $F = 217Hz$, $R_L = 8\Omega$, GS = Low ($A_v = 2$) Vripple = 200mVpp, Input Grounded, $C_{in} = 220nF$, $C_b = 1\mu F$		53		dB
PSRR	Power Supply Rejection Ratio ² $F = 217Hz$, $R_L = 8\Omega$, GS = Low ($A_v = 2$) Vripple = 200mVpp, Input Floating, $C_b = 1\mu F$		70		dB
Z_{in}	Input Impedance GS = Low ($A_v = 2$)	37.5	50	62.5	K Ω
R_{feed}	Internal Feedback Resistor	37.5	50	62.5	K Ω
V_N	Output Voltage Noise $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$ Unweighted, $V_{stdby} = Gnd$ A weighted, $V_{stdby} = Gnd$ Unweighted, GS = Low ($A_v = 2$) A weighted, GS = Low ($A_v = 2$) Unweighted, GS = High ($A_v = 10$) A weighted, GS = High ($A_v = 10$)		6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $F = 217Hz$

2) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $F = 217Hz$

Table 4: Electrical Characteristics - $V_{CC} = +3.3V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{GS} = Gnd$, $V_{stdby} = Gnd$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	50	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$	350	500		mW
BTL GAIN	$GS = Low$ ($A_v = 2$) input signal $V_{in} = 100mV$ rms, No load	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise $P_O = 380mW$ rms, $GS = Low$ ($A_v = 2$) $20Hz < F < 20kHz$, $R_L = 8\Omega$		0.5		%
PSRR	Power Supply Rejection Ratio ¹ $F = 217Hz$, $R_L = 8\Omega$, $GS = Low$ ($A_v = 2$) Vripple = 200mVpp, Input Grounded, $C_{in} = 220nF$, $C_b = 1\mu F$		53		dB
PSRR	Power Supply Rejection Ratio ² $F = 217Hz$, $R_L = 8\Omega$, $GS = Low$ ($A_v = 2$) Vripple = 200mVpp, Input Floating, $C_b = 1\mu F$		68		dB
Z_{in}	Input Impedance $GS = Low$ ($A_v = 2$)	37.5	50	62.5	K Ω
R_{feed}	Internal Feedback Resistor	37.5	50	62.5	K Ω
V_N	Output Voltage Noise $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$ Unweighted, $V_{stdby} = Gnd$ A weighted, $V_{stdby} = Gnd$ Unweighted, $GS = Low$ ($A_v = 2$) A weighted, $GS = Low$ ($A_v = 2$) Unweighted, $GS = High$ ($A_v = 10$) A weighted, $GS = High$ ($A_v = 10$)		6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $F = 217Hz$

2) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{CC} @ $F = 217Hz$

Table 5: Electrical characteristics - $V_{CC} = 2.8V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{GS} = Gnd$, $V_{stdby} = Gnd$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	50	mV
BTL GAIN	$GS = Low$ ($A_v = 2$) input signal $V_{in} = 100mV$ rms, No load	5.6	6	6.4	dB
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$	250	350		mW

Table 5: Electrical characteristics - $V_{CC} = 2.8V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
THD + N	Total Harmonic Distortion + Noise $P_o = 250mW$ rms, $G_S = Low$ ($A_v = 2$) $20Hz < F < 20kHz$, $R_L = 8\Omega$		0.5		%
PSRR	Power Supply Rejection Ratio ¹ $F = 217Hz$, $R_L = 8\Omega$, $G_S = Low$ ($A_v = 2$) Vripple = 200mVpp, Input Grounded, $C_{in} = 220nF$, $C_b = 1\mu F$		53		dB
PSRR	Power Supply Rejection Ratio ² $F = 217Hz$, $R_L = 8\Omega$, $G_S = Low$ ($A_v = 2$) Vripple = 200mVpp, Input Floating, $C_b = 1\mu F$		68		dB
Z_{in}	Input Impedance $G_S = Low$ ($A_v = 2$)	37.5	50	62.5	$K\Omega$
Rfeed	Internal Feedback Resistor	37.5	50	62.5	$K\Omega$
V_N	Output Voltage Noise $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$ Unweighted, $V_{stdby} = Gnd$ A weighted, $V_{stdby} = Gnd$ Unweighted, $G_S = Low$ ($A_v = 2$) A weighted, $G_S = Low$ ($A_v = 2$) Unweighted, $G_S = High$ ($A_v = 10$) A weighted, $G_S = High$ ($A_v = 10$)		6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{cc} @ $F = 217Hz$

2) Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is an added sinus signal to V_{cc} @ $F = 217Hz$

Table 6: Application Components Information

Components	Functional Description
R_{in}	Inverting input resistor which sets the closed loop gain (when $G_S = high$) in conjunction with the internal feedback resistor Rfeed. This resistor also forms a high pass filter with C_{in1} $F_c = 1 / (2 \times \pi \times R_{in} \times C_{in1})$
C_{in1}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In1
C_{in2}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In2. This capacitor also forms a high pass filter with Z_{in} (internal input impedance when $G_S = Low$) $F_c = 1 / (2 \times \pi \times Z_{in} \times C_{in2})$
C_s	Supply Bypass capacitor which provides power supply filtering (Recommended value = $1\mu F$)
C_b	Bypass pin capacitor which provides half supply filtering (Recommended value = $1\mu F$)
A_v	Closed loop gain in BTL configuration When $G_S = Low$, $A_v = 2$ or 6dB When $G_S = high$, $A_v = 2 \times (R_{feed} / R_{in})$. Rfeed value see Electrical Characteristics.

Remarks:

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor $C_s = 1\mu F$.
2. The standby response time is about $1\mu s$.

Figure 2: Power supply rejection ratio (psrr) vs power supply

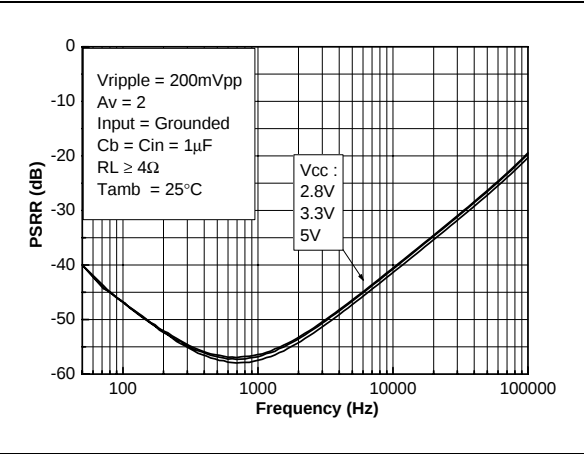


Figure 5: Power supply rejection ratio (PSRR) vs bypass capacitor

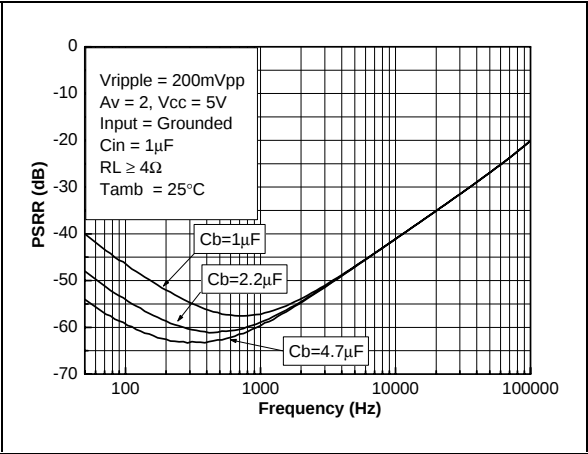


Figure 3: Power supply rejection ratio (PSRR) vs power supply

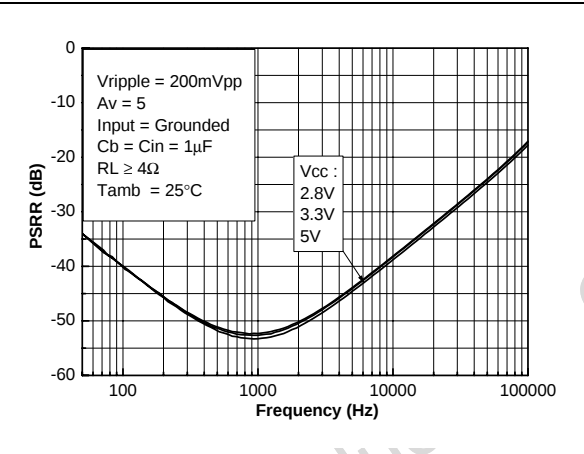


Figure 6: Power supply rejection ratio (PSRR) vs bypass capacitor

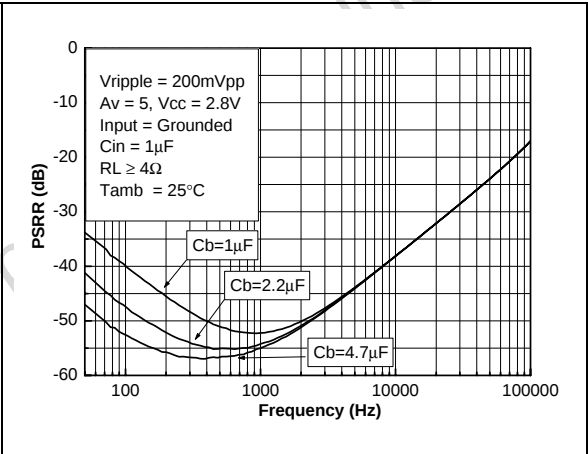


Figure 4: Power supply rejection ratio (PSRR) vs power supply

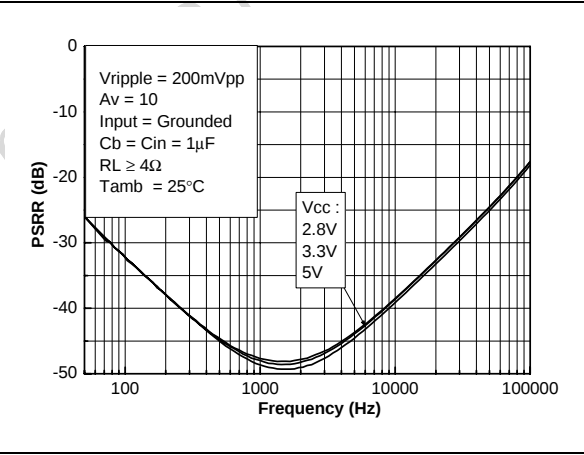


Figure 7: Power supply rejection ratio (PSRR) vs bypass capacitor

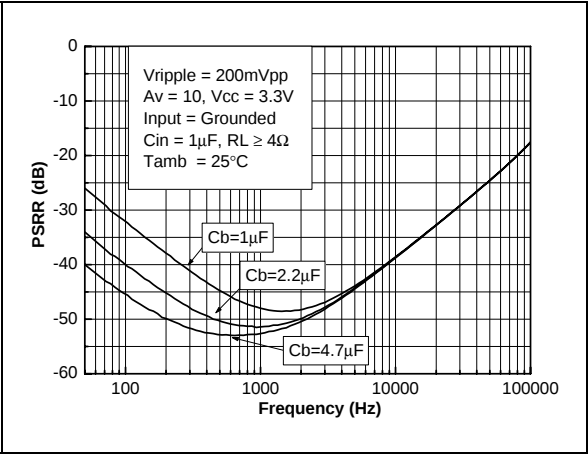


Figure 8: Power supply rejection ratio (PSRR)

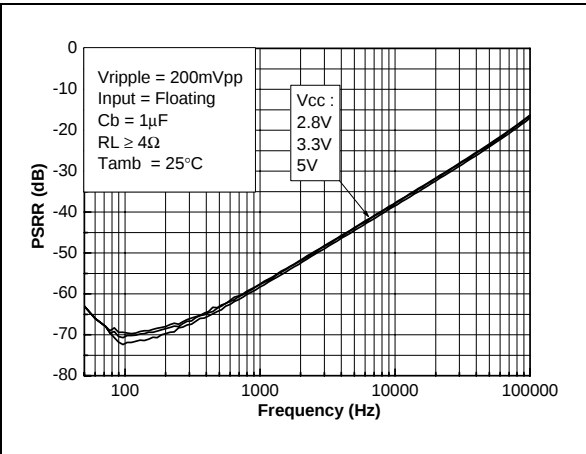


Figure 9: Crosstalk between inputs vs frequency

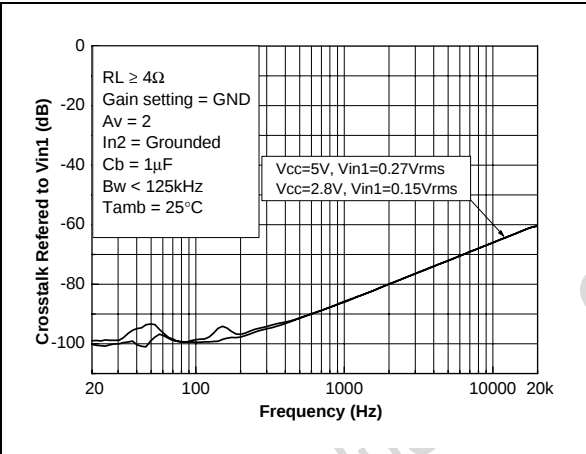


Figure 10: Crosstalk between inputs vs frequency

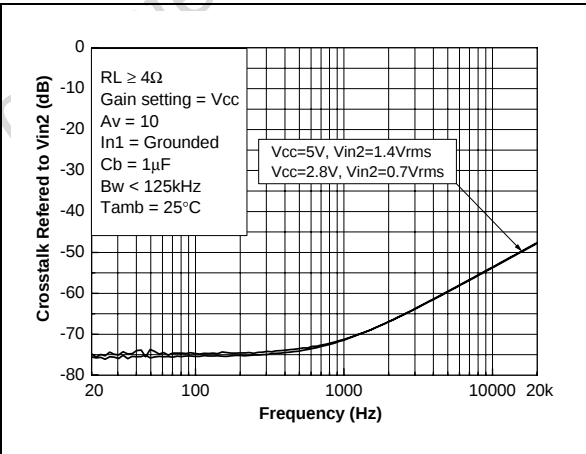


Figure 11: Signal to noise ratio vs power supply with a weighted filter

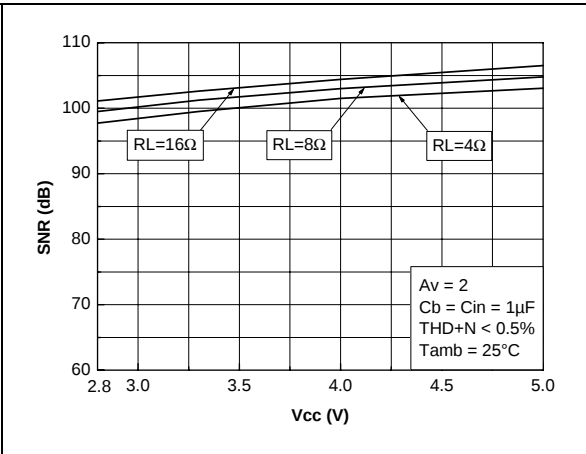


Figure 12: Signal to noise ratio vs power supply with a weighted filter

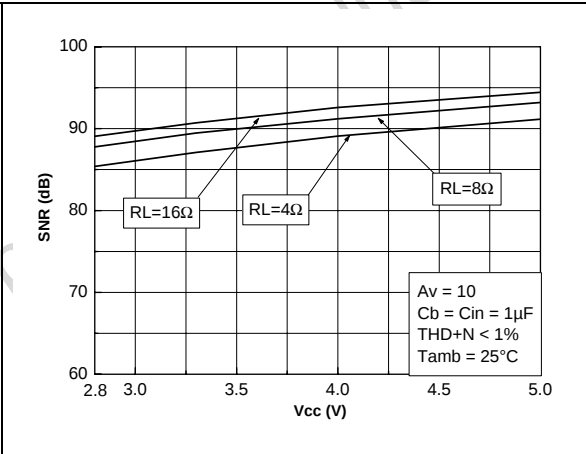


Figure 13: Signal to noise ratio vs power supply with unweighted filter (20Hz to 20kHz)

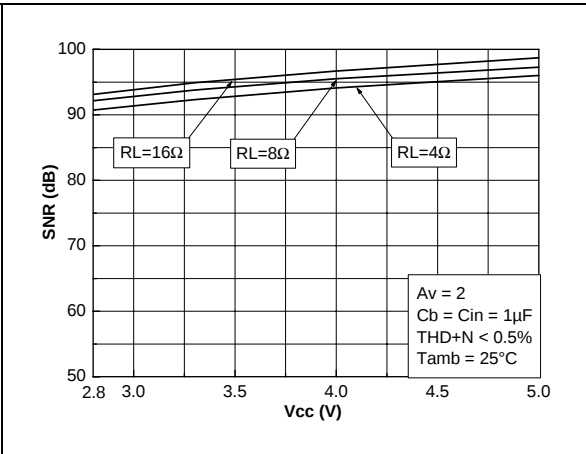


Figure 14: Signal to noise ratio vs power supply with unweighted filter (20Hz to 20kHz)

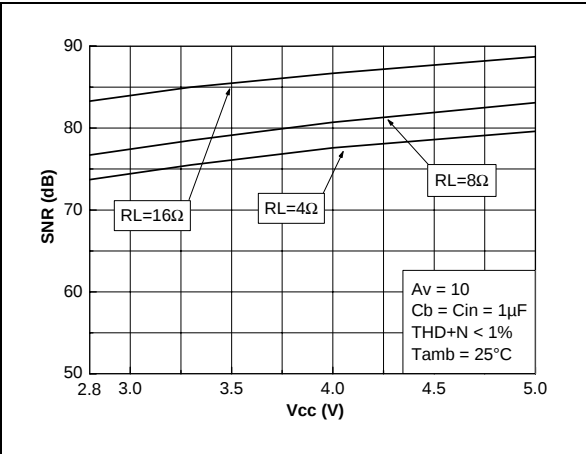


Figure 15: Output power vs power supply voltage

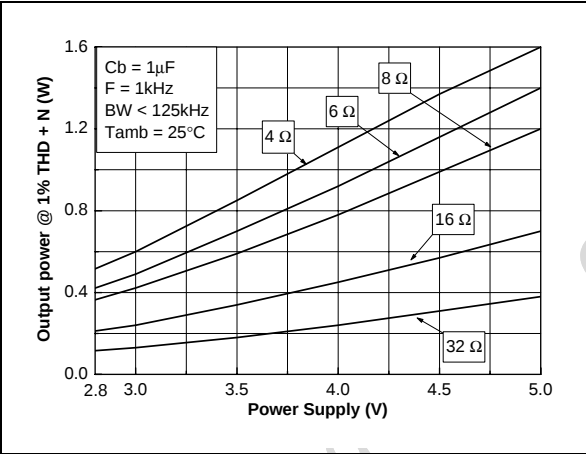


Figure 16: Output power vs power supply voltage

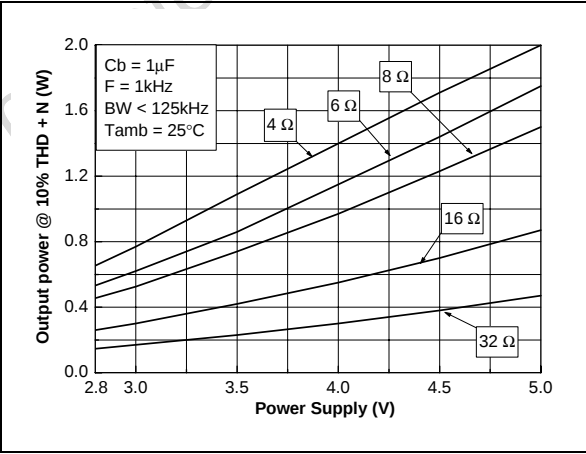


Figure 17: Power dissipation vs output power

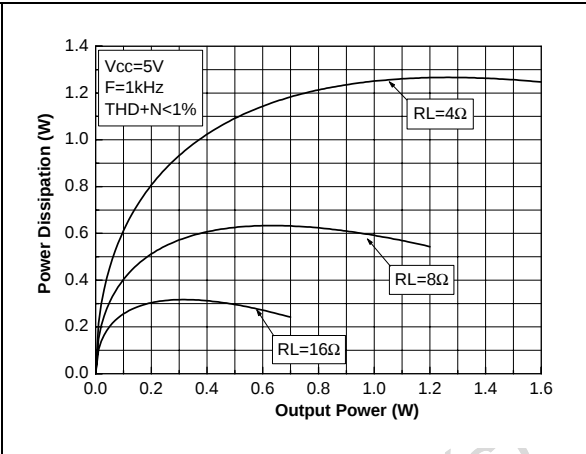


Figure 18: Power dissipation vs output power

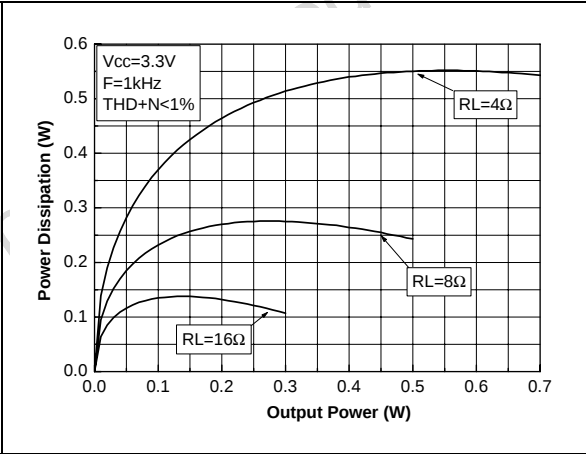


Figure 19: Power dissipation vs output power

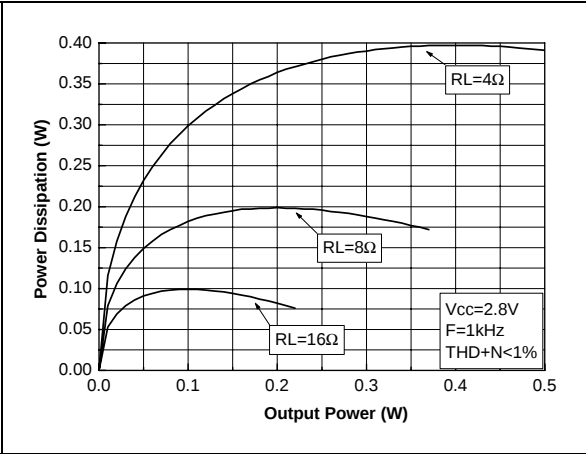


Figure 20: Power derating curves

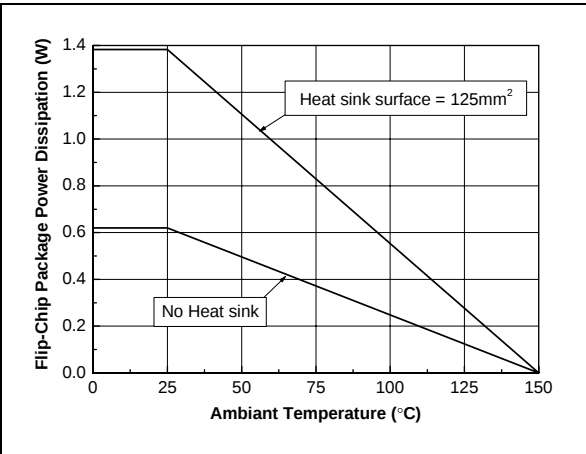


Figure 23: Current consumption vs power supply voltage

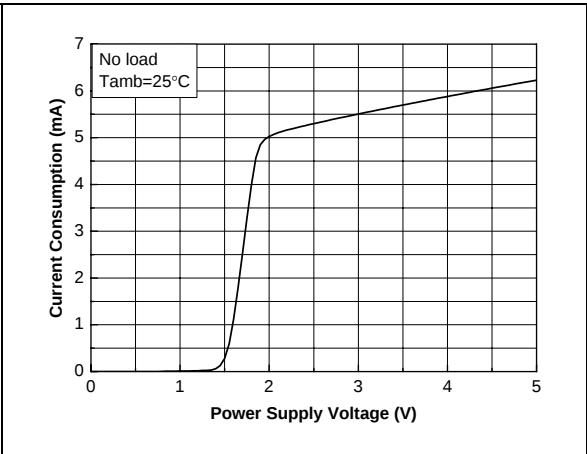


Figure 21: Clipping voltage vs power supply voltage and load resistor

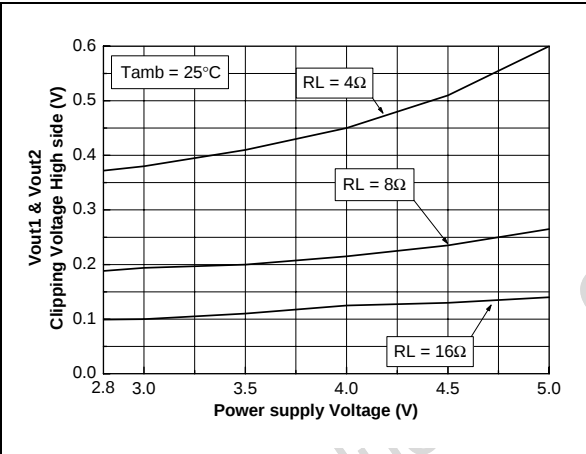


Figure 24: Current consumption vs standby voltage @ Vcc = 5V

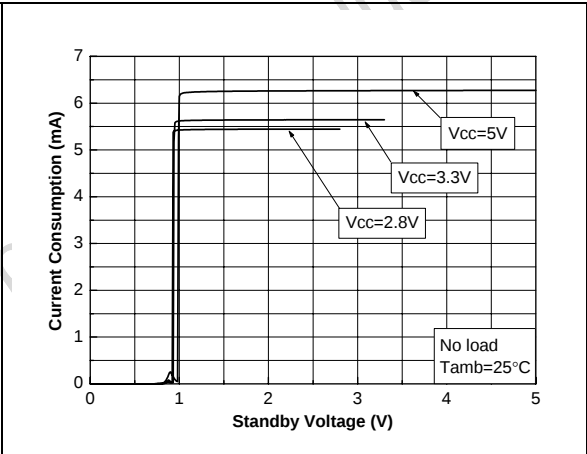


Figure 22: Clipping voltage vs power supply voltage and load resistor

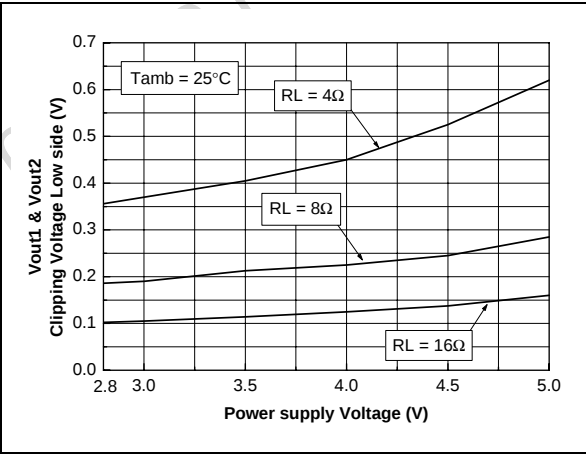


Figure 25: THD + N vs output power

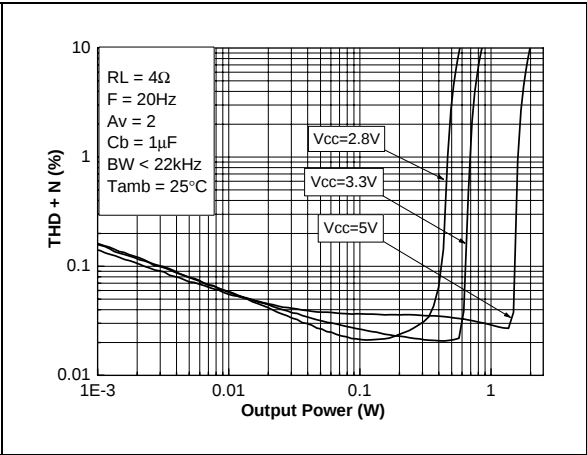


Figure 26: THD + N vs output power

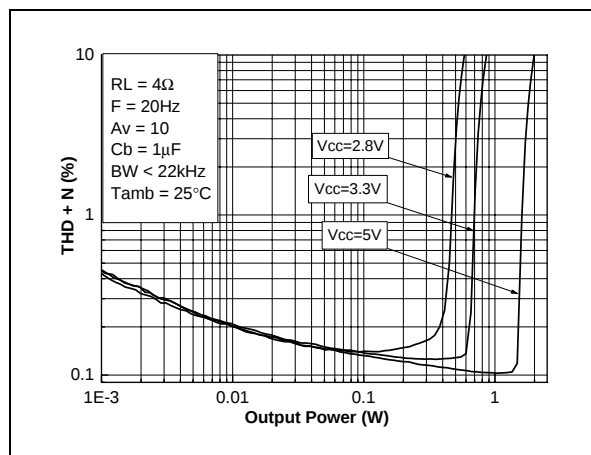


Figure 29: THD + N vs Output power

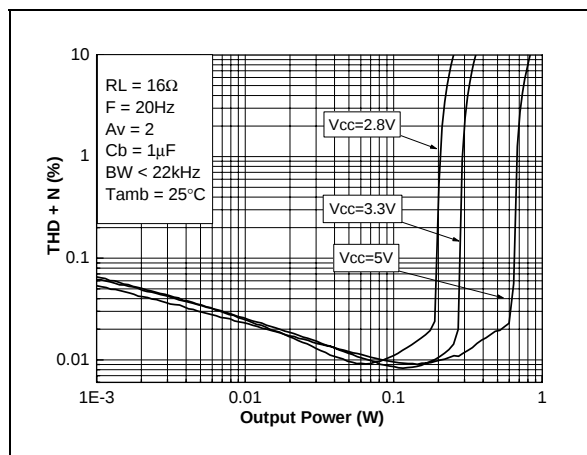


Figure 27: THD + N vs output power

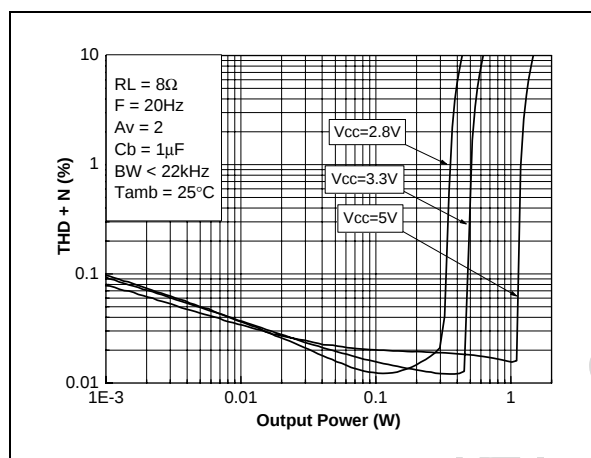


Figure 30: THD + N vs output power

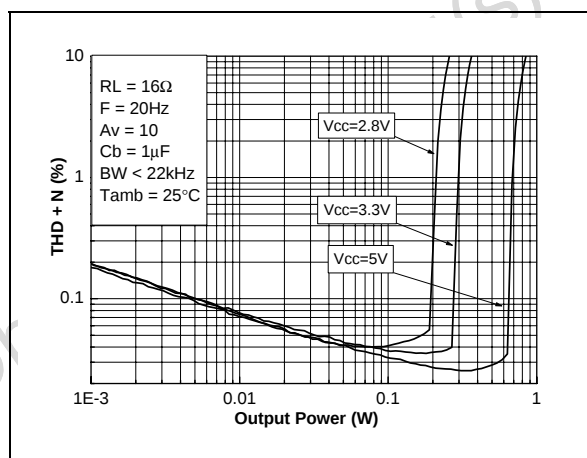


Figure 28: THD + N vs output power

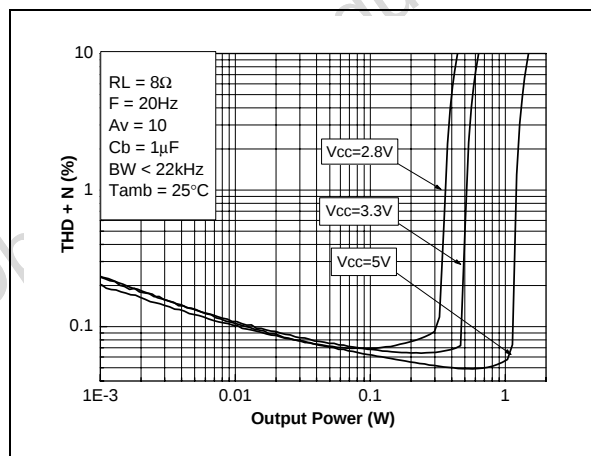


Figure 31: THD + N vs output power

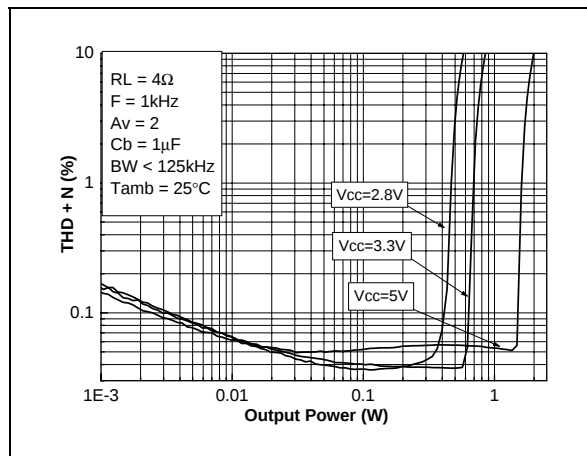


Figure 32: THD + N vs output power

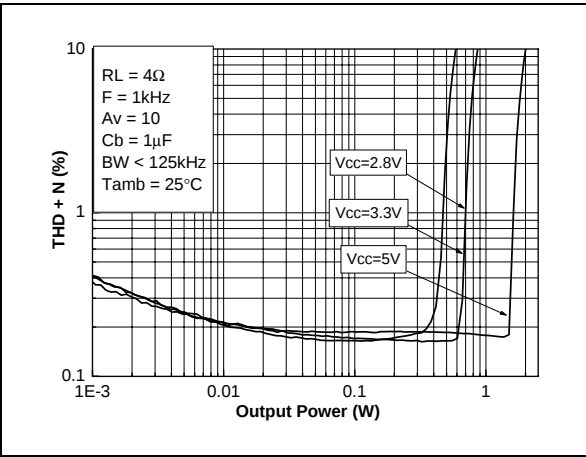


Figure 35: THD + N vs output power

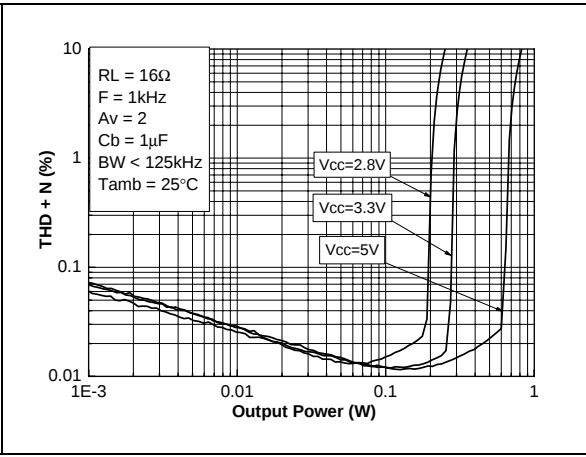


Figure 33: THD + N vs output power

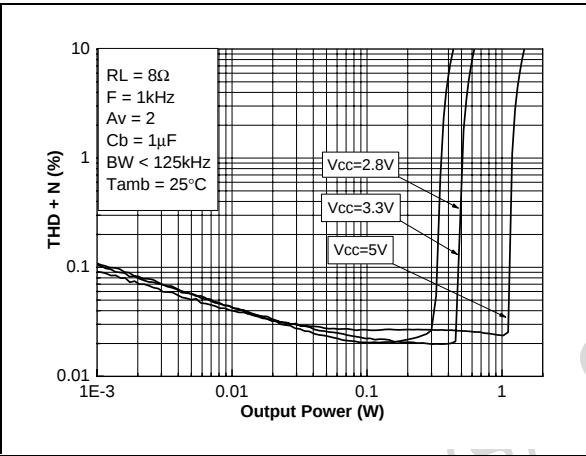


Figure 36: THD + N vs output power

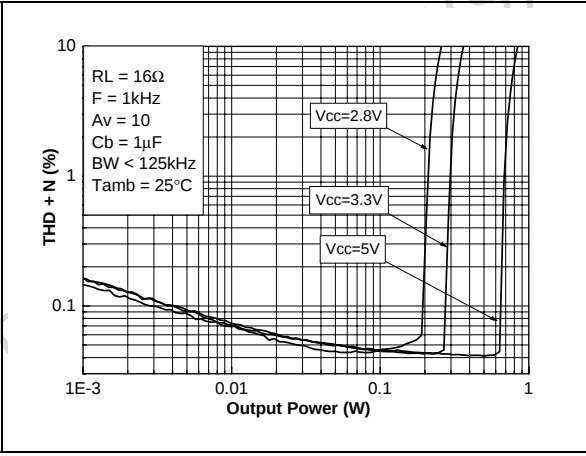


Figure 34: THD + N vs output power

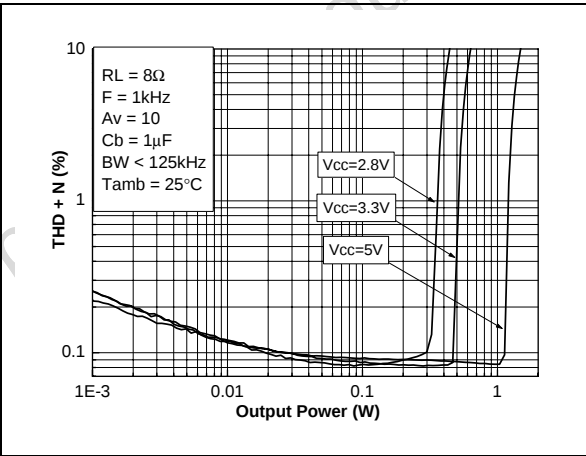


Figure 37: THD + N vs output power

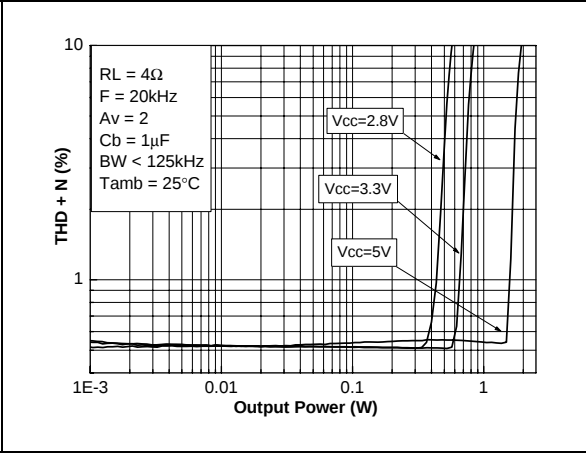


Figure 38: THD + N vs output power

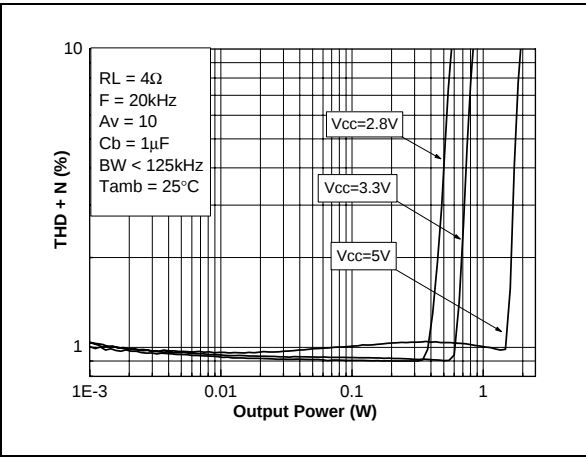


Figure 41: THD + N vs output power

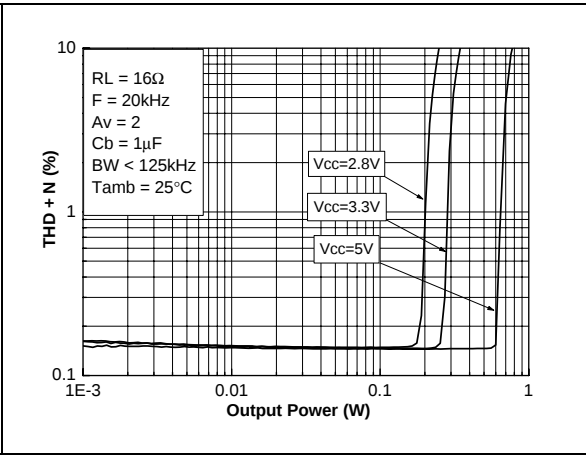


Figure 39: THD + N vs output power

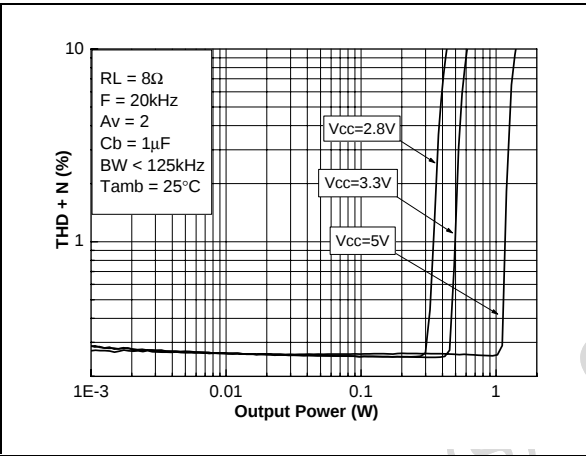


Figure 42: THD + N vs output power

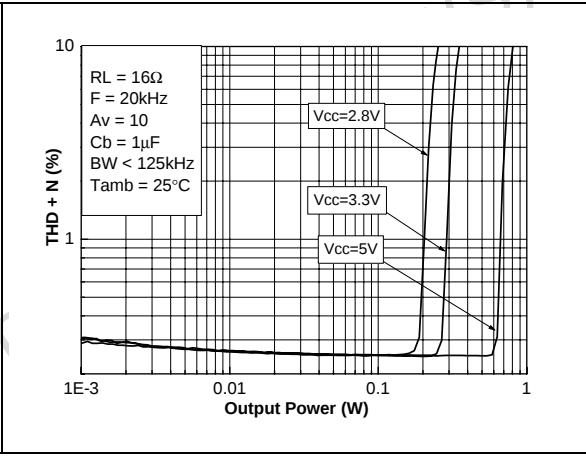


Figure 40: THD + N vs output power

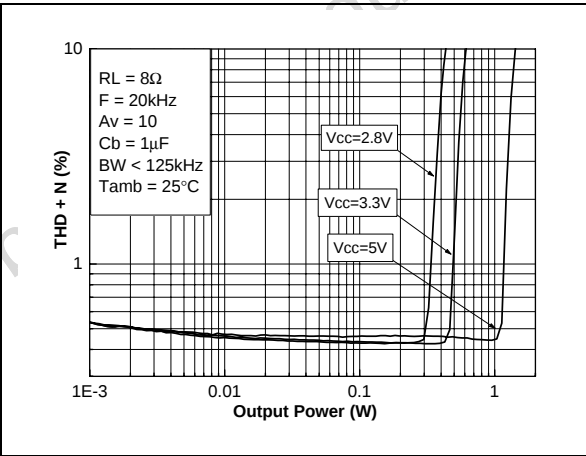


Figure 43: THD + N vs frequency

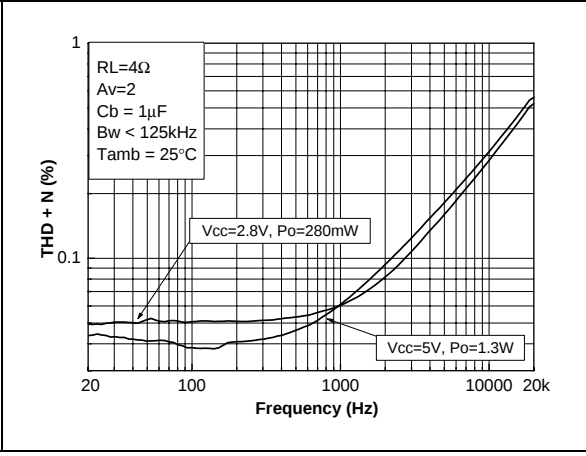


Figure 44: THD + N vs frequency

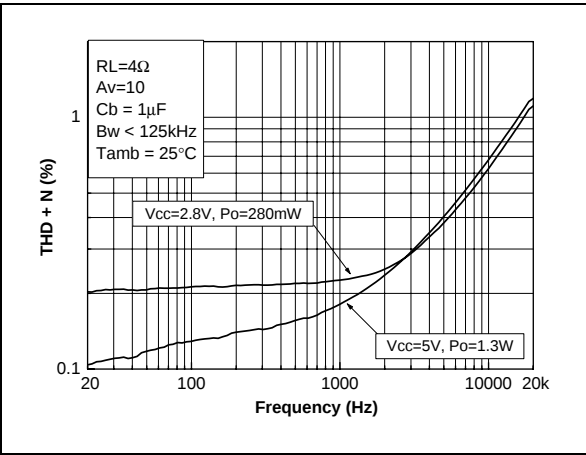


Figure 47: THD + N vs frequency

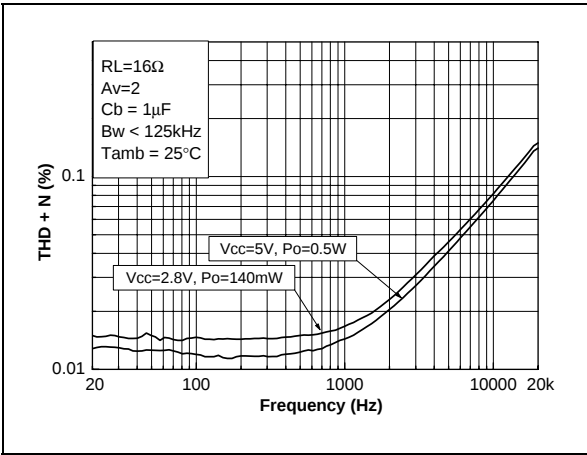


Figure 45: THD + N vs frequency

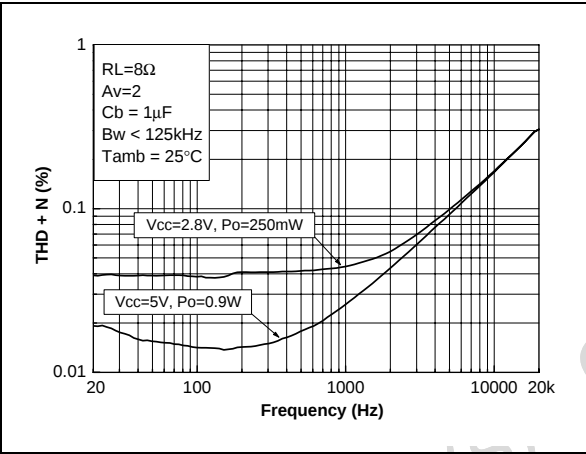


Figure 48: THD + N vs frequency

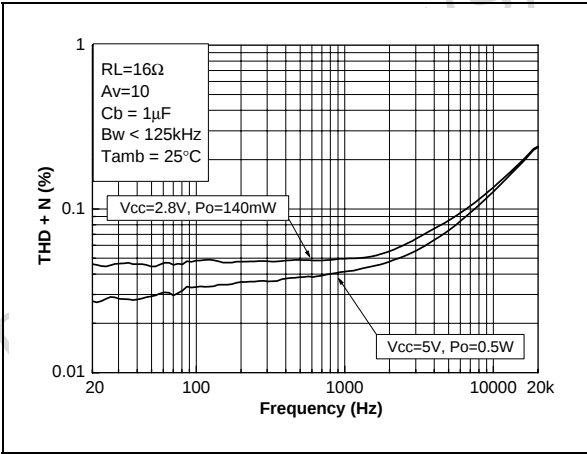
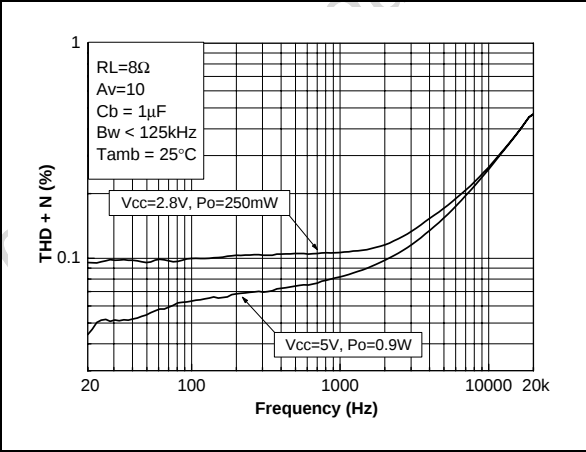


Figure 46: THD + N vs frequency



3 Application Information

3.1 BTL Configuration Principle

The TS4973 are monolithic power amplifiers with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = $V_{out1} = V_{out}$ (V)

Single ended output 2 = $V_{out2} = -V_{out}$ (V)

And $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2 V_{out_{RMS}})^2}{R_L} \text{ (W)}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

3.2 Gain In Typical Application Schematic (cf. page1 of TS4973 datasheet)

Depending on gain select (G_s) voltage, the output is driven by $In1$ when $G_s \geq 1.5V$ and by $In2$ when $G_s \leq 0.4V$. In the flat region (no C_{IN} effect), the gain is expressed by this general equation:

$$A_v = \frac{V_{out1} - V_{out2}}{V_{in(1,2)}}$$

If $G_s \leq 0.4V$: The typical value is

$$A_v = \frac{V_{out1} - V_{out2}}{V_{in2}} = 2$$

with a range of:

$$1.9 \leq A_v = \frac{V_{out1} - V_{out2}}{V_{in2}} \leq 2.1$$

If $G_s \geq 1.5V$: The typical value is (R_{in} in $k\Omega$)

$$A_v = \frac{V_{out1} - V_{out2}}{V_{in1}} = \frac{100}{R_{in}}$$

with a range of :

$$\frac{75}{R_{in}} \leq A_v = \frac{V_{out1} - V_{out2}}{V_{in1}} \leq \frac{125}{R_{in}}$$

Remark: V_{out2} is in phase with V_{in} and V_{out1} is phased 180° with V_{in} . This means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

3.3 Low frequency response

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} (or the input impedance

Z_{in} when $G_s \leq 0.4V$) a high-pass filter with a -3dB cut off frequency.

If $G_s \leq 0.4V$: The typical value is (C_{in2} in nF)

$$F_{CL} = \frac{4823}{C_{in2}} \text{ (Hz)}$$

with a range of

$$\frac{6366}{C_{in2}} \leq F_{CL} \text{ (Hz)} \leq \frac{3789}{C_{in2}}$$

If $G_s \geq 1.5V$: The value is (R_{in} in $k\Omega$, C_{in1} in nF):

$$F_{CL} \leq \frac{159000}{R_{in} C_{in1}} \text{ (Hz)}$$

3.4 Power dissipation and efficiency

Hypothesis:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} \text{ (A)}$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Then, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{cc} I_{CC_{AVG}} \text{ (W)}$$

Then, the **power dissipated by the amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \text{ (W)}$$

$$P_{diss} = \frac{2\sqrt{2} V_{cc}}{\pi \sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} \text{ (W)}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss_{max}} = \frac{2 V_{cc}^2}{\pi^2 R_L} \text{ (W)}$$

Remark: This maximum value is only dependent upon power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4 V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so

$$\frac{\pi}{4} = 78.5\%$$

3.5 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4973. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B .

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With 1μF, you can expect similar THD+N performances to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1μF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than 1μF, those disturbances on the power supply rail are more filtered.

C_B has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_B is lower than 1μF, THD+N increases at lower frequencies and PSRR worsens.

If C_B is higher than 1μF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN} , the higher the PSRR.

3.6 Wake-up Time: T_{WU}

T_{WU} is directly linked to the size of the bypass capacitor C_B . The slower the speed is, the higher C_B is. When power supply is apply or standby command is released, output amplifier are immediately un function. At this moment, the charge of C_B begins and the internal bias voltage, raise at the speed controlled by C_B . So, we define the T_{WU} when the internal bias voltage reaches

80% of the final value. With this condition, we can write with C_B in μF:

$$T_{WU} \approx 0.42 C_B \text{ (s)}$$

3.7 Shutdown time

When the standby command is set, the time to put the two output stage in high impedance and the internal circuitry in shutdown mode is a few microseconds.

3.8 Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_B .

Size of C_{in} is due to the lower cut-off frequency and PSRR value requested. Size of C_B is due to THD+N and PSRR requested always in lower frequency.

Moreover, C_B determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of C_B is directly proportional to the internal generator resistance 350kΩ.

Then, the charge time constant for C_B is $\tau_b = 350k\Omega \times C_B$ (s)

As C_B is directly connected to the non-inverting input and if we want to minimize, in amplitude and duration, the output spike on V_{out1} , C_{in} must be charged faster than C_B . The charge time constant of C_{in} is:

If $G_S \leq 0.4V$: $\tau_{in} = 40000 \times C_{in2}$ (s)

If $G_S \geq 1.5V$: $\tau_{in} = R_{in} \times C_{in1}$ (s)

Thus we have the relation

$$\tau_{in} \ll \tau_b \text{ (s)}$$

The respect of this relation permits to minimize the pop and click noise.

Remark: Minimize C_{in} and C_B has a benefit on pop and click phenomena but also on cost and size of the application.

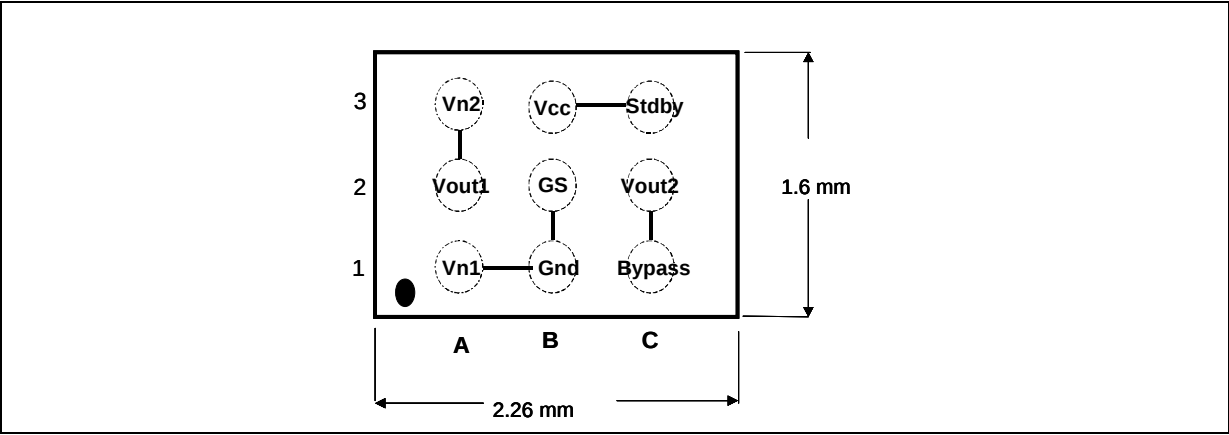
3.9 Biasing of C_{in1} and C_{in2}

An internal bias circuitry allow to keep C_{in1} and C_{in2} always bias with the right DC value.

This circuitry eliminates all "possible clicks" when gain select pin is used to switch for a gain to another.

4 Mechanical Data

Figure 49: Daisy chain mechanical data (top view: all drawings dimensions are in millimeters)



Remarks:

Daisy chain sample is featuring pins connection two by two. The schematic above is illustrating the way connecting pins each other. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting an Ohmmeter between pin 8 and pin 1, the soldering process continuity can be tested.

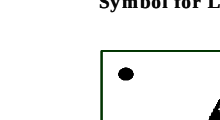
Table 7: Order Codes

Part Number	Temperature Range	Package	Marking
		J	
TSDC05IJT	-40, +85°C	•	DC5

Technical drawing of a PCB layout for a 3x3 grid of components. The drawing shows a 3x3 grid of circular pads. The top row has a horizontal dimension of 500µm between the first two pads and 500µm between the second and third pads. The vertical dimension between the first and second rows is 500µm, and between the second and third rows is 500µm. The top-left pad has a diameter of $\Phi=250\mu\text{m}$. The top-middle pad has a diameter of $\Phi=400\mu\text{m}$. The top-right pad has a diameter of 340µm min. The top-right pad is connected to a horizontal bar with a width of 75µm min. to 100µm max. and a length of 150µm min. The bottom-left pad is labeled "Non Solder mask opening". The bottom-middle pad is labeled "Pad in Cu 18µm with Flash NiAu (2-6µm, 0.2µm max)".

	A	B	C
3	Vin2	VCC	STBY
2	VOUT1	GS	VOUT2
1	Vin1	GND	BYPASS

Symbol for Lead Free Version



- Logo: **ST**
- Part Number: **A73**
- Three digit Date Code: **YWW**
- The Dot is for marking pin **A1**
- **E** symbol for Lead Free only

5 Package Mechanical Data

Figure 53: Flip-Chip - 9 bumps

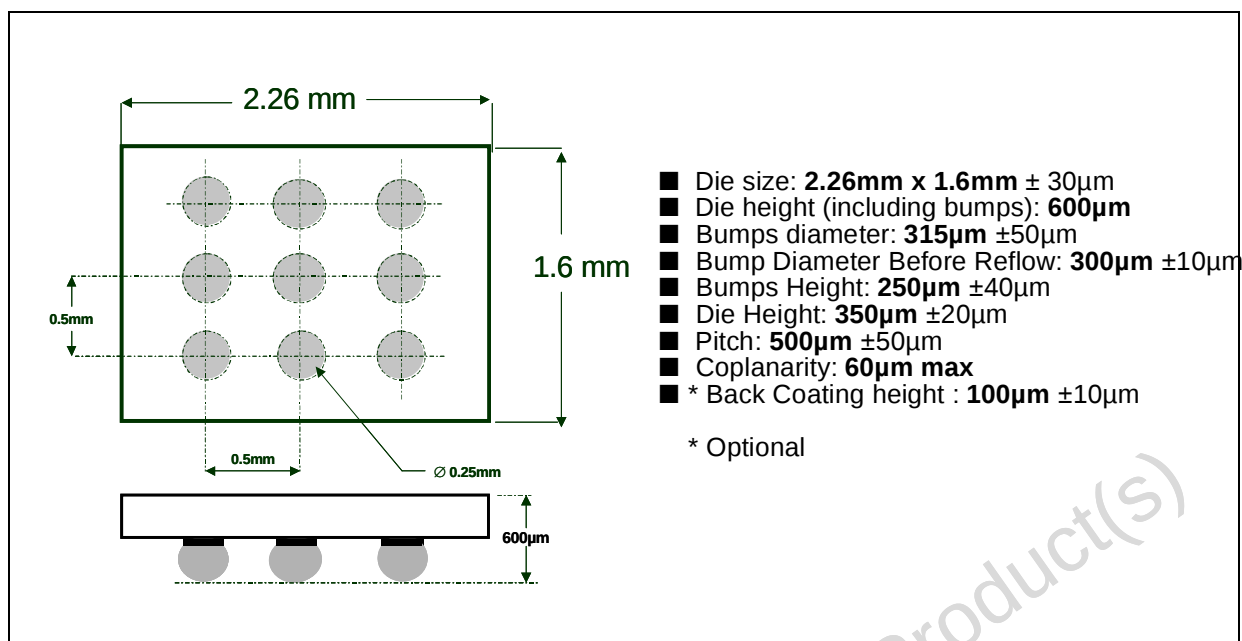
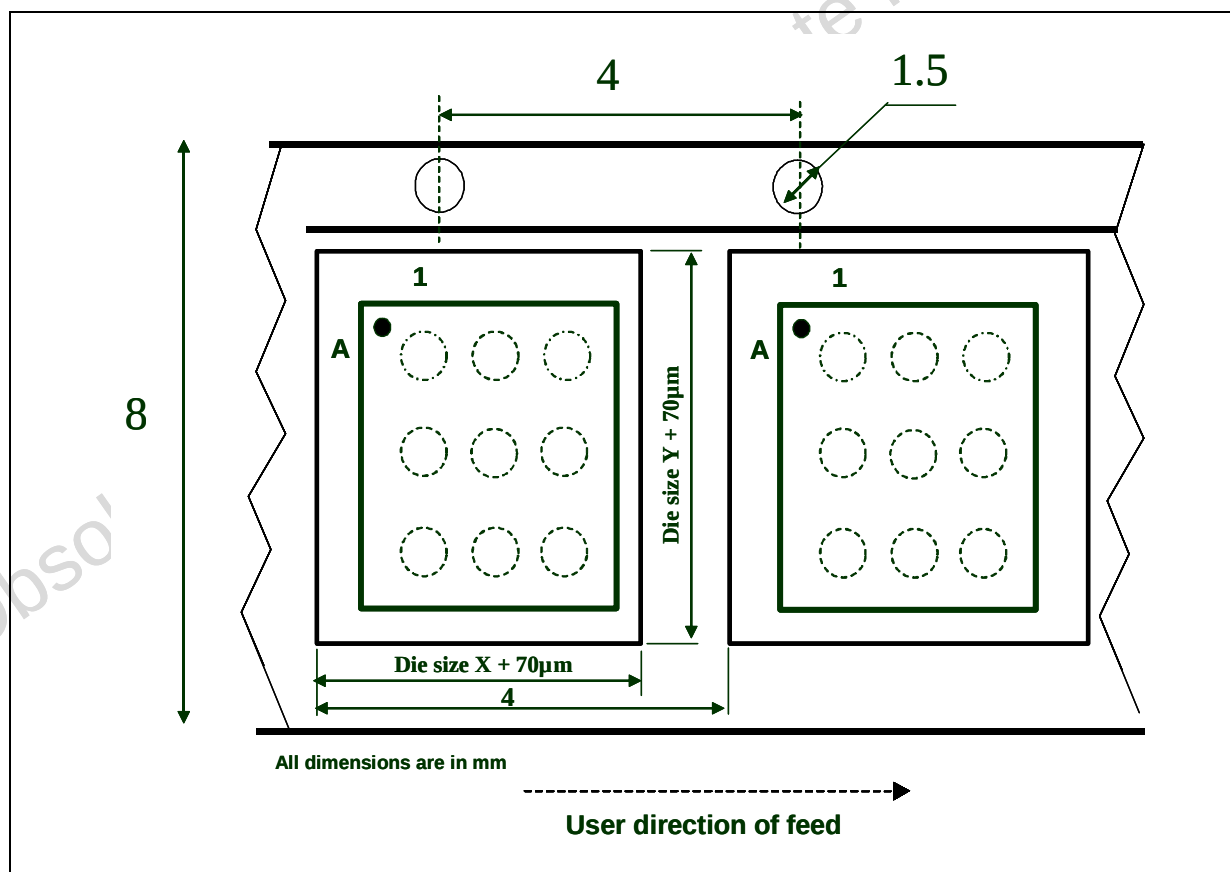


Figure 54: Tape & reel specification (top view)



6 Revision History

Date	Revision	Description of Changes
01 Aug 2004	1	First Release
01 Oct 2004	2	Flip Chip with Back Coating Order Code

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