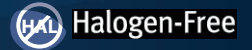
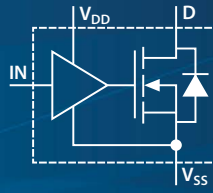


## EPC21701 – eToF™ Laser Driver IC

80 V

15 A Peak

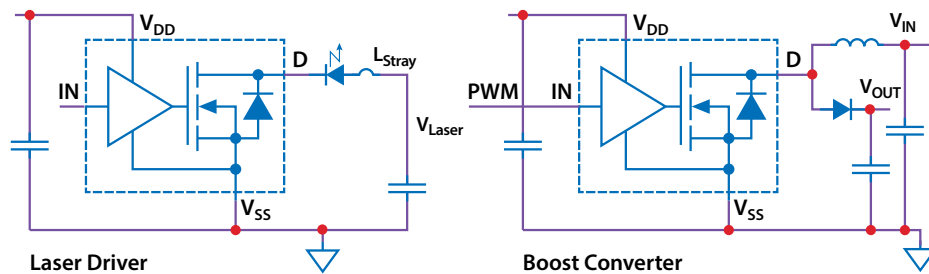


The EPC21701 is a single chip laser driver that is controlled using 3.3 V logic at high frequencies over 50 MHz to modulate laser driving currents of up to 15 Amps. Full driver integration is implemented using EPC's proprietary GaN IC technology.

Wafer-level chip-scale packaging is used resulting in an LGA package that measures only 1.7 x 1 mm. The LGA package has low inductance and lays out very well with the laser system.

The EPC21701 uses a 5 V logic supply and is capable of interfacing to digital controllers. It can switch at frequencies exceeding 50 MHz.

**Figure 1: Typical Connection Diagram**



### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless indicated otherwise.

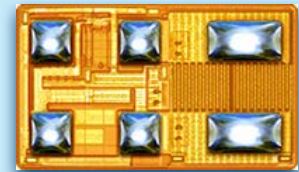
Symbol	Definition	MIN	MAX	UNIT
$V_D$	Drain Voltage		80	V
$V_{DD}$	Low Side Supply Voltage	-0.3	5.5	
IN	Logic Input	-0.3	5	
$I_D$	Average Drain Current		7.2	A
$T_J$	Operating Junction Temperature	-40	125	°C
$T_{STG}$	Storage Temperature	-40	150	

### ESD Ratings

Symbol	Definition	MIN	UNIT
HBW	Human-body model	+/-500	V
CDM	Charged-device model <sup>6</sup>	N/A	

### Thermal Characteristics

Symbol	Definition	MIN	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.5	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	11	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	120	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC9172 EVB)	69	



Die size: 1.7 x 1 mm

EPC21701 eToF laser driver ICs are supplied in passivated die form with solder bumps.

### Features

- $V_{Laser}$  operating range up to 60 V
- 15 A peak current
- Switching frequency greater than 50 MHz
- Typical voltage switching time 1 ns
- 5 V nominal logic power supply
- 3.3 V logic compatible input control
- 2 ns minimum output pulse width
- 3.5 ns delay time from input to output

### Applications

- Time of flight measurement
  - Gesture recognition
  - Driver awareness
  - Robotic vision
  - Industrial safety
- ToF module using VCSEL laser for camera modules, laptops, and smart phones
- Boost control switch
- Flyback control switch
- Forward control switch
- Class-E Amplifier

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC21701>

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless indicated otherwise.

Symbol	Definition	MIN	TYP	MAX	UNIT
$V_{Laser}$	Laser Driver Voltage <sup>5</sup>	5		60	V
$V_{DD}$	Logic Supply Voltage <sup>5</sup>		5		

## Truth Table

IN	Laser
0	Off
1	On

## Electrical Characteristics

All ratings at  $T_j = 25^\circ\text{C}$ .  $V_{Laser} = 40\text{ V}$ ,  $I_D = 10\text{ A}$ ,  $V_{IL} = 0\text{ V}$ ,  $V_{IH} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $f = 50\text{ MHz}$ ,  $t_{PW} = 10\text{ ns}$  unless indicated otherwise.

Symbol	Definition	MIN	TYP	MAX	UNIT
<b>Operating Power Supply, <math>V_{DD}</math></b>					
$I_{DD(Off)}$	$V_{DD}$ Quiescent current with laser driver off		10.4	23	mA
$I_{DD(30\text{ MHz})}$	Operating current off $V_{DD}$		52.5		
<b>Input Pins</b>					
$V_{IH}$	High-level input voltage threshold	1.9			V
$V_{IL}$	Low-level input voltage threshold			0.5	
$V_{IHyst}$	Hysteresis between rising and falling threshold	35			mV
$R_{IN}$	Input pulldown resistance		1.25		k $\Omega$
<b>Power Stage</b>					
$R_{DS(on)}^1$	Drain to Source Resistance		54		m $\Omega$
$I_{D(peak)}^1$	Peak Laser Drive Current Capability, $f = 50\text{ MHz}$	15			A
$C_{OSS}^1$	$V_{DS} = 40\text{ V}$ , $V_{IN} = 0\text{ V}$		80		pF
$Q_{OSS}^1$	$V_{DS} = 40\text{ V}$ , $V_{IN} = 0\text{ V}$		4.2		nC
$E_{OSS}^1$	$V_{DS} = 40\text{ V}$ , $V_{IN} = 0\text{ V}$		70		nJ
$C_{OSS(ER)}^{1,2}$	$V_{DS} = 0\text{ to }40\text{ V}$ , $V_{IN} = 0\text{ V}$		90		pF
$C_{OSS(TR)}^{1,3}$	$V_{DS} = 0\text{ to }40\text{ V}$ , $V_{IN} = 0\text{ V}$		105		
<b>Dynamic Characteristics</b>					
$t_{D(on)}^1$	Turn on delay time		3.7	6.8	ns
$t_F^1$	Drain fall time		0.52	1.5	
$t_{D(off)}^1$	Turn off delay time		3.6	6.1	
$t_R^{1,4}$	Drain rise time		0.42		
$t_{dPW}^1$	Pulse width distortion	-2	-0.12	1.6	
$t_{in(min(on))}^1$	Minimum input pulse width		2		
$t_{D(min(on))}^1$	Minimum drain pulse width		1.9		
$t_{On(Max)}^1$	Maximum on time		500		$\mu\text{s}$
$f_{Max}^1$	Maximum frequency, $0^\circ\text{C}$ to $100^\circ\text{C}$		50		MHz

### Notes:

- 1 Guaranteed by design, but not tested
- 2  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50% max ( $V_D$ )
- 3  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50% max ( $V_D$ )
- 4 Drain rise time is determined by ZVS charging of the output capacitance
- 5 See Power Sequencing section in Applications Information for considerations on laser drive voltage
- 6 Paragraph 2.7 of AEC Q100-011 Rev. D, Jan. 29, 2019 states that CDM specification is not necessary on such a small device

## Pinout Description

Pin	Description
$V_{DD}$	Input Voltage Supply (Decouple to $V_{SS}$ with small, low inductance capacitor)
IN	Logic input
D	Power Drain
$V_{SS}$	Power Source and Signal Return, Internally Connected to Substrate

Performance Curves

Figure 2: Typical Quiescent Current vs. Frequency

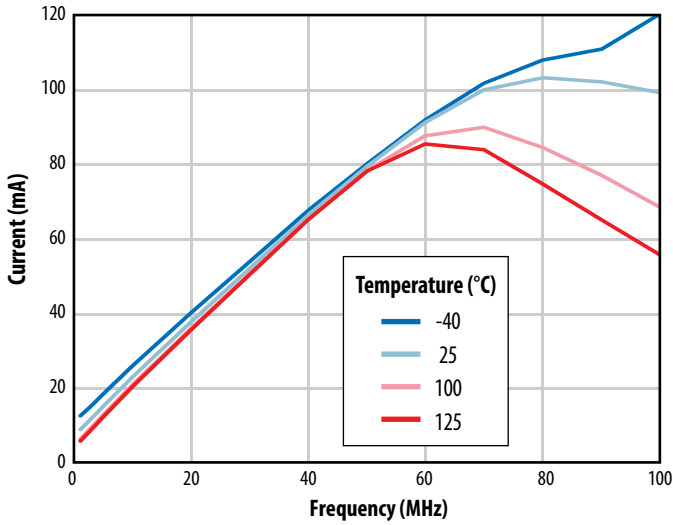


Figure 3: Typical Quiescent Current vs. Temperature

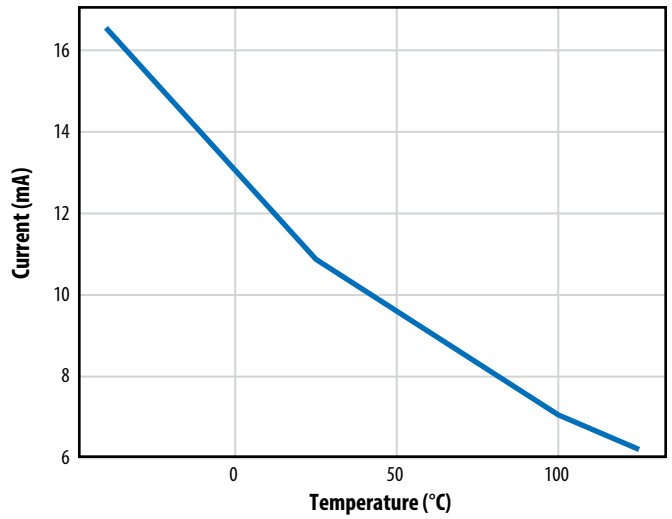


Figure 4: Turn On Propagation Delay vs. Temperature

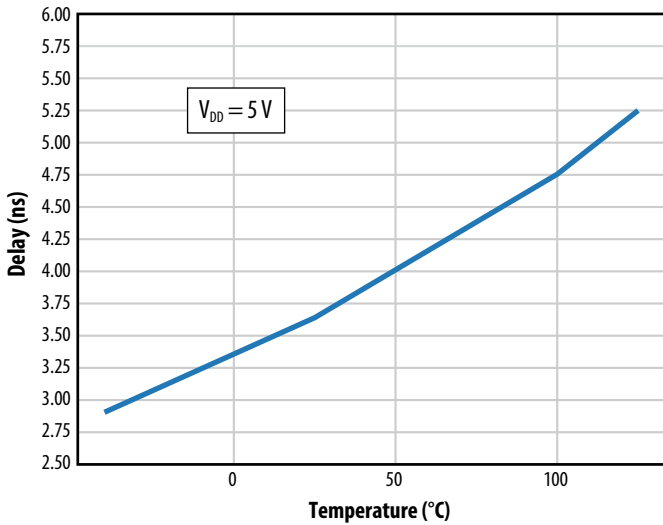


Figure 5: Turn Off Propagation Delay vs. Temperature

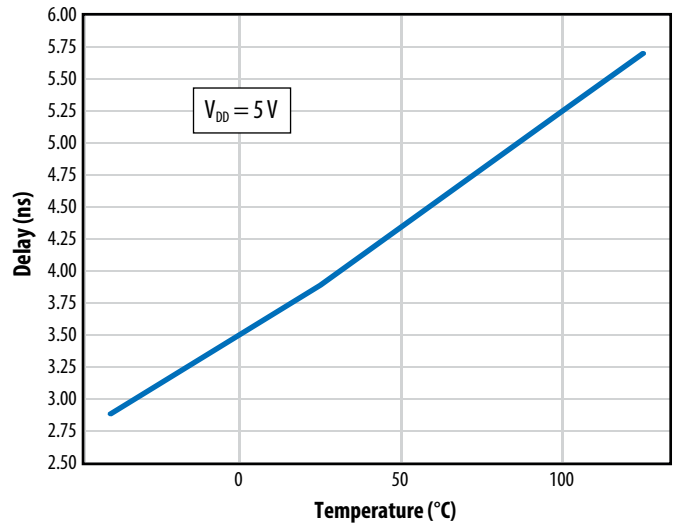


Figure 6: Typical C<sub>oss</sub>

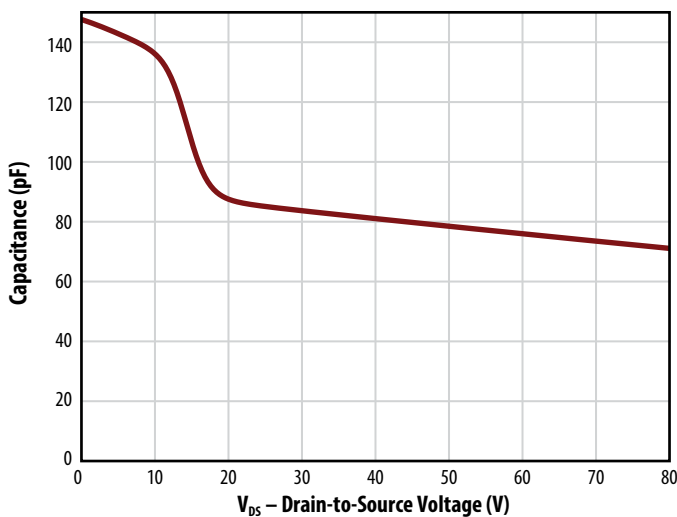


Figure 7: Typical Output Charge and C<sub>oss</sub> Stored Energy

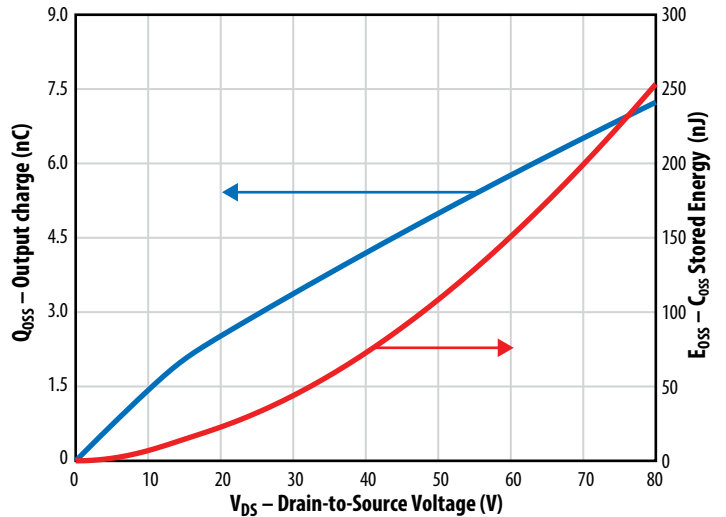
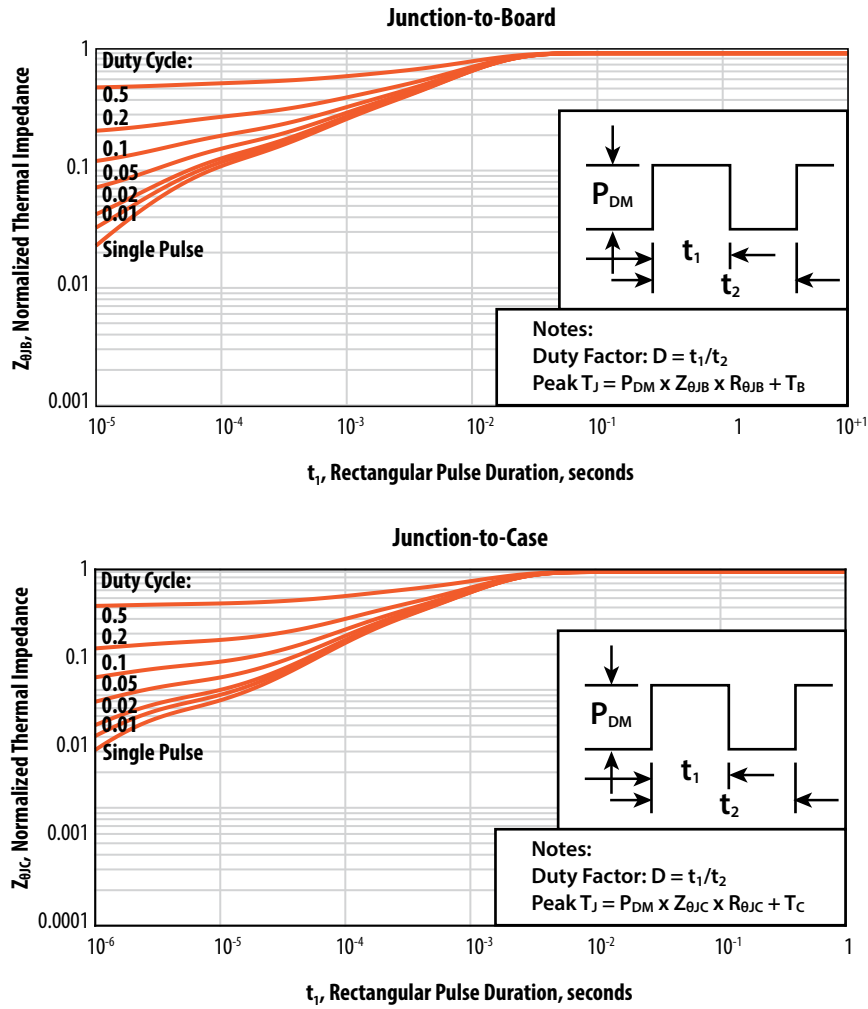


Figure 8: Transient Thermal Impedance



**Application Information**

**Safety Warning**

This device is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

**Power Sequencing**

IN must be held low during power up sequence. For power up, input must be held low until  $V_{DD}$  is up and stabilized. Either Drain or  $V_{DD}$  can be powered first (or together). For power down, IN should be brought low before  $V_{DD}$  is removed. Either Drain or  $V_{DD}$  can be removed first (or together).

Power Up	IN	$V_{DD}$	Drain
1	Low	0 V	0 V
2	Low	5 V	$V_{Laser Drive}$
3	Active	5 V	$V_{Laser Drive}$
Power Down	IN	$V_{DD}$	Drain
1	Low	5 V	$V_{Laser Drive}$
2	Low	0 V	0 V

## Application Information

### Layout and decoupling

Minimizing inductance in both power and gate drive loops is critical. The power loop is primary, and gate drive loop secondary. Short, wide traces are required, and returning in the second layer using a thin dielectric will cancel much of the inductance. Using multiple ceramic capacitors in parallel will reduce stray inductance and impedance in the power loop. Use high quality NPO or COG capacitors for both power and gate drive. This will increase effective capacitance as capacitors with lower quality materials will lose much more capacitance with voltage. Recommended layout is shown below. Component recommendations for power and gate drive decoupling capacitors are shown in [EPC9172 demonstration board](#) quick start guide.

Turn off current is limited by the energy of the power loop stray inductance transferring to the  $C_{OSS}$  of the power FET of the laser driver.  $E_{OSS}$  vs.  $V_{DS}$  curve is in the datasheet (Figure 7).

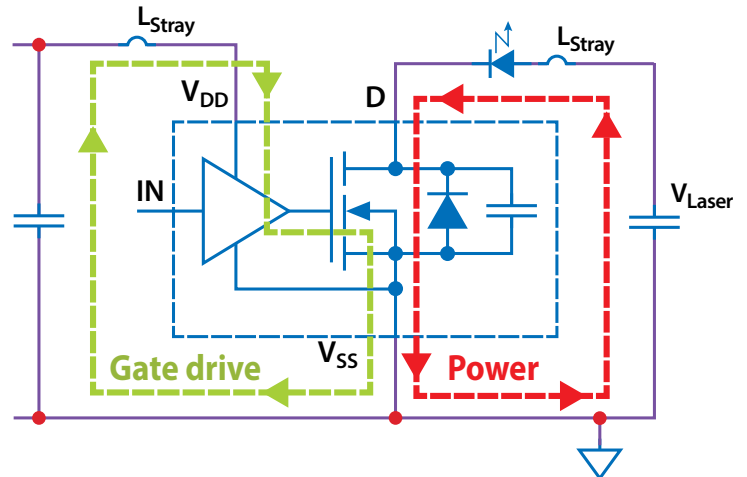
### Start up

$V_{DD}$  should be applied before the laser voltage. For applications where the laser voltage is below 10 V and at elevated temperatures, it may take a few pulses before the pulse width stabilizes.

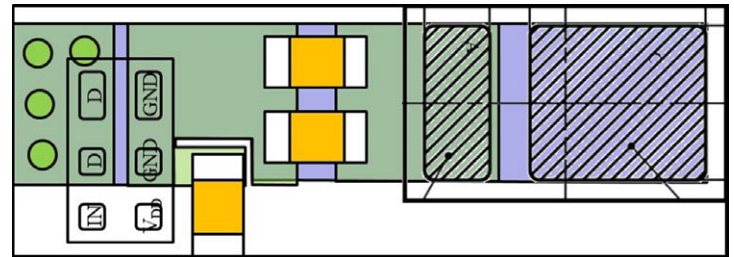
### Output Capacitance

Output capacitance ( $C_{OSS}$ ) is the capacitance between D and  $V_{SS}$ . Output charge ( $Q_{OSS}$ ) is the integral of output capacitance over voltage. Just like discrete power FETs, output capacitance is charged and discharged with each cycle. This takes time and dissipates power. Please refer to FET application notes to determine impact.

## Power and Gate Drive Turn On Loops

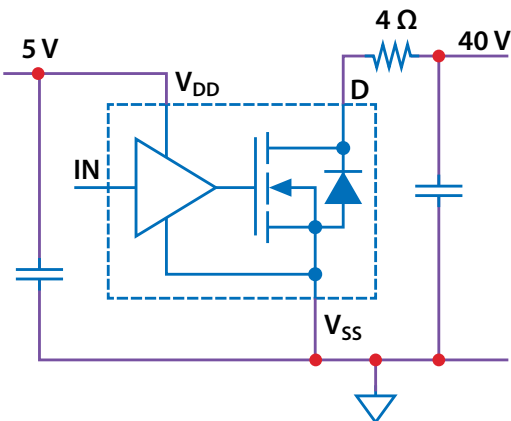


## Recommended Layout

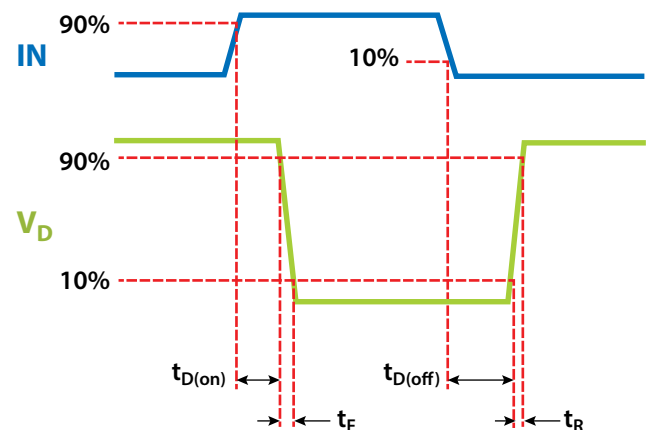


Cathode to drain connection on second conductor layer

## Parameter Measurement Test Circuits

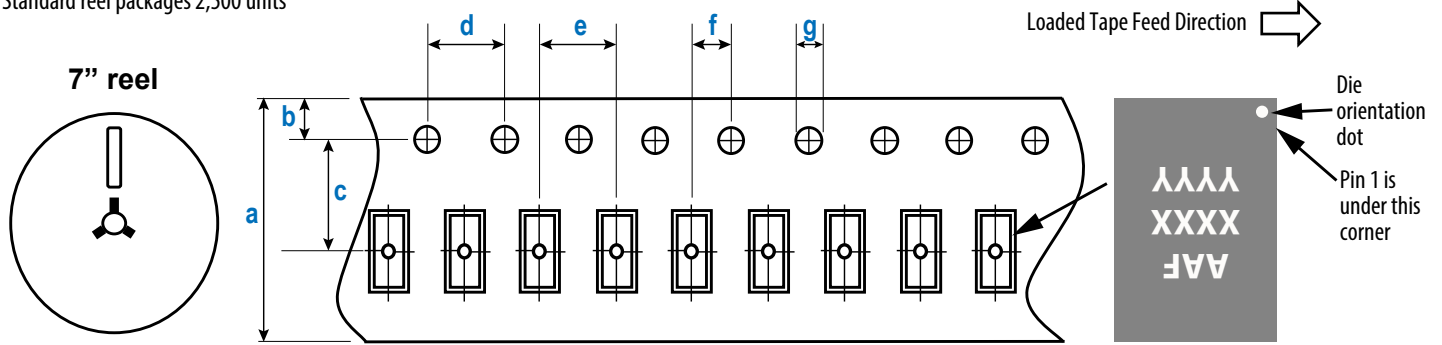


## Parameter Measurement Definitions



**TAPE AND REEL CONFIGURATION**

4 mm pitch, 8 mm wide tape on 7" reel  
Standard reel packages 2,500 units

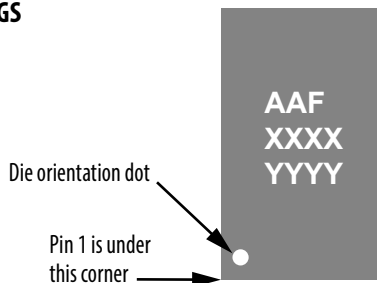


EPC21701 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

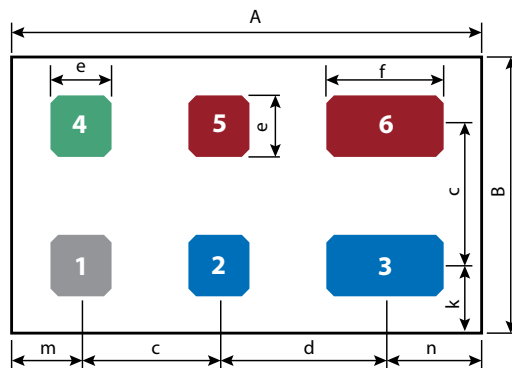
**DIE MARKINGS**



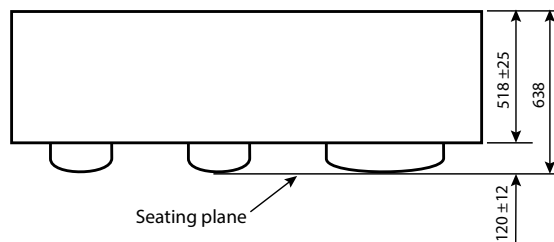
Part Number	Laser Markings		
	Part Number Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC21701	AAAF	XXXX	YYYY

**DIE OUTLINE**

Solder Bump View



Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1620	1650	1680
B	920	950	980
c		500	
d		600	
e	205	225	245
f	405	425	445
k		225	
m		225	
n		325	

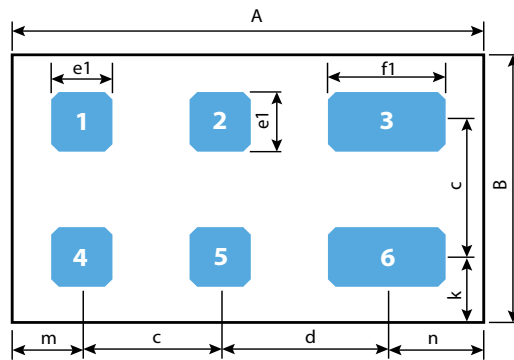
Pad 1 is  $V_{IN}$ ;

Pads 2 & 3 are Drain;

Pad 4 is  $V_{DD}$ ;

Pads 5 and 6 are  $V_{SS}$

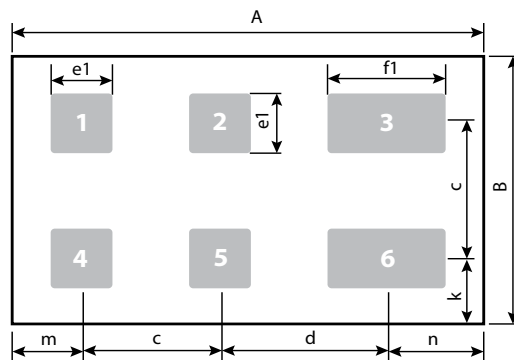
**RECOMMENDED  
LAND PATTERN**  
(units in  $\mu\text{m}$ )



DIM	MICROMETERS
<b>A</b>	1650
<b>B</b>	950
<b>c</b>	500
<b>d</b>	600
<b>e1</b>	205
<b>f1</b>	405
<b>k</b>	225
<b>m</b>	225
<b>n</b>	325

Pad 1 is  $V_{IN}$ ; Pads 2 and 3 are Drain;  
Pad 4 is  $V_{DD}$ ; Pads 5 and 6 are  $V_{SS}$

**RECOMMENDED  
STENCIL DRAWING**  
(measurements in  $\mu\text{m}$ )



DIM	MICROMETERS
<b>A</b>	1650
<b>B</b>	950
<b>c</b>	500
<b>d</b>	600
<b>e1</b>	225
<b>f1</b>	425
<b>k</b>	225
<b>m</b>	225
<b>n</b>	325

Recommended stencil should be 4mil (100  $\mu\text{m}$ ) thick, must be laser cut, opening per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at

<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Revised December, 2022