



8741A UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

- 8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported
- 1024 x 8 EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins
- Fully Compatible with All Microprocessor Families
- 3.6 MHz 8741A-8 Available
- Expandable I/O
- RAM Power-Down Capability
- Over 90 Instructions: 70% Single Byte
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

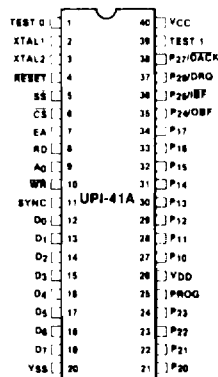
The Intel 8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS[®]-48, MCS-80, MCS-85, MCS-86, and other 8-bit systems.

The UPI-41A has 1K words of program memory and 64 words of data memory on-chip.

The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, single-step mode for debug and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

Pin Configuration



290241-2

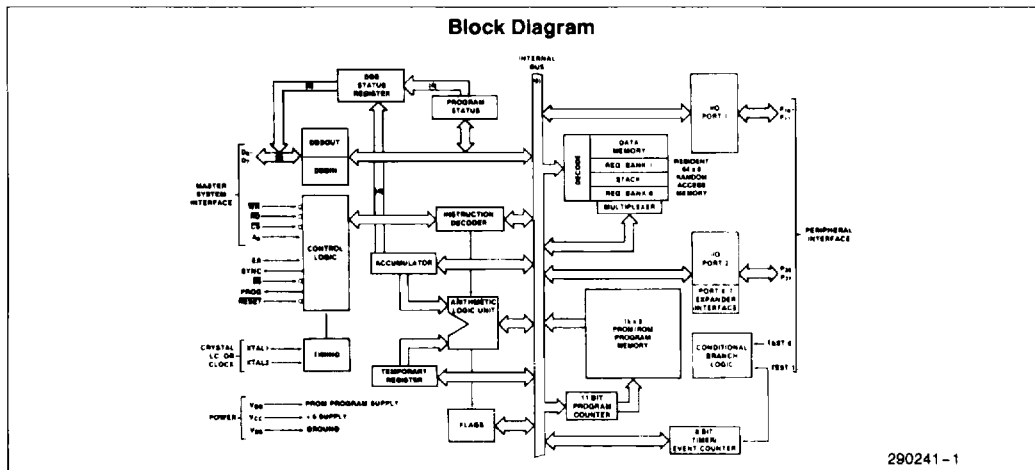


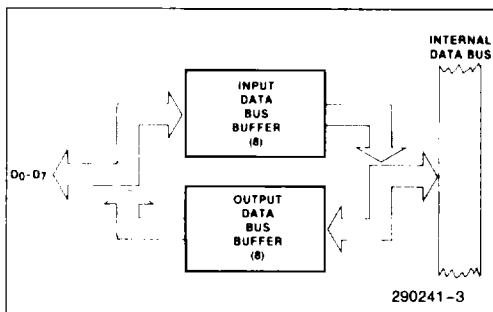
Table 1. Pin Description

Signal	Description
D ₀ –D ₇ (BUS)	Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-41A to an 8-bit master system data bus.
P ₁₀ –P ₁₇	8-bit, PORT 1 quasi-bidirectional I/O lines.
P ₂₀ –P ₂₇	8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P ₂₀ –P ₂₃) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P ₂₄ –P ₂₇) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P ₂₄ as OBF (Output Buffer Full), P ₂₅ as IBF (Input Buffer Full), P ₂₆ as DRQ (DMA Request), and P ₂₇ as DACK (DMA Acknowledge).
WR	I/O write input which enables the master CPU to write data and command words to the UPI-41A INPUT DATA BUS BUFFER.
RD	I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
CS	Chip select input used to select one UPI-41A out of several connected to a common data bus.
A ₀	Address input used by the master processor to indicate whether byte transfer is data or command. During a write operation flag F ₁ is set to the status of the A ₀ input.
TEST 0, TEST 1	Input pins which can be directly tested using conditional branch instructions. (T ₁) also functions as the event timer input (under software control). T ₀ is used during PROM programming and verification in the 8741A.

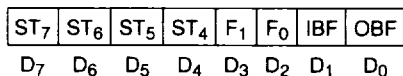
Signal	Description
XTAL 1, XTAL 2	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	Output signal which occurs once per UPI-41A instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
EA	External access input which allows emulation, testing and PROM verification.
PROG	Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243.
RESET	Input used to reset status flip-flops and to set the program counter to zero. RESET is also used during PROM programming and verification. RESET should be held low for a minimum of 8 instruction cycles after power-up.
SS	Single step input used in the 8741A in conjunction with the SYNC output to step the program through each instruction.
V _{CC}	+5V main power supply pin.
V _{DD}	+5V during normal operation. +25V during programming operation. Low power standby supply pin in ROM version.
V _{SS}	Circuit ground potential.

UPI-41A FEATURES AND ENHANCEMENTS

- Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.

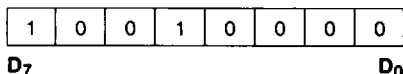


- 8 Bits of Status



ST₄–ST₇ are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the accumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

MOV STS, A Op Code: 90H



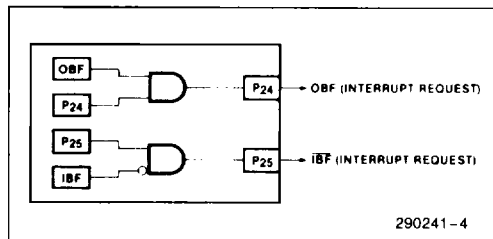
- $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F₁ and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.



- P₂₄ and P₂₅ are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

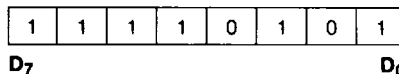
If the "EN FLAGS" instruction has been executed, P₂₄ becomes the OBF (Output Buffer Full) pin. A "1" written to P₂₄ enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P₂₄ disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI41A (in Output Data Bus Buffer).

If "EN FLAGS" has been executed, P₂₅ becomes the IBF (Input Buffer Full) pin. A "1" written to P₂₅ enables the IBF pin (the pin outputs the inverse of the IBF Status Bit). A "0" written to P₂₅ disables the IBF pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.



Data Bus Buffer Interrupt Capability

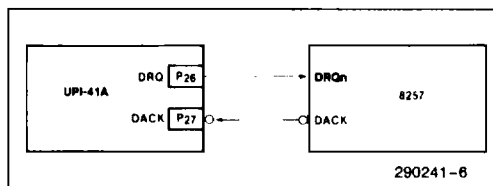
EN FLAGS Op Code: 0F5H



- P₂₆ and P₂₇ are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

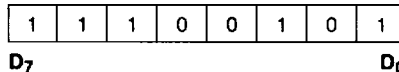
If the "EN DMA" instruction has been executed, P₂₆ becomes the DRQ (DMA Request) pin. A "1" written to P₂₆ causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

If "EN DMA" has been executed, P₂₇ becomes the DACK (DMA Acknowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA Handshake Capability

EN DMA Op Code: 0E5H



APPLICATIONS

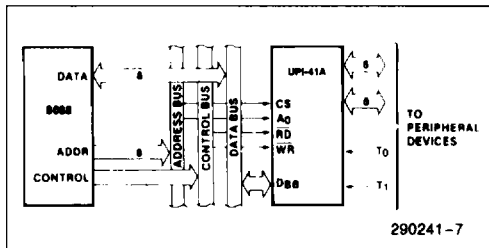


Figure 1. 8085A-8741A Interface

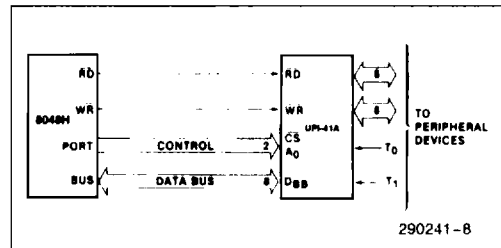


Figure 2. 8048H-8741A Interface

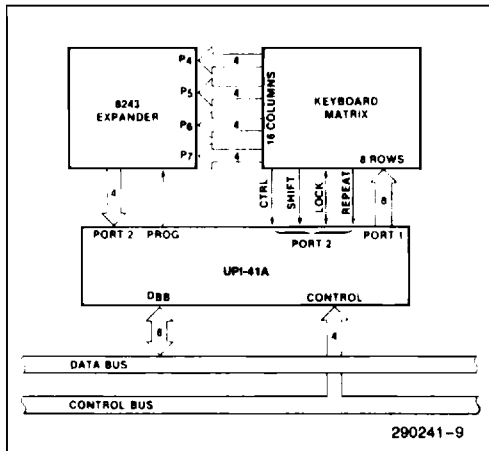


Figure 3. 8741A-8243 Keyboard Scanner

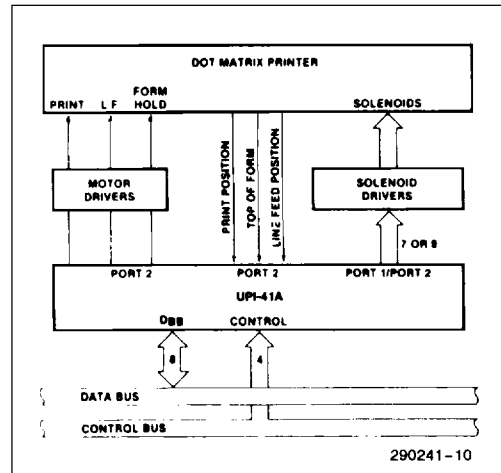


Figure 4. 8741A Matrix Printer Interface

PROGRAMMING, VERIFYING, AND ERASING THE 8741A EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6 MHz)
Reset	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output during Verify
P20-1	Address Input
V _{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed 8741A will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. $A_0 = 0V$, $CS = 5V$, $EA = 5V$, $\overline{RESET} = 0V$, $TEST0 = 5V$, $V_{DD} = 5V$, clock applied or internal oscillator operating, BUS and PROG floating
2. Insert 8741A in programming socket
3. $TEST\ 0 = 0V$ (select program mode)
4. $EA = 23V$ (active program mode)
5. Address applied to BUS and P20-1
6. $\overline{RESET} = 5V$ (latch address)
7. Data applied to BUS

8. $V_{DD} = 25V$ (programming power)
9. $PROG = 0V$ followed by one 50 ms pulse to 23V
10. $V_{DD} = 5V$
11. $TEST\ 0 = 5V$ (verify mode)
12. Read and verify data on BUS
13. $TEST\ 0 = 0V$
14. $\overline{RESET} = 0V$ and repeat from step 6
15. Programmer should be at conditions of step 1 when 8741A is removed from socket

8741A Erasure Characteristics

The erasure characteristics of the 8741A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms ($\text{\AA}$). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 $\text{\AA}$ range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8741A in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8741A window to prevent unintentional erasure.

The recommended erasure procedure for the 8741A is exposure to shortwave ultraviolet light which has a wavelength of 2537 $\text{\AA}$. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15 w-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The 8741A should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias 0°C to +70°C
Storage Temperature -65°C to +150°C
Voltage on Any Pin with
Respect to Ground 0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} 0V, V_{CC} = V_{DD} = +5V ±10%

Symbol	Parameter	Min	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage (except XTAL1, XTAL2, $\overline{\text{RESET}}$)	-0.5	0.8	V	
V _{IL1}	Input Low Voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	-0.5	0.6	V	
V _{IH}	Input High Voltage (except XTAL1, XTAL2, $\overline{\text{RESET}}$)	2.2	V _{CC}		
V _{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	3.8	V _{CC}	V	
V _{OL}	Output Low Voltage (D ₀ -D ₇)		0.45	V	I _{OL} = 2.0 mA
V _{OL1}	Output Low Voltage (P ₁₀ P ₁₇ , P ₂₀ P ₂₇ , Sync)		0.45	V	I _{OL} = 1.6 mA
V _{OL2}	Output Low Voltage (PROG)		0.45	V	I _{OL} = 1.0 mA
V _{OH}	Output High Voltage (D ₀ -D ₇)	2.4		V	I _{OH} = -400 μ A
V _{OH1}	Output High Voltage (All Other Outputs)	2.4		V	I _{OH} = -50 μ A
I _{IL}	Input Leakage Current (T ₀ , T ₁ , $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, A ₀ , EA)		±10	μ A	V _{SS} ≤ V _{IN} ≤ V _{CC}
I _{OZ}	Output Leakage Current (D ₀ -D ₇ , High Z State)		±10	μ A	V _{SS} + 0.45 ≤ V _{IN} ≤ V _{CC}
I _{LI}	Low Input Load Current (P ₁₀ P ₁₇ , P ₂₀ P ₂₇)		0.5	mA	V _{IL} = 0.8V
I _{LI1}	Low Input Load Current ($\overline{\text{RESET}}$, $\overline{\text{SS}}$)		0.2	mA	V _{IL} = 0.8V
I _{DD}	V _{DD} Supply Current		15	mA	Typical = 5 mA
I _{CC} + I _{DD}	Total Supply Current		125	mA	Typical = 60 mA

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A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{SS} = 0V, V_{CC} = V_{DD} = +5V ±10%

DBB READ

Symbol	Parameter	Min	Max	Unit	Test Conditions
t _{AR}	$\overline{\text{CS}}$, A ₀ Setup to $\overline{\text{RD}}$ ↓	0		ns	
t _{RA}	$\overline{\text{CS}}$, A ₀ Hold after $\overline{\text{RD}}$ ↑	0		ns	
t _{RR}	$\overline{\text{RD}}$ Pulse Width	250		ns	
t _{AD}	$\overline{\text{CS}}$, A ₀ to Data Out Delay		225	ns	C _L = 150 pF
t _{RD}	$\overline{\text{RD}}$ ↓ to Data Out Delay		225	ns	C _L = 150 pF
t _{DF}	$\overline{\text{RD}}$ ↑ to Data Float Delay		100	ns	
t _{CY}	Cycle Time (except 8741A-8)	2.5	15	μ s	6.0 MHz XTAL
t _{CY}	Cycle Time (8741A-8)	4.17	15	μ s	3.6 MHz XTAL

DBB WRITE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	0		ns	
t_{WA}	$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$ ↑	150		ns	
t_{WD}	Data Hold after $\overline{WR}$ ↑	0		ns	

A.C. TIMING SPECIFICATION FOR PROGRAMMING

 $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = +5\text{V} \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Setup Time to $\overline{\text{RESET}}$ ↑	$4t_{CY}$			
t_{WA}	Address Hold Time after $\overline{\text{RESET}}$ ↑	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG ↑	$4t_{CY}$			
t_{WD}	Data in Hold Time after PROG ↓	$4t_{CY}$			
t_{PH}	$\overline{\text{RESET}}$ Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Setup Time to PROG ↑	$4t_{CY}$			
t_{VDDH}	V_{DD} Hold Time after PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	Test 0 Hold Time after Program Mode	$4t_{CY}$			
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$		
t_{WW}	$\overline{\text{RESET}}$ Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{\text{RESET}}$ Setup Time before EA ↑	$4t_{CY}$			

NOTE:

1. If TEST 0 is high, t_{DO} can be triggered by $\overline{\text{RESET}}$ ↑.

D.C. SPECIFICATION FOR PROGRAMMING

 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}, V_{CC} = 5\text{V} \pm 5\%, V_{DD} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

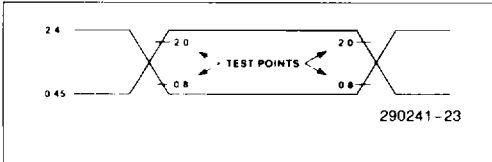
A.C. CHARACTERISTICS—DMA

Symbol	Parameter	Min	Max	Units	Test Conditions
t _{ACC}	DACK to $\overline{WR}$ or $\overline{RD}$	0		ns	
t _{CAC}	$\overline{RD}$ or $\overline{WR}$ to DACK	0		ns	
t _{ACD}	DACK to Data Valid		225	ns	C _L = 150 pF
t _{CRQ}	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared		200	ns	

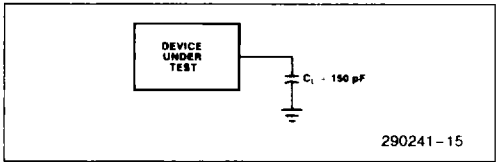
A.C. CHARACTERISTICS—PORT 2 T_A = 0°C to +70°C, V_{CC} = +5V ± 10%

Symbol	Parameter	Min	Max	Units	Test Conditions
t _{CP}	Port Control Setup before Falling Edge of PROG	10		ns	
t _{PC}	Port Control Hold after Falling Edge of PROG	100		ns	
t _{PR}	PROG to Time P2 Input Must Be Valid		810	ns	
t _{PF}	Input Data Hold Time	0	150	ns	
t _{DP}	Output Data Setup Time	250		ns	
t _{PD}	Output Data Hold Time	65		ns	
t _{pp}	PROG Pulse Width	1200		ns	

A.C. TESTING INPUT/OUTPUT WAVEFORM

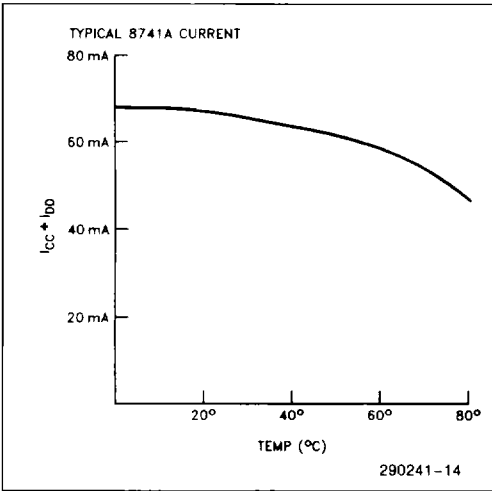


A.C. TESTING LOAD CIRCUIT

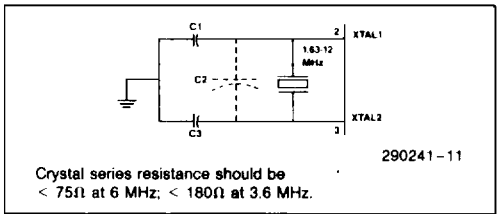


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TYPICAL 8741A CURRENT



CRYSTAL OSCILLATOR MODE



Crystal series resistance should be
< 75Ω at 6 MHz; < 180Ω at 3.6 MHz.

DRIVING FROM EXTERNAL SOURCE

Both XTAL1 and XTAL2 should be driven.
Resistors to V_{CC} are needed to ensure $V_{IH} = 3.8V$ if TTL circuitry is used.

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LC OSCILLATOR MODE

L	C	NOMINAL f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz

$$f = \frac{1}{2\pi\sqrt{LC'}}$$
$$C' = \frac{C + 3C_{pp}}{2}$$
$$C_{pp} \approx 5-10 \text{ pF}$$

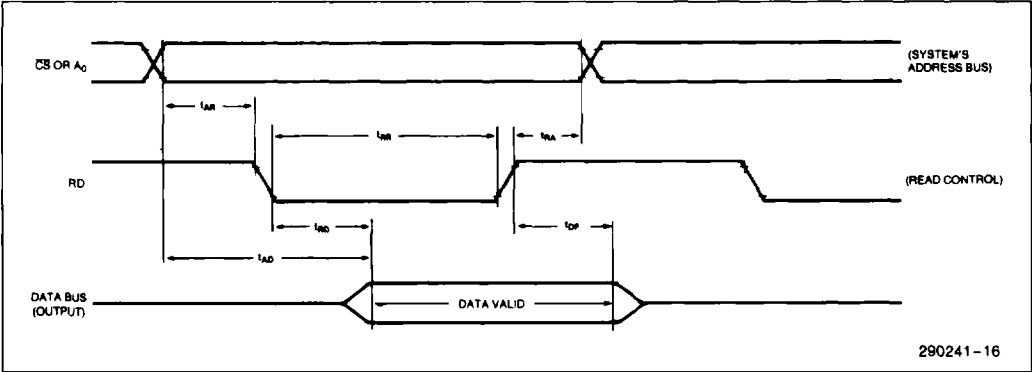
Pin-to-Pin Capacitance

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Each C should be approximately 20 pF, including stray capacitance.

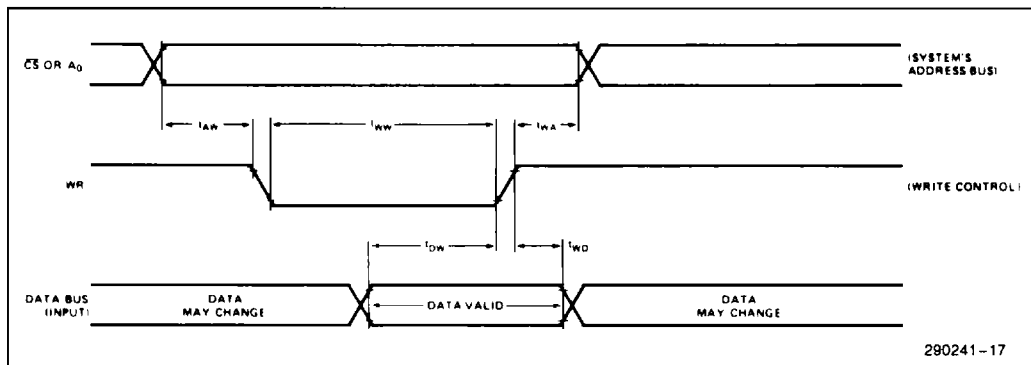
WAVEFORMS

READ OPERATION—DATA BUS BUFFER REGISTER

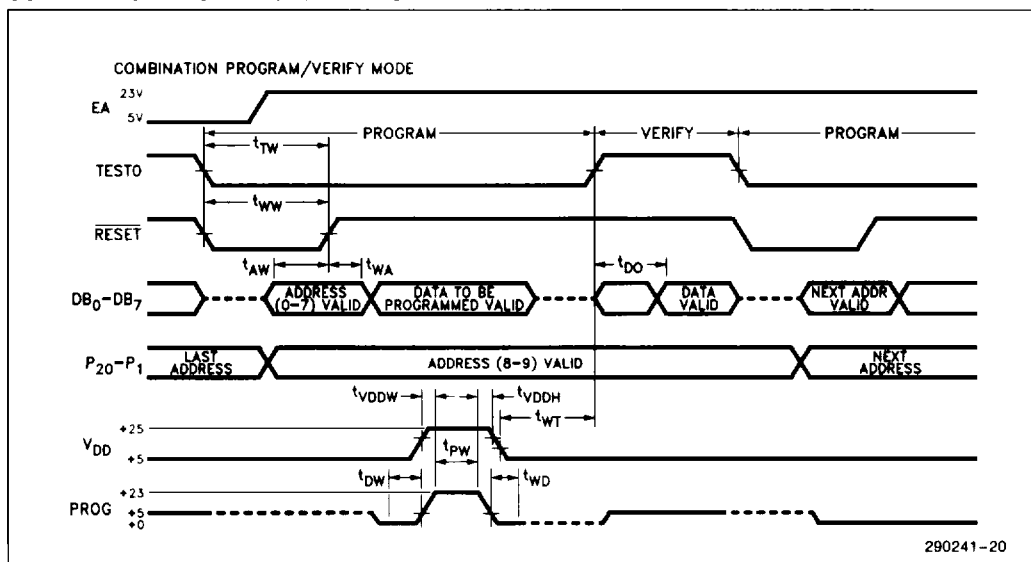


WAVEFORMS

WRITE OPERATION—DATA BUS BUFFER REGISTER

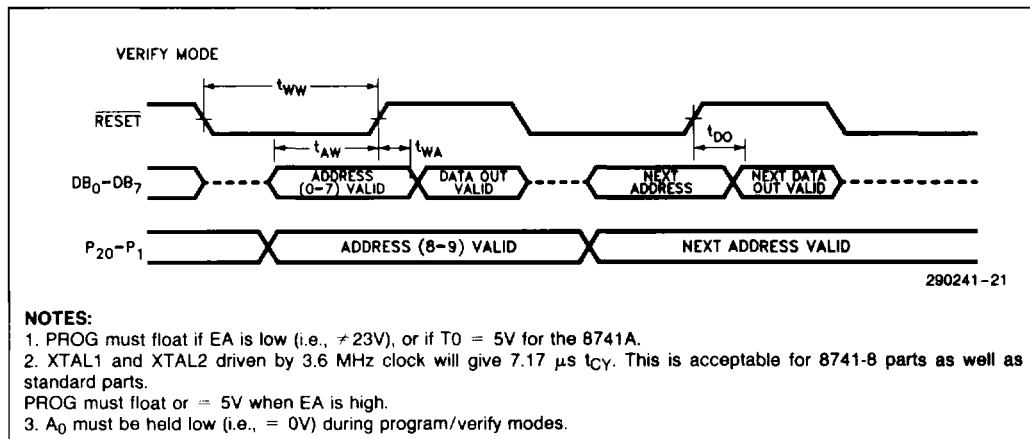


COMBINATION PROGRAM/VERIFY MODE

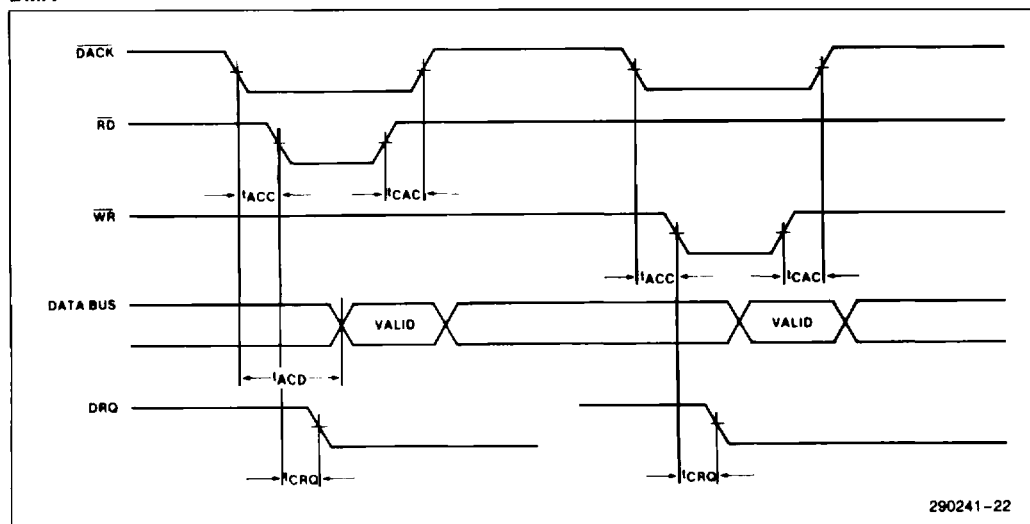


WAVEFORMS

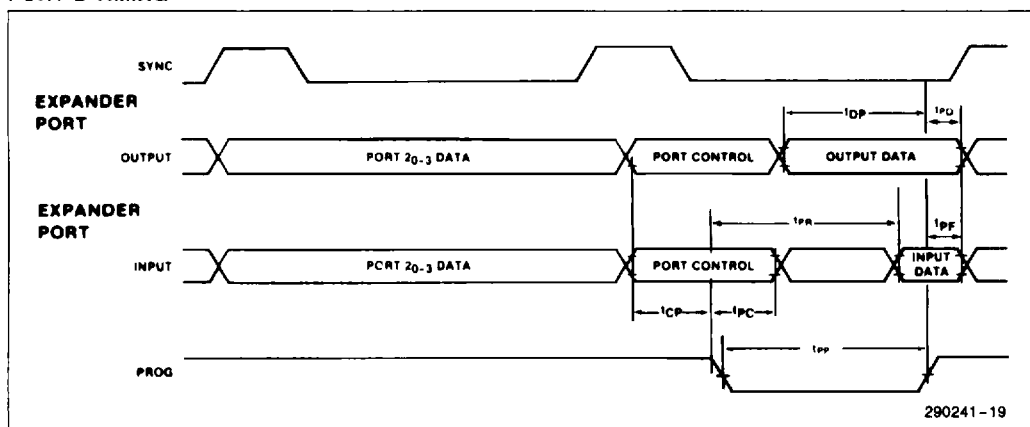
VERIFY MODE



DMA



PORT 2 TIMING



PORT TIMING DURING EXTERNAL ACCESS (EA)

