

16-bit Single Chip Microcontroller

- Low voltage operation from 1.2 V with a single alkaline or silver oxide button battery.
- Ultra low standby power consumption (0.4 μ A during HALT state in super economy mode)
- Embedded A/D converter to support various sensing applications

■ DESCRIPTIONS

The S1C17W34/W35/W36 is a 16-bit MCU that features low-voltage operation from 1.2 V even though Flash memory is included. The embedded high-efficiency DC-DC converter generates the constant-voltage to drive the IC with lower power consumption than 4-bit MCUs. This IC includes a real-time clock, a stopwatch, an LCD driver, a temperature sensor, an A/D converter, and a PWM timer capable of being used to generate drive waveforms for a motor driver as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an LCD display and a temperature measurement function.

■ FEATURES

Model	S1C17W34	S1C17W35	S1C17W36
CPU			
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17		
Other	On-chip debugger		
Embedded Flash memory			
Capacity	128K bytes (for both instructions and data)	256K bytes (for both instructions and data)	384K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * Programming by the debugging tool ICDmini		
Other	Security function to protect from reading/programming by ICDmini		
	On-board programming function using ICDmini		
	Flash programming voltage can be generated internally.		
Embedded RAM			
Capacity	12K bytes		16K bytes
Embedded display RAM			
Capacity	640 bytes		
Clock generator (CLG)			
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)		
System clock frequency (operating frequency)	1.1 MHz (max.) VDD = 1.2 to 1.6 V		
	4.2 MHz (max.) VDD = 1.6 to 3.6 V		
IOSC oscillator circuit (boot clock source)	700 kHz (typ.) embedded oscillator		
	23 μs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)		
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator		
	Oscillation stop detection circuit included		
OSC3 oscillator circuit	4.2 MHz (max.) crystal/ceramic oscillator		
	250, 384, 500 kHz, 1, 2, and 4 MHz-switchable embedded oscillator		
	2.1 MHz (max.) CR oscillator (an external R is required)		
EXOSC clock input	4.2 MHz (max.) square or sine wave input		
Other	Configurable system clock division ratio		
	2 channels of external clock outputs (FOUT)		
	Configurable system clock used at wake up from SLEEP state		
	Operating clock frequency for the CPU and all peripheral circuits is selectable.		
I/O port (PPORT)			
Number of general-purpose I/O ports	Input/output port: 52 bits (max.)		
	Output port: 1 bit (max.)		
	Pins are shared with the peripheral I/O.		
Number of input interrupt ports	48 bits (max.)		
Number of ports that support universal port multiplexer (UPMUX)	32 bits		
	A peripheral circuit I/O function selected via software can be assigned to each port.		
Timers			
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.		
	Programmable NMI/reset generation cycle		
Real-time clock (RTCA2)	3 time zones		
	128-1 Hz and second counters (common for all time zones)		
	Minute, hour, day, day of the week, month, and year counters (available for each time zone)		
	Theoretical regulation function for 1-second correction		
	Alarm and stopwatch functions		
16-bit timer (T16)	4 channels		
	Generates the SPIA master clocks and the ADC12A operating clock/trigger signal.		
16-bit PWM timer (T16B)	3 channels		
	Event counter/capture function		
	PWM waveform generation function		
	Number of PWM output or capture input ports: 2 ports/channel		

S1C17W34/W35/W36

Model	S1C17W34	S1C17W35	S1C17W36
Supply voltage detector (SVD)			
Detection level	30 levels (1.2 to 3.6 V)		
Other	Intermittent operation mode Generates an interrupt or reset according to the detection level evaluation. V _{DD} or an external voltage level is detectable.		
Serial interfaces			
UART (UART2)	2 channels Baud-rate generator included, IrDA1.0 supported Open drain output, signal polarity, and baud rate division ratio are configurable.		
Synchronous serial interface (SPIA)	2 channels 2 to 16-bit variable data length The 16-bit timer (T16) can be used for the baud-rate generator in master mode.		
I ² C (I2C) *1	1 channel Baud-rate generator included		
Sound generator (SNDA)			
Buzzer output function	512 Hz to 16 kHz output frequencies One-shot output function		
Melody generation function	Pitch: 128 Hz to 16 kHz ≈ C3 to C6 Duration: 7 notes/rests (Half note/rest to thirty-second note/rest) Tempo: 16 tempos (30 to 480) Tie/slur may be specified.		
IR remote controller (REMC2)			
Number of transmitter channels	1 channel		
Other	EL lamp drive waveform can be generated for an application example.		
LCD driver (LCD32B)			
LCD output	80 SEG × 1–16 COM (max.), 64 SEG × 17–32 COM (max.)		
LCD contrast	16 levels		
Other	1/5 or 1/4 bias power supply included, external voltage can be applied.		
R/F converter (RFC)			
Conversion method	CR oscillation type with 24-bit counters		
Number of conversion channels	2 channels (Up to two sensors can be connected to each channel.)		
Supported sensors	DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only)		
12-bit A/D converter (ADC12A)			
Conversion method	Successive approximation type		
Resolution	12 bits		
Number of conversion channels	1 channel		
Number of analog signal inputs	8 ports/channel (The temperature sensor output is connected to a port.)		
Temperature sensor/reference voltage generator (TSRVR)			
Temperature sensor circuit	Sensor output can be measured using ADC12A.		
Reference voltage generator	Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V _{DD} , and external input.		
Multiplier/divider (COPRO2)			
Arithmetic functions	16-bit × 16-bit multiplier 16-bit × 16-bit + 32-bit multiply and accumulation unit 32-bit ÷ 32-bit divider		
Reset			
#RESET pin	Reset when the reset pin is set to low.		
Power-on reset	Reset at power on.		
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).		
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).		
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).		
Interrupt			
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)		
Programmable interrupt	External interrupt: 2 systems (8 levels) Internal interrupt: 21 systems (8 levels)		
Power supply voltage			
V _{DD} operating voltage	1.2 to 3.6 V		
V _{DD} operating voltage for Flash programming	2.4 to 3.6 V (V _{PP} = 7.5 V external power supply is required.) 2.4 to 3.6 V (When V _{PP} is generated internally)		
V _{DD} operating voltage for using LCD driver	2.5 to 3.6 V		
V _{DD} operating voltage for super economy mode	2.5 to 3.6 V		
Operating temperature			
Operating temperature range	-40 to 85 °C		
Current consumption (Typ. value)			
SLEEP mode *2	0.15 μA I _{OSC} = OFF, OSC1 = OFF, OSC3 = OFF		
HALT mode	0.6 μA OSC1 = 32 kHz, RTC = ON 0.4 μA OSC1 = 32 kHz, RTC = ON, super economy mode 5.4 μA OSC1 = 32 kHz, RTC = ON, LCD = ON (no panel load, 1/5 bias), super economy mode		

S1C17W34/W35/W36

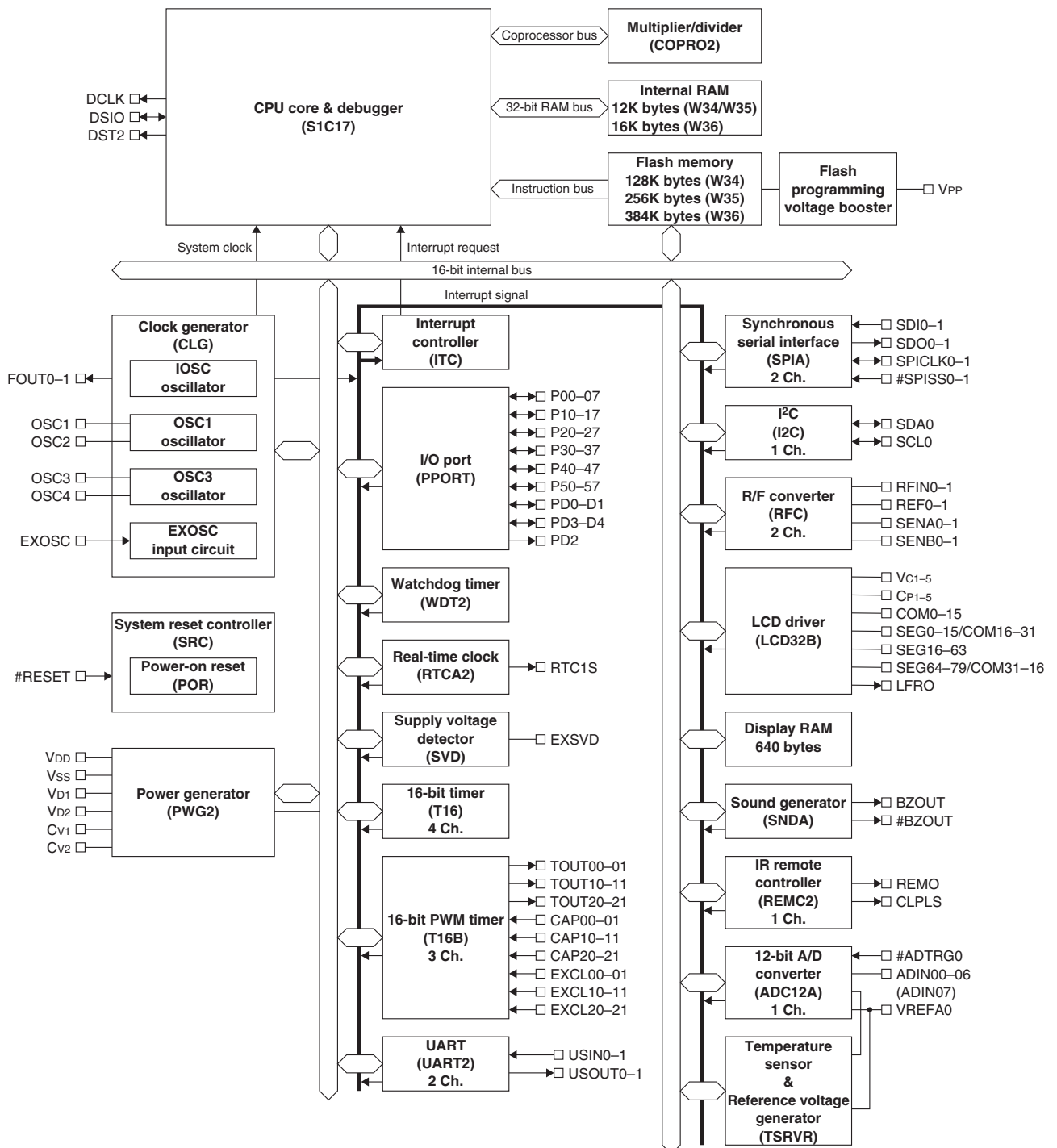
Model	S1C17W34	S1C17W35	S1C17W36
Current consumption (Typ. value)			
RUN mode	6 μA OSC1 = 32 kHz, RTC = ON, CPU = OSC1		
	3 μA OSC1 = 32 kHz, RTC = ON, CPU = OSC1, super economy mode		
	150 μA		
	OSC3 = 1 MHz (ceramic oscillator), OSC1 = 32 kHz, RTC = ON, CPU = OSC3		
Shipping form			
1 *3	QFP21-176PIN (P-LQFP176-2424-0.50, 24 × 24 mm, t = 1.7 mm, 0.5 mm pitch)		
2	Die form (Pad pitch: 80 μm (min.))		

*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.

*2 The RAM retains data even in SLEEP mode.

*3 Shown in parentheses is a JEITA package name.

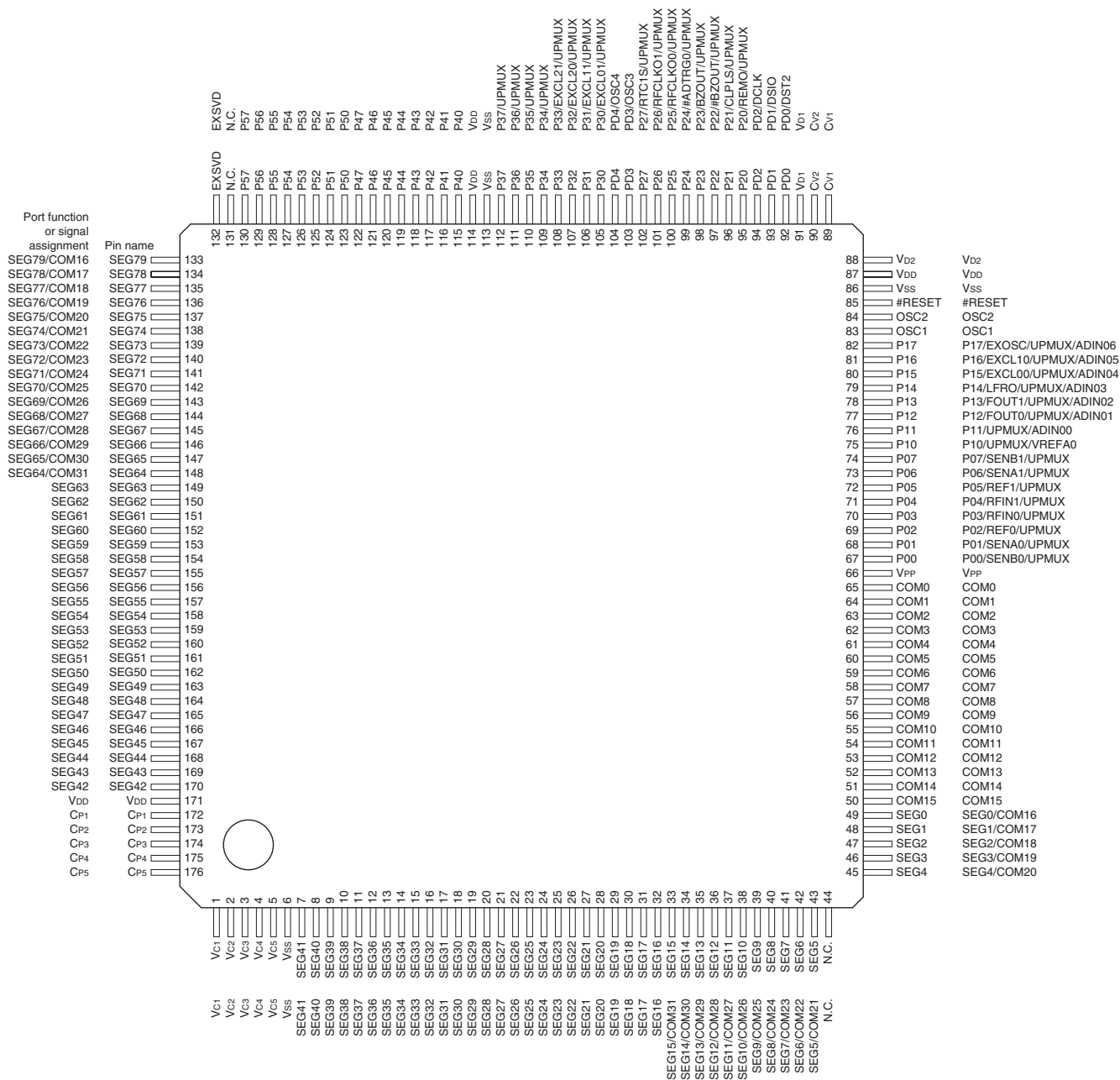
BLOCK DIAGRAM



S1C17W34/W35/W36

■ PIN CONFIGURATION DIAGRAMS

QFP21-176PIN



Chip



S1C17W34/W35/W36

PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the “I/O Ports” chapter).

I/O:	I	= Input
	O	= Output
	I/O	= Input/output
	P	= Power supply
	A	= Analog signal
	Hi-Z	= High impedance state
Initial state:	I (Pull-up)	= Input with pulled up
	I (Pull-down)	= Input with pulled down
	Hi-Z	= High impedance state
	O (H)	= High level output
	O (L)	= Low level output

Tolerant fail-safe structure:



= Over voltage tolerant fail-safe type I/O cell included (see the “I/O Ports” chapter)

The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD} .

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	–	–	Power supply (+)
V_{SS}	V_{SS}	P	–	–	GND
V_{PP}	V_{PP}	P	–	–	Power supply for Flash programming
V_{D1}	V_{D1}	A	–	–	DC-DC converter output
V_{D2}	V_{D2}	A	–	–	DC-DC converter stabilization capacitor connect pin
$CV1-2$	$CV1-2$	A	–	–	DC-DC converter charge pump capacitor connect pins
$VC1-5$	$VC1-5$	P	–	–	LCD panel driver power supply
$CP1-5$	$CP1-5$	A	–	–	LCD power supply booster capacitor connect pins
OSC1	OSC1	A	–	–	OSC1 oscillator circuit input
OSC2	OSC2	A	–	–	OSC1 oscillator circuit output
#RESET	#RESET	I	I (Pull-up)	–	Reset input
P00	P00	I/O	Hi-Z	–	I/O port
	SENB0	A			R/F converter Ch.0 sensor B oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P01	P01	I/O	Hi-Z	–	I/O port
	SENA0	A			R/F converter Ch.0 sensor A oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P02	P02	I/O	Hi-Z	–	I/O port
	REF0	A			R/F converter Ch.0 reference oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P03	P03	I/O	Hi-Z	–	I/O port
	RFIN0	A			R/F converter Ch.0 oscillation input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P04	P04	I/O	Hi-Z	–	I/O port
	RFIN1	A			R/F converter Ch.1 oscillation input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P05	P05	I/O	Hi-Z	–	I/O port
	REF1	A			R/F converter Ch.1 reference oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P06	P06	I/O	Hi-Z	–	I/O port
	SENA1	A			R/F converter Ch.1 sensor A oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P07	P07	I/O	Hi-Z	–	I/O port
	SENB1	A			R/F converter Ch.1 sensor B oscillator pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P10	P10	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input

S1C17W34/W35/W36

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P11	P11	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0
P12	P12	I/O	Hi-Z	–	I/O port
	FOUT0	O			Clock external output Ch.0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1
P13	P13	I/O	Hi-Z	–	I/O port
	FOUT1	O			Clock external output Ch.1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2
P14	P14	I/O	Hi-Z	–	I/O port
	LFRO	O			LCD frame signal monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3
P15	P15	I/O	Hi-Z	–	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4
P16	P16	I/O	Hi-Z	–	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5
P17	P17	I/O	Hi-Z	–	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6
P20	P20	I/O	Hi-Z	–	I/O port
	REMO	O			IR remote controller transmit data output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P21	P21	I/O	Hi-Z	–	I/O port
	CLPLS	O			IR remote controller clear pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P22	P22	I/O	Hi-Z	–	I/O port
	#BZOUT	O			Sound generator inverted output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P23	P23	I/O	Hi-Z	–	I/O port
	BZOUT	O			Sound generator output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P24	P24	I/O	Hi-Z	–	I/O port
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P25	P25	I/O	Hi-Z	–	I/O port
	RFCLK00	O			R/F converter Ch.0 clock monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P26	P26	I/O	Hi-Z	–	I/O port
	RFCLK01	O			R/F converter Ch.1 clock monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P27	P27	I/O	Hi-Z	–	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P30	P30	I/O	Hi-Z	–	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P31	P31	I/O	Hi-Z	–	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P32	P32	I/O	Hi-Z	–	I/O port
	EXCL20	I			16-bit PWM timer Ch.2 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P33	P33	I/O	Hi-Z	–	I/O port
	EXCL21	I			16-bit PWM timer Ch.2 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P34	P34	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

S1C17W34/W35/W36

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P35	P35	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P36	P36	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P37	P37	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P40–47	P40–47	I/O	Hi-Z	–	I/O ports
P50–57	P50–57	I/O	Hi-Z	–	I/O ports
PD0	DST2	O	O (L)	–	On-chip debugger status output
	PD0	I/O			I/O port
PD1	DSIO	I/O	I (Pull-up)	–	On-chip debugger data input/output
	PD1	I/O			I/O port
PD2	DCLK	O	O (H)	–	On-chip debugger clock output
	PD2	O			Output port
PD3	PD3	I/O	Hi-Z	–	I/O port
	OSC3	A			OSC3 oscillator circuit input
PD4	PD4	I/O	Hi-Z	–	I/O port
	OSC4	A			OSC3 oscillator circuit output
EXSVD	EXSVD	A	Hi-Z	✓	External power supply voltage detection input
SEG0	SEG0	A	Hi-Z	–	LCD segment output
	COM16	A			LCD common output
SEG1	SEG1	A	Hi-Z	–	LCD segment output
	COM17	A			LCD common output
SEG2	SEG2	A	Hi-Z	–	LCD segment output
	COM18	A			LCD common output
SEG3	SEG3	A	Hi-Z	–	LCD segment output
	COM19	A			LCD common output
SEG4	SEG4	A	Hi-Z	–	LCD segment output
	COM20	A			LCD common output
SEG5	SEG5	A	Hi-Z	–	LCD segment output
	COM21	A			LCD common output
SEG6	SEG6	A	Hi-Z	–	LCD segment output
	COM22	A			LCD common output
SEG7	SEG7	A	Hi-Z	–	LCD segment output
	COM23	A			LCD common output
SEG8	SEG8	A	Hi-Z	–	LCD segment output
	COM24	A			LCD common output
SEG9	SEG9	A	Hi-Z	–	LCD segment output
	COM25	A			LCD common output
SEG10	SEG10	A	Hi-Z	–	LCD segment output
	COM26	A			LCD common output
SEG11	SEG11	A	Hi-Z	–	LCD segment output
	COM27	A			LCD common output
SEG12	SEG12	A	Hi-Z	–	LCD segment output
	COM28	A			LCD common output
SEG13	SEG13	A	Hi-Z	–	LCD segment output
	COM29	A			LCD common output
SEG14	SEG14	A	Hi-Z	–	LCD segment output
	COM30	A			LCD common output
SEG15	SEG15	A	Hi-Z	–	LCD segment output
	COM31	A			LCD common output
SEG16–63	SEG16–63	A	Hi-Z	–	LCD segment outputs
SEG64	SEG64	A	Hi-Z	–	LCD segment output
	COM31	A			LCD common output
SEG65	SEG65	A	Hi-Z	–	LCD segment output
	COM30	A			LCD common output
SEG66	SEG66	A	Hi-Z	–	LCD segment output
	COM29	A			LCD common output
SEG67	SEG67	A	Hi-Z	–	LCD segment output
	COM28	A			LCD common output
SEG68	SEG68	A	Hi-Z	–	LCD segment output
	COM27	A			LCD common output
SEG69	SEG69	A	Hi-Z	–	LCD segment output
	COM26	A			LCD common output

S1C17W34/W35/W36

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
SEG70	SEG70	A	Hi-Z	–	LCD segment output
	COM25	A			LCD common output
SEG71	SEG71	A	Hi-Z	–	LCD segment output
	COM24	A			LCD common output
SEG72	SEG72	A	Hi-Z	–	LCD segment output
	COM23	A			LCD common output
SEG73	SEG73	A	Hi-Z	–	LCD segment output
	COM22	A			LCD common output
SEG74	SEG74	A	Hi-Z	–	LCD segment output
	COM21	A			LCD common output
SEG75	SEG75	A	Hi-Z	–	LCD segment output
	COM20	A			LCD common output
SEG76	SEG76	A	Hi-Z	–	LCD segment output
	COM19	A			LCD common output
SEG77	SEG77	A	Hi-Z	–	LCD segment output
	COM18	A			LCD common output
SEG78	SEG78	A	Hi-Z	–	LCD segment output
	COM17	A			LCD common output
SEG79	SEG79	A	Hi-Z	–	LCD segment output
	COM16	A			LCD common output
COM0–15	COM0–15	A	Hi-Z	–	LCD common outputs

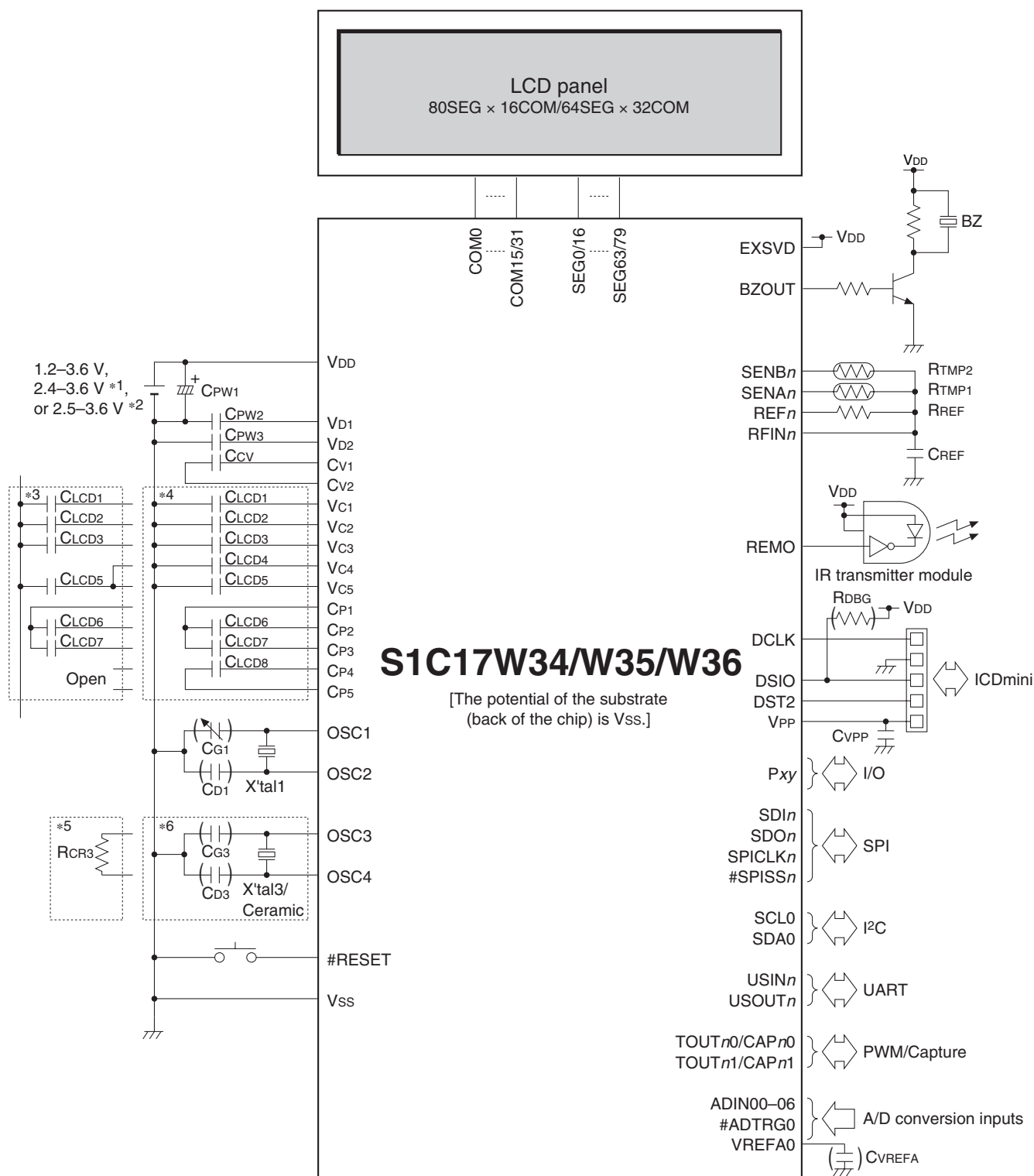
Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number <i>n</i>	Function
Synchronous serial interface (SPIA)	SDIn	I	<i>n</i> = 0, 1	SPIA Ch. <i>n</i> data input
	SDOn	O		SPIA Ch. <i>n</i> data output
	SPICLK <i>n</i>	I/O		SPIA Ch. <i>n</i> clock input/output
	#SPISS <i>n</i>	I		SPIA Ch. <i>n</i> slave-select input
I ² C (I2C)	SCL <i>n</i>	I/O	<i>n</i> = 0	I2C Ch. <i>n</i> clock input/output
	SDA <i>n</i>	I/O		I2C Ch. <i>n</i> data input/output
UART (UART2)	USIN <i>n</i>	I	<i>n</i> = 0, 1	UART2 Ch. <i>n</i> data input
	USOUT <i>n</i>	O		UART2 Ch. <i>n</i> data output
16-bit PWM timer (T16B)	TOUT <i>n</i> 0/CAP <i>n</i> 0	I/O	<i>n</i> = 0, 1, 2	T16B Ch. <i>n</i> PWM output/capture input 0
	TOUT <i>n</i> 1/CAP <i>n</i> 1	I/O		T16B Ch. <i>n</i> PWM output/capture input 1

S1C17W34/W35/W36

■ BASIC EXTERNAL CONNECTION DIAGRAM



- *1: For Flash programming
- *2: For super economy mode/LCD operation
- *3: When 1/4 bias is selected
- *4: When 1/5 bias is selected
- *5: When OSC3 CR oscillator is selected
- *6: When OSC3 crystal/ceramic oscillator is selected
- (): Do not mount components if unnecessary.

S1C17W34/W35/W36

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