

## 3.2Gbps, 4 Differential Channel, Serial ReDriver™ with Equalization, De-emphasis, and Squelch

### Features

- Supports data rates up to 3.2Gbps on each lane
- Optimized for SATA i/m operation
- Adjustable Transmitter De-Emphasis & Amplitude
- Adjustable Receiver Equalization
- Two Spread Spectrum Reference Clock Buffer Outputs
- Optimized for SATA applications
- Input signal level detection & output squelch on all channels
- 100-Ohm Differential CML I/O's
- Low Power (100mW per Channel)
- Standby Mode – Power Down State
- V<sub>DD</sub> Operating Range: 1.5V to 1.8V
- Industrial temperture range
- Packaging (Pb-free & Green): 84-ball LFBGA (NB84)

### Description

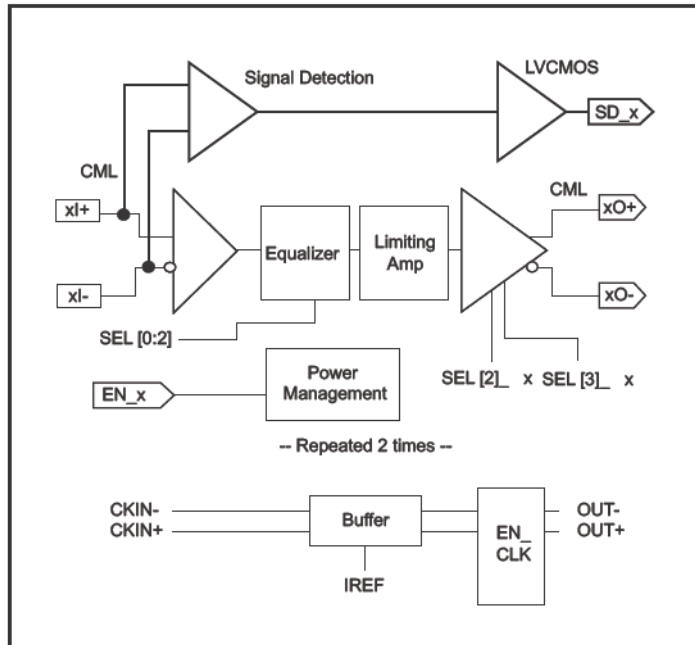
Pericom Semiconductor's PI2EQX3202B is a low power, signal ReDriver™. The device provides programmable equalization, amplification, and de-emphasis by using 7 select bits, SEL[0:6], to optimize performance over a variety of physical mediums by reducing Inter-symbol Interference. PI2EQX3202B supports four 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

A low-level input signal detection and output squelch function is provided for all four channels. Each channel operates fully independently. When a channel is enabled (EN\_x=1) and operating, that channels input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (V<sub>th</sub>-) then the outputs are driven to the common mode voltage.

In addition to providing signal re-conditioning, Pericom's PI2EQX3202B also provides power management Stand-by mode operated by an Enable pin.

### Block Diagram



### Pin Description

|   | 1               | 2               | 3               | 4               | 5      | 6      | 7      | 8               | 9      | 10              |
|---|-----------------|-----------------|-----------------|-----------------|--------|--------|--------|-----------------|--------|-----------------|
| A | SD_C            | SD_D            | SEL0_A          | SEL0_B          | SEL4_A | SEL4_B | SEL6_A | SEL6_B          | EN_A   | EN_B            |
| B | V <sub>DD</sub> | SD_B            | V <sub>DD</sub> | SEL1_A          | SEL2_A | SEL3_A | SEL5_A | V <sub>DD</sub> | EN_C   | V <sub>DD</sub> |
| C | BO+             | SD_A            | AI+             | SEL1_B          | SEL2_B | SEL3_B | SEL5_B | BI+             | EN_D   | AO+             |
| D | BO-             | V <sub>DD</sub> | AI-             | 84-Ball LFBGA   |        |        |        | BI-             | GND    | AO-             |
| E | GND             | V <sub>DD</sub> | GND             |                 |        |        |        | GND             | GND    | GND             |
| F | V <sub>DD</sub> | GND             | V <sub>DD</sub> |                 |        |        |        | V <sub>DD</sub> | GND    | V <sub>DD</sub> |
| G | DO+             | SEL0_C          | CI+             |                 |        |        |        | DI+             | SEL6_C | CO+             |
| H | DO-             | SEL0_D          | CI-             | V <sub>DD</sub> | CKIN+  | CKIN-  | GND    | DI-             | SEL6_D | CO-             |
| J | GND             | SEL1_C          | GND             | SEL2_C          | SEL2_D | SEL3_D | IREF   | GND             | SEL4_D | GND             |
| K | EN_CLK          | SEL1_D          | SEL3_C          | SEL4_C          | OUT0+  | OUT0-  | OUT1+  | OUT1-           | SEL5_C | SEL5_D          |

**Pin Description**

| Pin #                                                         | Pin Name         | I/O | Description                                                                                                                                                                                                                      |
|---------------------------------------------------------------|------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B1, F1, D2, E2,<br>B3, F3, H4, B8,<br>F8, B10, F10            | V <sub>DD</sub>  | PWR | Supply Voltage, 1.5V to 1.8V ± 0.1V                                                                                                                                                                                              |
| C3<br>D3                                                      | AI+<br>AI-       | I   | CML Input Channel A with internal 50Ω pull down                                                                                                                                                                                  |
| E1, J1, F2, E3,<br>J3, H7, E8, J8,<br>D9, E9, F9, E10,<br>J10 | GND              | PWR | Supply Ground                                                                                                                                                                                                                    |
| C8<br>D8                                                      | BI+<br>BI-       | I   | CML Input Channel B with internal 50Ω pull down                                                                                                                                                                                  |
| G3<br>H3                                                      | CI+<br>CI-       | I   | CML Input Channel C with internal 50Ω pull down                                                                                                                                                                                  |
| G8<br>H8                                                      | DI+<br>DI-       | I   | CML Input Channel D with internal 50Ω pull down                                                                                                                                                                                  |
| A3, B4, B5                                                    | SEL[0:2]_A       | I   | Selection pins for equalizer (see Amplifier Configuration Table)<br>w/ 50kΩ internal pull up                                                                                                                                     |
| A4, C4, C5                                                    | SEL[0:2]_B       | I   |                                                                                                                                                                                                                                  |
| G2, J2, J4                                                    | SEL[0:2]_C       | I   |                                                                                                                                                                                                                                  |
| H2, K2, J5                                                    | SEL[0:2]_D       | I   |                                                                                                                                                                                                                                  |
| B6, A5                                                        | SEL[3:4]_A       | I   | Selection pins for amplifier (see Amplifier Configuration Table)<br>w/ 50kΩ internal pull up                                                                                                                                     |
| C6, A6                                                        | SEL[3:4]_B       | I   |                                                                                                                                                                                                                                  |
| K3, K4                                                        | SEL[3:4]_C       | I   |                                                                                                                                                                                                                                  |
| J6, J9                                                        | SEL[3:4]_D       | I   |                                                                                                                                                                                                                                  |
| B7, A7                                                        | SEL[5:6]_A       | I   | Selection pins for De-Emphasis (See De-Emphasis Configuration Table)<br>w/ 50kΩ internal pull up                                                                                                                                 |
| C7, A8                                                        | SEL[5:6]_B       | I   |                                                                                                                                                                                                                                  |
| K9, G9                                                        | SEL[5:6]_C       | I   |                                                                                                                                                                                                                                  |
| K10, H9                                                       | SEL[5:6]_D       | I   |                                                                                                                                                                                                                                  |
| C10<br>D10                                                    | AO+<br>AO-       | O   | CML Output Channel A internal 50Ω pull up to V <sub>DD</sub> during normal operation and 2kΩ when EN_A=0. Drives to output common mode voltage when input is <V <sub>TH-</sub> .                                                 |
| C1<br>D1                                                      | BO+<br>BO-       | O   | CML Output Channel B with internal 50Ω pull up to V <sub>DD</sub> during normal operation and 2kΩ when EN_B=0. Drives to output common mode voltage when input is <V <sub>TH-</sub> .                                            |
| G10<br>H10                                                    | CO+<br>CO-       | O   | CML Output Channel C with internal 50Ω pull up to V <sub>DD</sub> during normal operation and 2kΩ when EN_C=0. Drives to output common mode voltage when input is <V <sub>TH-</sub> .                                            |
| G1<br>H1                                                      | DO+<br>DO-       | O   | CML Output Channel D with internal 50Ω pull up to V <sub>DD</sub> during normal operation and 2kΩ when EN_D=0. Drives to output common mode voltage when input is <V <sub>TH-</sub> .                                            |
| A9, A10, B9, C9                                               | EN_<br>[A,B,C,D] | I   | Active HIGH LVCMOS signal input pins, when HIGH, it enables the CML output. When LOW, it disables the CML output (x0+, x0-) to HI-z state. Both x0+ & x0- outputs will be pulled up to V <sub>DD</sub> by internal 2kΩ resistor. |

(Continued)

| Pin #       | Pin Name                  | I/O | Description                                                                                                                                                                                 |
|-------------|---------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H6<br>H5    | CKIN-<br>CKIN+            | I   | Differential Reference Clock Input                                                                                                                                                          |
| K5<br>K6    | OUT0+,<br>OUT0-           | O   | Differential Reference Clock Outputs                                                                                                                                                        |
| K7<br>K8    | OUT1+,<br>OUT1-           | O   |                                                                                                                                                                                             |
| J7          | IREF                      | O   | External 475Ω resistor connection to set the differential output current                                                                                                                    |
| K1          | EN_CLK                    | I   | Active HIGH LVCMOS signal input pin. When HIGH, it enables the OUTx+/OUTx- outputs. When LOW, it disables these outputs, with 50Ω to ground termination.                                    |
| C2,B2,A1,A2 | SD_A, SD_B,<br>SD_C, SD_D | O   | Signal detect output. Provides a LVCMOS high output when a valid input signal is detected. When low, SD_X indicates that the input signal level is below the signal detect threshold level. |

### Output Swing Control

| SEL3 [A:D] | SEL4 [A:D] | Swing |
|------------|------------|-------|
| 0          | 0          | 1x    |
| 0          | 1          | 0.8x  |
| 1          | 0          | 1.2x  |
| 1          | 1          | 1.4x  |

### Output De-emphasis Adjustment

| SEL5 [A:D] | SEL6 [A:D] | De-emphasis |
|------------|------------|-------------|
| 0          | 0          | 0dB         |
| 0          | 1          | -2.5dB      |
| 1          | 0          | -3.5dB      |
| 1          | 1          | -4.5dB      |

### Equalizer Selection

| SEL0 [A:D] | SEL1 [A:D] | SEL2 [A:D] | Compliance Channel @ 1.6GHz |
|------------|------------|------------|-----------------------------|
| 0          | 0          | 0          | No Equalization             |
| 0          | 0          | 1          | 0.5dB ± 0.5dB               |
| 0          | 1          | 0          | 1.5dB ± 1.0dB               |
| 0          | 1          | 1          | 2.5dB ± 1.0dB               |
| 1          | 0          | 0          | 3.5dB ± 1.0dB               |
| 1          | 0          | 1          | 4.5dB ± 1.0dB               |
| 1          | 1          | 0          | 5.5dB ± 1.0dB               |
| 1          | 1          | 1          | 6.5dB ± 1.0dB               |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

|                                          |                                |
|------------------------------------------|--------------------------------|
| Storage Temperature.....                 | –65°C to +150°C                |
| Supply Voltage to Ground Potential ..... | –0.5V to +2.5V                 |
| DC SIG Voltage .....                     | –0.5V to V <sub>DD</sub> +0.5V |
| Current Output .....                     | –25mA to +25mA                 |
| Power Dissipation Continuous .....       | 800mW                          |
| Operating Temperature.....               | –40 to +85°C                   |

### Note:

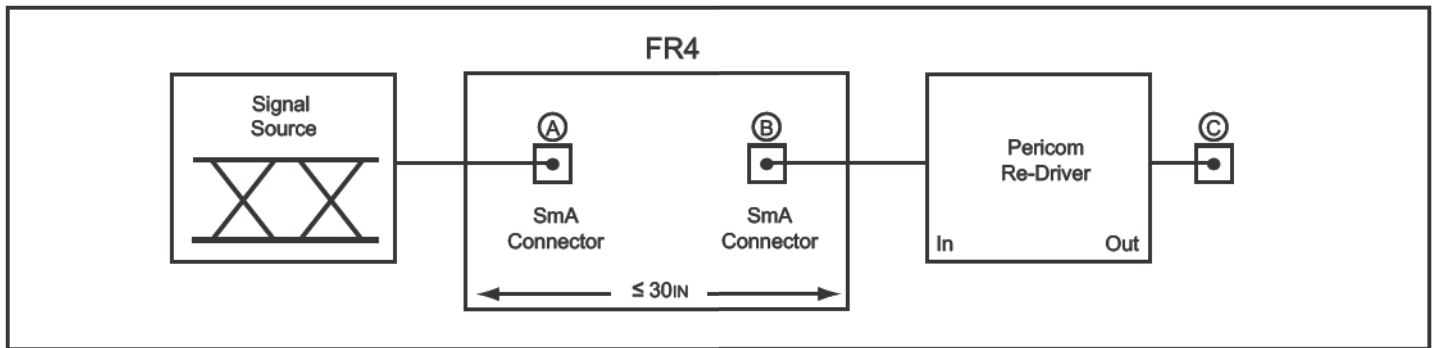
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## AC/DC Electrical Characteristics (V<sub>DD</sub> = 1.4V to 1.9V)

| Symbol                  | Parameter                               | Conditions              | Min.  | Typ. | Max. | Units |
|-------------------------|-----------------------------------------|-------------------------|-------|------|------|-------|
| Ps                      | Supply Power                            | EN = LVCMOS Low         |       |      | 0.1  | W     |
|                         |                                         | EN = LVCMOS High        |       |      | 0.6  |       |
| t <sub>PD</sub>         | Latency                                 | From input to output    |       | 2.0  |      | ns    |
| CML Receiver Input      |                                         |                         |       |      |      |       |
| V <sub>RX-DIFF-P</sub>  | Differential Input Peak-to-peak Voltage |                         | 0.200 |      |      | V     |
| V <sub>RX-CM-ACP</sub>  | AC Peak Common Mode Input Voltage       |                         |       |      | 150  | mV    |
| V <sub>TH-</sub>        | Signal Detect Threshold                 | E <sub>N</sub> X = High | 50    |      | 200  | mVp-p |
| Z <sub>RX-DIFF-DC</sub> | DC Differential Input Impedance         |                         | 80    | 100  | 120  | Ω     |
| Z <sub>RX-DC</sub>      | DC Input Impedance                      |                         | 40    | 50   | 60   |       |
| Equalization            |                                         |                         |       |      |      |       |
| J <sub>RS</sub>         | Residual Jitter <sup>(1,2)</sup>        | Total Jitter            |       |      | 0.3  | Ulp-p |
|                         |                                         | Deterministic jitter    |       |      | 0.2  |       |
| J <sub>RM</sub>         | Random Jitter <sup>(1,2)</sup>          |                         |       | 1.5  |      | psrms |

### Notes

- K28.7 pattern is applied differentially at point A as shown in Figure 1.
- Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.



**Figure 1. Test Condition Referenced in the Electrical Characteristic Table**

#### AC/DC Electrical Characteristics ( $V_{DD} = 1.4V$ to $1.9V$ )

| Symbol                                        | Parameter                                                         | Conditions                                    | Min.                   | Typ.                  | Max.                   | Units  |
|-----------------------------------------------|-------------------------------------------------------------------|-----------------------------------------------|------------------------|-----------------------|------------------------|--------|
| CML Transmitter Output (100-Ohm differential) |                                                                   |                                               |                        |                       |                        |        |
| V <sub>DIFFP</sub>                            | Output Voltage Swing<br>  V <sub>TX-D+</sub> - V <sub>TX-D-</sub> |                                               | 200                    |                       | 600                    | mVp-p  |
| V <sub>TX-DIFFP-P</sub>                       | Output Voltage Swing<br>  V <sub>TX-D+</sub> - V <sub>TX-D-</sub> |                                               | 400 <sup>(2)</sup>     |                       | 1200 <sup>(3)</sup>    | mVp-pd |
| V <sub>TX-C</sub> <sup>(4)</sup>              | Common-Mode Voltage                                               | V <sub>TX-D+</sub> - V <sub>TX-D-</sub>   / 2 |                        | V <sub>DD</sub> - 0.3 |                        |        |
| t <sub>F</sub> , t <sub>R</sub>               | Transition Time                                                   | 20% to 80% <sup>(1)</sup>                     |                        |                       | 150                    | ps     |
| Z <sub>OUT</sub>                              | Output Resistance                                                 | Single-ended                                  | 40                     | 50                    | 60                     | Ω      |
| Z <sub>TX-DIFF-DC</sub>                       | DC Differential TX Impedance                                      |                                               | 80                     | 100                   | 120                    | Ω      |
| C <sub>TX</sub>                               | AC Coupling Capacitor                                             |                                               | 75                     |                       | 200                    | nF     |
| LVCMOS Control Pins                           |                                                                   |                                               |                        |                       |                        |        |
| V <sub>IH</sub>                               | Input High Voltage                                                |                                               | 0.65 × V <sub>DD</sub> |                       | V <sub>DD</sub>        | V      |
| V <sub>IL</sub>                               | Input Low Voltage                                                 |                                               |                        |                       | 0.35 × V <sub>DD</sub> |        |
| I <sub>IH</sub>                               | Input High Current                                                |                                               |                        |                       | 250                    | μA     |
| I <sub>IL</sub>                               | Input Low Current                                                 |                                               |                        |                       | 500                    |        |
| LVCMOS Outputs                                |                                                                   |                                               |                        |                       |                        |        |
| V <sub>OH</sub>                               | Output HIGH Voltage                                               | I <sub>OH</sub> = -10mA                       | V <sub>DD</sub> -0.4   |                       |                        | V      |
| V <sub>OL</sub>                               | Output LOW Voltage                                                | I <sub>OL</sub> = 10mA                        |                        |                       | 0.4                    | V      |

**Note:**

1. Using K28.7 (0011111000) pattern)
2. When 0.8x swing selected
3. When 1.4x swing selected
4. The parameter is determined by device characterization, and is not production tested

### AC Switching Characteristics for Clock Buffer ( $V_{DD} = 1.4$ to $1.9V$ ) <sup>(3)</sup>

| Symbol                              | Parameters                                                            | Min  | Max. | Units | Notes |
|-------------------------------------|-----------------------------------------------------------------------|------|------|-------|-------|
| $T_{rise} / T_{fall}$               | Rise and Fall Time (measured between 0.175V to 0.525V) <sup>(1)</sup> | 125  | 525  | ps    | 1     |
| $\Delta T_{rise} / \Delta T_{fall}$ | Rise and Fall Time Variation                                          |      | 75   |       | 1     |
| $V_{HIGH}$                          | Voltage High including overshoot                                      | 660  | 900  | mV    | 1     |
| $V_{LOW}$                           | Voltage Low including undershoot                                      | -150 |      |       | 1     |
| $V_{CROSS}$                         | Absolute crossing point voltages                                      | -200 | 550  |       | 1     |
| $\Delta V_{CROSS}$                  | Total Variation of Vcross over all edges                              | 200  | 250  |       | 1     |
| $T_{DC}$                            | Duty Cycle (input duty cycle = 50%) <sup>(2)</sup>                    | 45   | 55   | %     | 2     |

#### Notes:

1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ , and 2pF.

### Configuration Test Load Board Termination

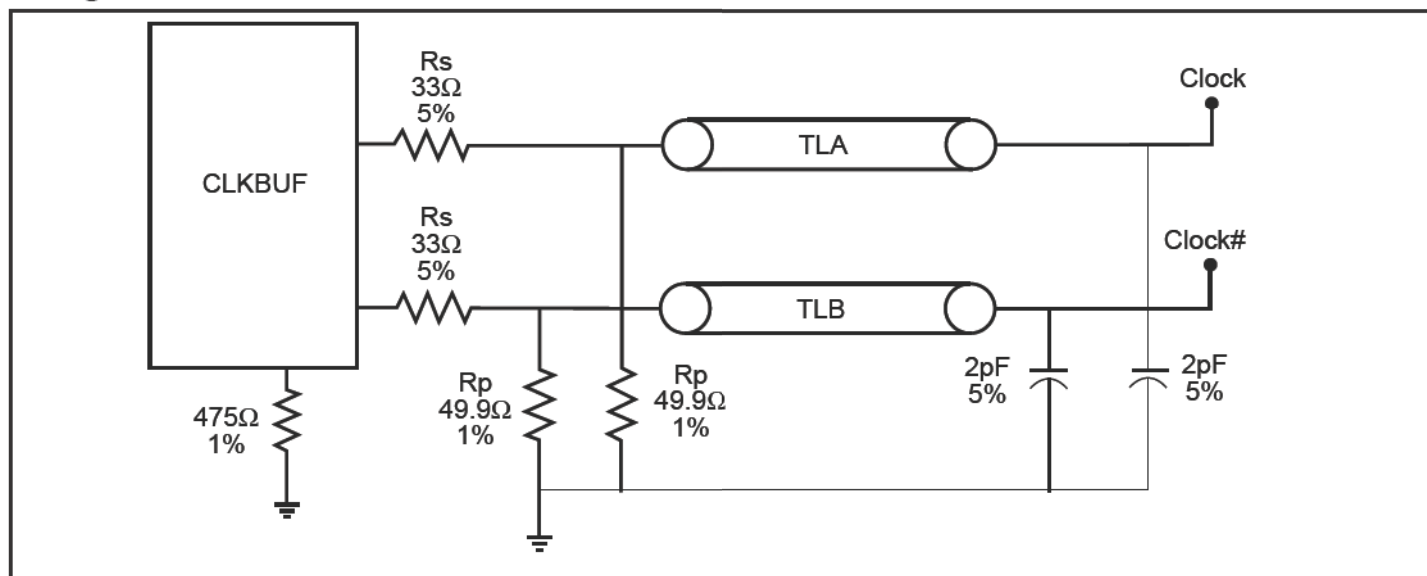
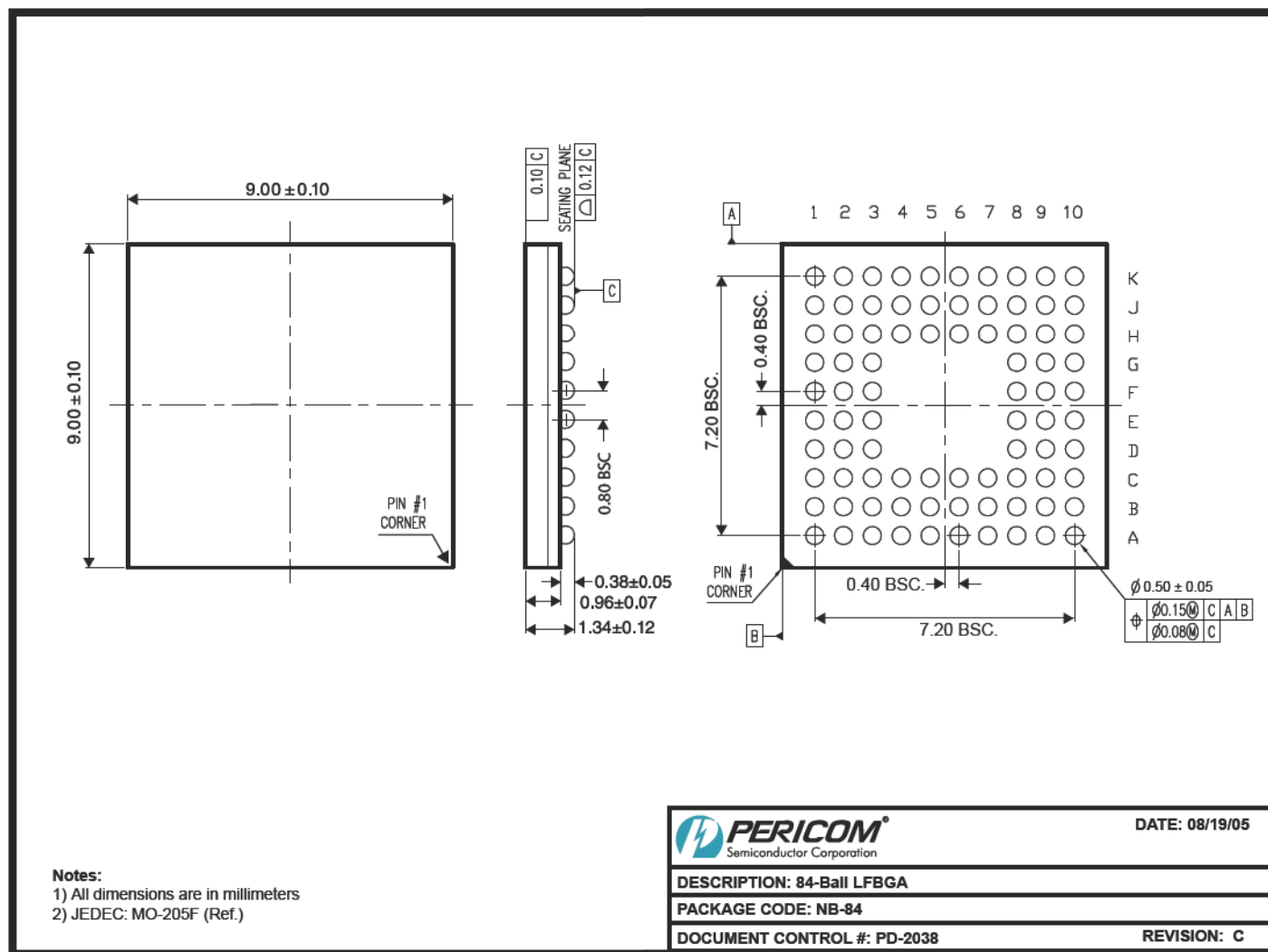


Figure 2. Configuration test load board termination

#### Note:

- TLA and TLB are 3" transmission lines.

## Package Mechanical: 84-ball LFBGA (NB)



05-5338

## Ordering Information

| Ordering Number | Package Code | Package Description           |
|-----------------|--------------|-------------------------------|
| PI2EQX3202BNBE  | NB           | Pb-free & Green 84-Ball LFBGA |

### Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- X suffix = Tape/Reel