

8-Input Data Selector/ Multiplexer with 3-State Outputs High-Performance Silicon-Gate CMOS

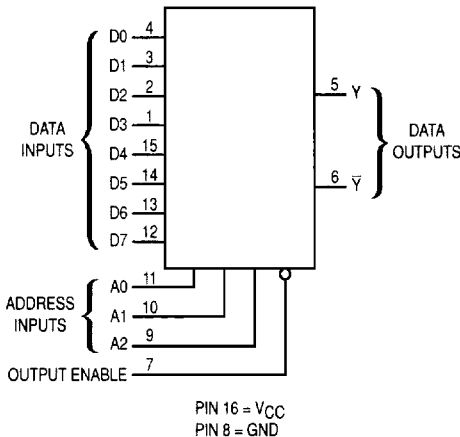
The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the $\bar{Y}$ outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

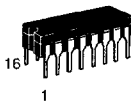
The HC251 is similar in function to the HC151 which does not have 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

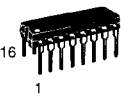
LOGIC DIAGRAM



MC54/74HC251



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

PIN ASSIGNMENT

D3	1	16	V _{CC}
D2	2	15	D4
D1	3	14	D5
D0	4	13	D6
Y	5	12	D7
$\bar{Y}$	6	11	A0
OUTPUT ENABLE	7	10	A1
GND	8	9	A2

FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Output Enable	Y	$\bar{Y}$
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

Z = high impedance
D0, D1, ..., D7 = the level of the respective D input.



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 25	mA
I _{out}	DC Output Current, per Pin	± 50	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C
Ceramic DIP: − 10 mW/°C from 100° to 125°C
SOIC Package: − 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Output Y or $\bar{Y}$ (Figures 1, 2 and 5)	2.0 4.5 6.0	185 37 31	230 46 39	280 56 48	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y or $\bar{Y}$ (Figures 3 and 5)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output $\bar{Y}$ (Figures 4 and 6)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output $\bar{Y}$ (Figures 4 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

CPD	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, VCC = 5.0 V	pF
		36	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

PIN DESCRIPTIONS**INPUTS****D0, D1, ..., D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)**

Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS**A0, A1, A2 (Pins 11, 10, 9)**

Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Output Enable (Pin 7)

Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and $\bar{Y}$ outputs are taken to the high-impedance state.

OUTPUTS**Y, $\bar{Y}$ (Pins 5, 6)**

Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ($\bar{Y}$ output) forms.

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SWITCHING WAVEFORMS

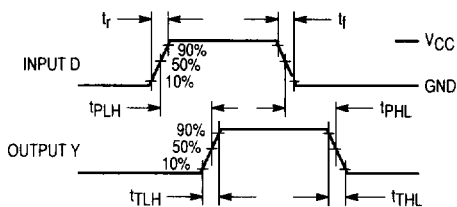


Figure 1.

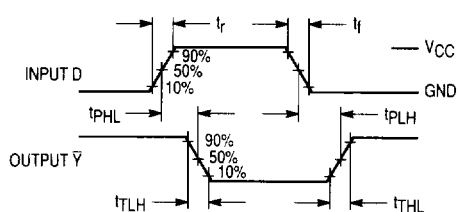


Figure 2.

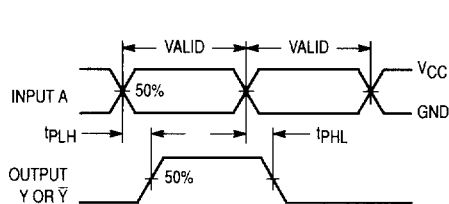


Figure 3.

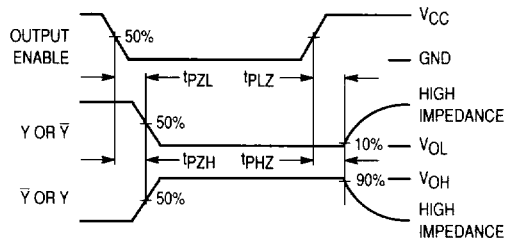
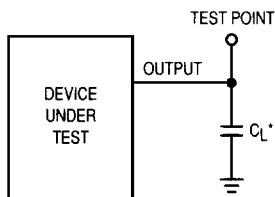


Figure 4.

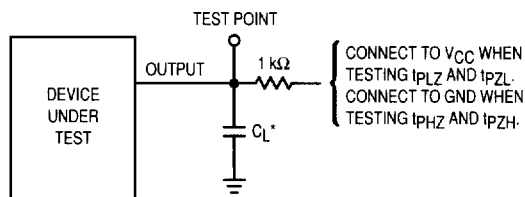
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TEST CIRCUITS



* Includes all probe and jig capacitance

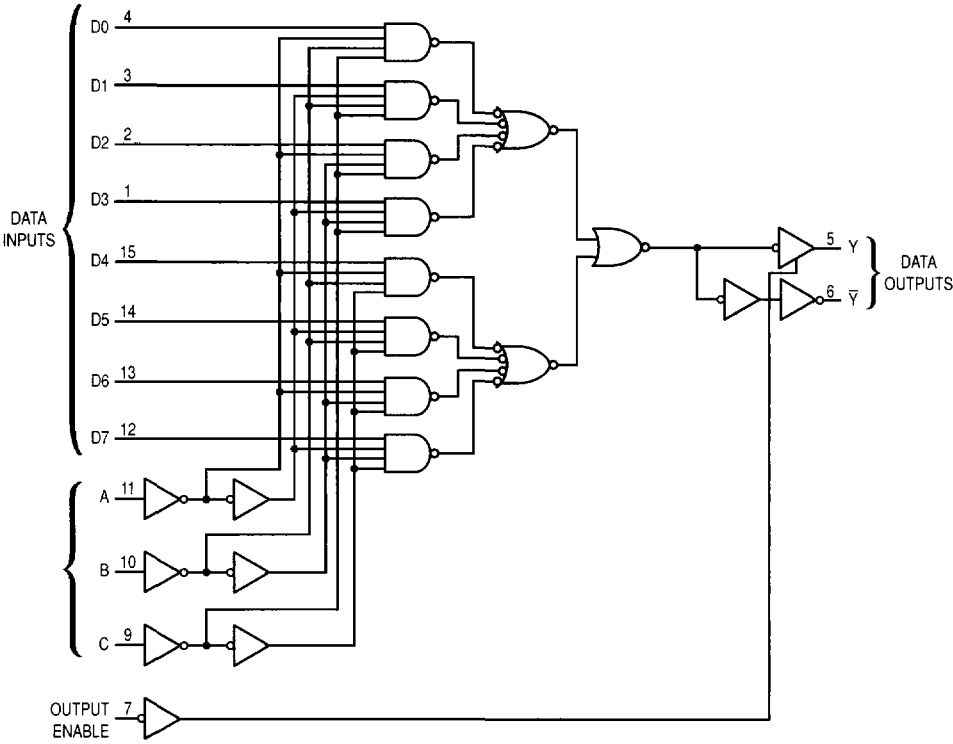
Figure 5.



* Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



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