



# DVI/HDMI 2:4 Low-Frequency Fanout Switch

**MAX4814E**

## General Description

The MAX4814E high-definition multimedia interface (HDMI™) switch provides routing for low-frequency signals. The MAX4814E operates from a single +5.0V  $\pm 10\%$  supply voltage and is ideal for connecting multiple HDMI sources to multiple loads.

The MAX4814E is a bidirectional 2:4 HDMI switch. Each switch consists of five single-pole/single-throw (SPST) channels. Two channels have a low  $3\Omega$  (typ) on-resistance to route +5V and drain (ground return), and three channels to route data. The device features a mode input to control the device through an I<sup>2</sup>C interface or direct-control logic inputs.

The MAX4814E is available in a 64-pin (10mm x 10mm) TQFP package and operates over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  extended temperature range.

## Applications

Commercial/Industrial HDMI/DVI™ (Digital Visual Interface) Switch Boxes

High-End Consumer Switchers

AV Receivers with Switching

HDMI is a trademark of HDMI Licensing, LLC.

DVI is a trademark of Digital Display Working Group.

## Features

- ◆ +5V/Drain Switched
- ◆ HPD (Hot-Plug Detect) Switching
- ◆ DDC (Display Data Channel) Switching
- ◆ Direct Entry or I<sup>2</sup>C Control
- ◆ Low 1 $\mu\text{A}$  Quiescent Current
- ◆  $\pm 6\text{kV}$  Human Body Model (HBM) ESD Protection on Switch I/Os
- ◆ Companion IC to the MAX3845
- ◆ Provides I<sup>2</sup>C Control for the MAX3845
- ◆ Compact 64-Pin, 10mm x 10mm TQFP Package
- ◆ Optimized Layout to Support 4:4 or 2:8 Configuration with Two Devices

## Ordering Information

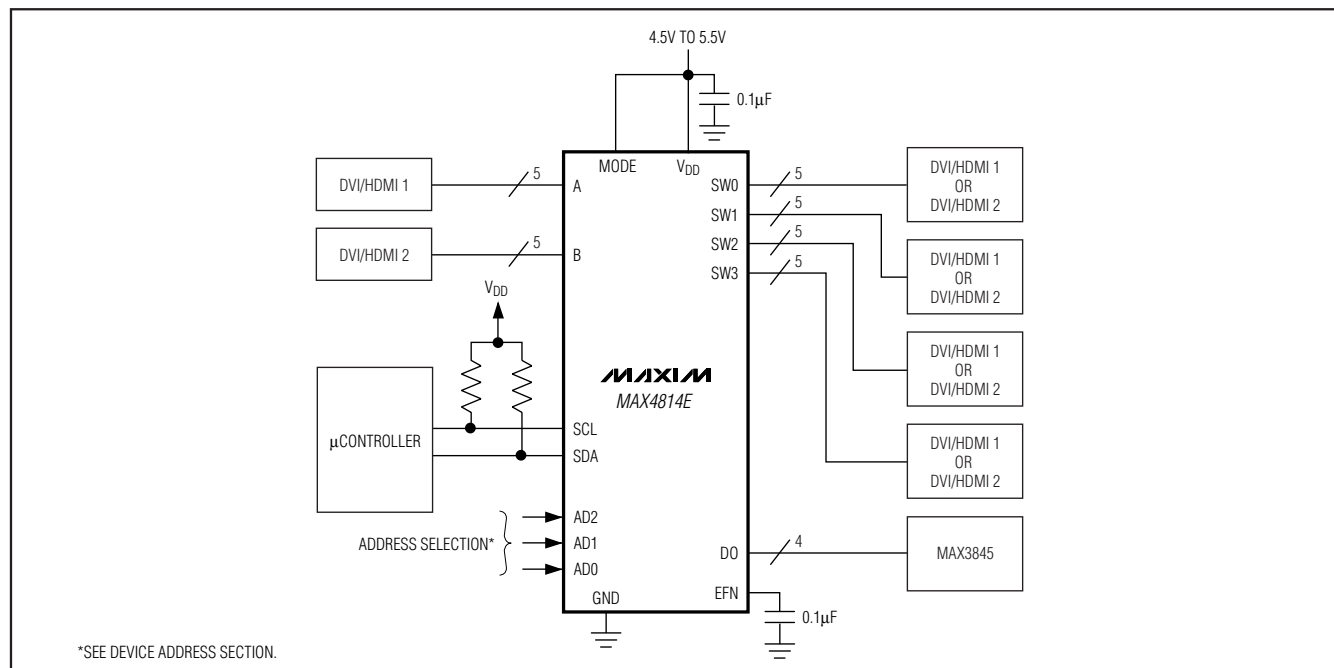
| PART         | TEMP RANGE                                     | PIN-PACKAGE | PKG CODE |
|--------------|------------------------------------------------|-------------|----------|
| MAX4814EECB+ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 64 TQFP-EP* | C64E-10  |

+Denotes a lead-free package.

\*EP = Exposed paddle.

Pin Configuration appears at end of data sheet.

## Typical I<sup>2</sup>C Operating Circuit



# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND. Note 1.)

|                                                                                |                                 |
|--------------------------------------------------------------------------------|---------------------------------|
| V <sub>DD</sub> , A <sub>-</sub> , B <sub>-</sub> , SW <sub>-</sub> , EFN..... | -0.3V to +6.0V                  |
| All Other Pins (except GND).....                                               | -0.3V to V <sub>DD</sub> + 0.3V |
| Continuous Current, A <sub>-</sub> , B <sub>-</sub> .....                      | ±60mA                           |
| Continuous Current, V <sub>DD</sub> or GND.....                                | ±100mA                          |

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

|                                                 |                 |
|-------------------------------------------------|-----------------|
| 64-Pin TQFP (derate 31.3mW/°C above +70°C)..... | 2508mW          |
| Operating Temperature Range .....               | -40°C to +85°C  |
| Junction Temperature .....                      | +150°C          |
| Storage Temperature Range .....                 | -65°C to +150°C |
| Lead Temperature (soldering) .....              | +300°C          |

**Note 1:** EFN must be either connected to V<sub>DD</sub> or left unconnected. EFN must not be connected to ground.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +5V ±10%, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>DD</sub> = +5V. Note 2.)

| PARAMETER                                                                  | SYMBOL            | CONDITIONS                                                                | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------|-------------------|---------------------------------------------------------------------------|-----|-----|-----|------|
| Power-Supply Voltage                                                       | V <sub>DD</sub>   |                                                                           | 4.5 | 5   | 5.5 | V    |
| Power-Supply Current                                                       | I <sub>DD</sub>   | EFN = unconnected; all inputs = 0; all outputs high or low, no loads      |     |     | 10  | μA   |
| EFN Leakage Current                                                        | I <sub>L</sub>    | V <sub>EFN</sub> = V <sub>DD</sub> - 0.2V                                 | -2  |     | +2  | μA   |
| <b>LOGIC INPUTS (DA<sub>-</sub>, DB<sub>-</sub>, MODE, AD<sub>-</sub>)</b> |                   |                                                                           |     |     |     |      |
| Input Low Voltage DA <sub>-</sub> , DB <sub>-</sub>                        | V <sub>IL</sub>   | MODE = 0V                                                                 |     |     | 0.8 | V    |
| Input High Voltage DA <sub>-</sub> , DB <sub>-</sub>                       | V <sub>IH</sub>   | MODE = 0V                                                                 | 2   |     |     | V    |
| Input-Voltage Hysteresis DA <sub>-</sub> , DB <sub>-</sub>                 | V <sub>HYST</sub> | MODE = 0V                                                                 |     | 150 |     | mV   |
| Input Low Voltage AD <sub>-</sub>                                          | V <sub>IL</sub>   | MODE = V <sub>DD</sub>                                                    |     |     | 0.8 | V    |
| Input High Voltage AD <sub>-</sub>                                         | V <sub>IH</sub>   | MODE = V <sub>DD</sub>                                                    | 2   |     |     | V    |
| Input-Voltage Hysteresis AD <sub>-</sub>                                   | V <sub>HYST</sub> | MODE = V <sub>DD</sub>                                                    |     | 150 |     | mV   |
| Input Low Voltage MODE                                                     | V <sub>IL</sub>   |                                                                           |     |     | 0.8 | V    |
| Input High Voltage MODE                                                    | V <sub>IH</sub>   |                                                                           | 2   |     |     | V    |
| Input-Voltage Hysteresis MODE                                              | V <sub>HYST</sub> |                                                                           |     | 150 |     | mV   |
| Input Leakage Current DA <sub>-</sub> , DB <sub>-</sub>                    | I <sub>L</sub>    | MODE = 0V                                                                 |     |     | ±1  | μA   |
| Input Leakage Current AD <sub>-</sub>                                      | I <sub>L</sub>    | MODE = V <sub>DD</sub>                                                    |     |     | ±1  | μA   |
| Input Leakage Current MODE                                                 | I <sub>L</sub>    |                                                                           |     |     | ±1  | μA   |
| <b>LOGIC OUTPUTS DO<sub>-</sub></b>                                        |                   |                                                                           |     |     |     |      |
| Output-Voltage Low                                                         | V <sub>OL</sub>   | MODE = V <sub>DD</sub> , I <sub>SINK</sub> = 30μA                         |     |     | 0.5 | V    |
| Output-Voltage High                                                        | V <sub>OH</sub>   | MODE = V <sub>DD</sub> , I <sub>SOURCE</sub> = 26μA                       | 2   |     |     | V    |
| Output Leakage Current                                                     | I <sub>L</sub>    | MODE = V <sub>DD</sub> , output at high impedance, V <sub>IN</sub> = 1.5V |     |     | ±1  | μA   |
| Output Rise Time                                                           | t <sub>R</sub>    | V <sub>OUT</sub> from 0.8V to 2.2V, C <sub>LOAD</sub> = 10pF              |     | 600 |     | ns   |
| Output Short-Circuit Current                                               | I <sub>SC</sub>   | I <sub>SOURCE</sub>                                                       |     |     | -1  | mA   |
|                                                                            |                   | I <sub>SINK</sub>                                                         |     |     | +3  |      |

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +5V$ . Note 2.)

| PARAMETER                                                                                   | SYMBOL       | CONDITIONS                                                        | MIN | TYP | MAX      | UNIT     |
|---------------------------------------------------------------------------------------------|--------------|-------------------------------------------------------------------|-----|-----|----------|----------|
| <b>ANALOG SWITCHES</b>                                                                      |              |                                                                   |     |     |          |          |
| On-Resistance Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                         | $R_{ON}$     | $V_{IN} = 2.5V$ , $I_{IN} = \pm 10mA$                             |     | 12  |          | $\Omega$ |
| On-Resistance-Flatness Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                | $R_{FLAT}$   | $V_{IN} = 0.8V, 2.5V, 3.7V$                                       |     | 2.5 |          | $\Omega$ |
| On-Channel -3dB Bandwidth Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]             | BW           | $R_S = R_L = 50\Omega$ , $C_L = 35pF$ , Figure 1                  |     | 190 |          | MHz      |
| Off-Isolation Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                         | $V_{ISO}$    | $R_S = R_L = 50\Omega$ , $f = 1MHz$ , Figure 1                    |     | 65  |          | dB       |
| Crosstalk Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                             | $V_{CT}$     | $R_S = R_L = 50\Omega$ , $f = 1MHz$ , Figure 1                    |     | 75  |          | dB       |
| On-Capacitance Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                        | CON          | $V_{DD} = 4.5V$ , $f = 1MHz$ , Figure 2                           |     | 37  |          | pF       |
| Off-Capacitance Standard Switches: A[1], A[2], A[3], B[1], B[2], B[3]                       | COFF         | $V_{DD} = 4.5V$ , $f = 1MHz$ , Figure 2                           |     | 15  |          | pF       |
| Charge Injection                                                                            | Q            | $V_{GEN} = 1.5V$ , $R_{GEN} = 0\Omega$ , $C_L = 100pF$ , Figure 3 |     | 13  |          | pC       |
| On-Resistance +5V/Drain: A[0], A[4], B[0], B[4]                                             | $R_{ON}$     | $V_{DD} = 4.5V$ , $V_{IN} = 0V$ or $V_{DD}$                       |     | 3   |          | $\Omega$ |
| Switch Leakage Current                                                                      | $I_L$        |                                                                   |     |     | $\pm 10$ | $\mu A$  |
| <b>I<sup>2</sup>C SPECIFICATIONS (SDA, SCL, MODE = <math>V_{DD}</math>)</b>                 |              |                                                                   |     |     |          |          |
| Input Low Voltage                                                                           | $V_{IL}$     |                                                                   |     |     | 0.8      | V        |
| Input High Voltage                                                                          | $V_{IH}$     |                                                                   | 2.4 |     |          | V        |
| Input-Voltage Hysteresis                                                                    | $V_{HYST}$   |                                                                   |     | 450 |          | mV       |
| Input Leakage Current                                                                       | $I_L$        |                                                                   |     |     | $\pm 1$  | $\mu A$  |
| Output-Voltage Low SDA                                                                      | $V_{OL}$     | $I_{SINK} = 3mA$                                                  |     |     | 0.4      | V        |
| <b>TIMING CHARACTERISTICS (Figure 4), MODE = <math>V_{DD}</math></b>                        |              |                                                                   |     |     |          |          |
| Serial Clock Frequency                                                                      | $f_{SCL}$    | $V_{DD} = 4.5V$                                                   | 100 | 400 |          | kHz      |
| Hold Time (Repeated) START Condition (after this period the first clock pulse is generated) | $t_{HD,STA}$ | $f_{SCL} = 100kHz$                                                | 4   |     |          | $\mu s$  |
| Low Period of the SCL Clock                                                                 | $t_{LOW}$    | $f_{SCL} = 100kHz$                                                | 4.7 |     |          | $\mu s$  |

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +5V$ . Note 2.)

| PARAMETER                                 | SYMBOL              | CONDITIONS                       | MIN | TYP     | MAX | UNIT          |
|-------------------------------------------|---------------------|----------------------------------|-----|---------|-----|---------------|
| High Period of the SCL Clock              | $t_{\text{HIGH}}$   | $f_{\text{SCL}} = 100\text{kHz}$ | 4   |         |     | $\mu\text{s}$ |
| Setup Time for a Repeated START Condition | $t_{\text{SU,STA}}$ | $f_{\text{SCL}} = 100\text{kHz}$ | 4.7 |         |     | $\mu\text{s}$ |
| Data Hold Time                            | $t_{\text{HD,DAT}}$ | $f_{\text{SCL}} = 100\text{kHz}$ | 25  |         |     | $\mu\text{s}$ |
| Data Setup Time                           | $t_{\text{SU,DAT}}$ | $f_{\text{SCL}} = 100\text{kHz}$ | 250 |         |     | ns            |
| <b>ESD PROTECTION (HUMAN BODY MODEL)</b>  |                     |                                  |     |         |     |               |
| SW_, A_, B_                               | ESD                 | Referenced to GND                |     | $\pm 6$ |     | kV            |
| All Other I/Os                            |                     |                                  |     | $\pm 2$ |     |               |

**Note 2:** Limits at  $T_A = -40^\circ\text{C}$  are guaranteed by design.

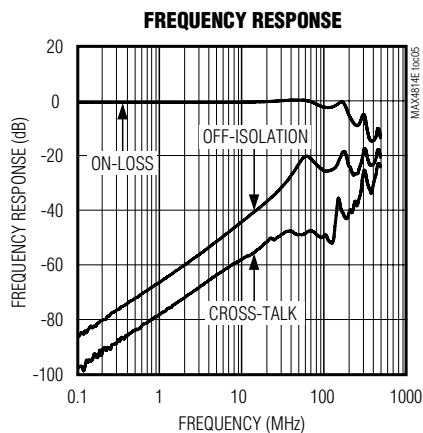
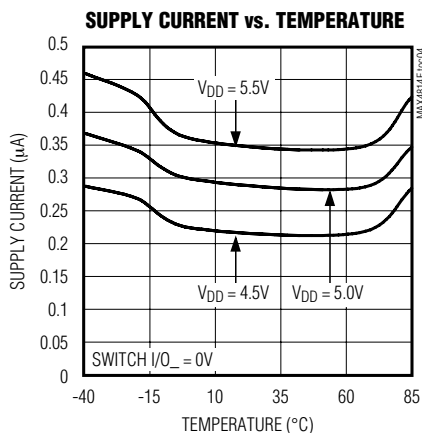
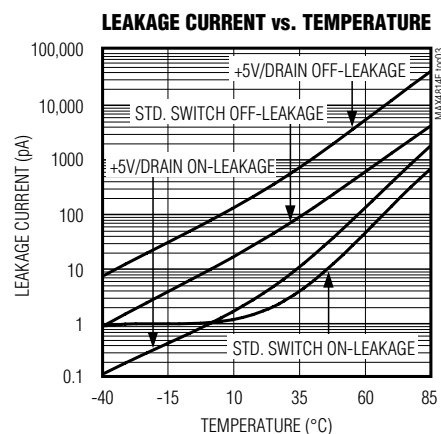
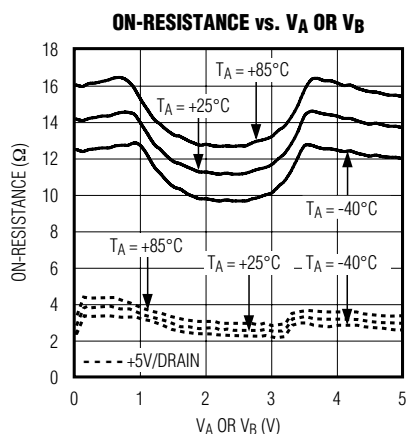
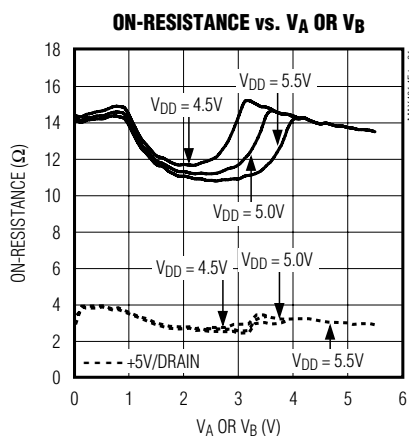
# MAX4814E



# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## Typical Operating Characteristics

( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## Pin Description

MAX4814E

| PIN                           | NAME            | FUNCTION                                                                                                                                                                                  |
|-------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 16, 24, 25, 33, 48, 56, 57 | GND             | Ground. Must connect all GND pins together.                                                                                                                                               |
| 2, 15, 34                     | I.C.            | Internally Connected. Leave I.C. unconnected                                                                                                                                              |
| 3                             | A[0]            | Switch A I/O 0. A[0] has a 3Ω (typ) resistance to switch 5V or drain.                                                                                                                     |
| 4                             | A[1]            | Switch A I/O 1. A[1] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 5                             | A[2]            | Switch A I/O 2. A[2] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 6                             | A[3]            | Switch A I/O 3. A[3] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 7                             | A[4]            | Switch A I/O 4. A[4] has a 3Ω (typ) resistance to switch 5V or drain.                                                                                                                     |
| 8, 9, 17, 32, 40, 41, 49, 64  | V <sub>DD</sub> | Positive-Supply Voltage Input. Connect V <sub>DD</sub> to a +5V supply voltage. Bypass V <sub>DD</sub> to GND with a 0.1μF capacitor. Must connect all V <sub>DD</sub> pins together.     |
| 10                            | B[0]            | Switch B I/O 0. B[0] has a 3Ω (typ) resistance to switch 5V or drain.                                                                                                                     |
| 11                            | B[1]            | Switch B I/O 1. B[1] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 12                            | B[2]            | Switch B I/O 2. B[2] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 13                            | B[3]            | Switch B I/O 3. B[3] has a 12Ω (typ) resistance to switch data.                                                                                                                           |
| 14                            | B[4]            | Switch B I/O 4. B[4] has a 3Ω (typ) resistance to switch 5V or drain.                                                                                                                     |
| 18                            | MODE            | MODE Selection Input. Connect MODE to V <sub>DD</sub> (MODE = 1) to select I <sup>2</sup> C control mode. Connect MODE to GND (MODE = 0) to select direct-control mode.                   |
| 19                            | SDA             | I <sup>2</sup> C-Compatible Serial Data I/O                                                                                                                                               |
| 20                            | SCL             | I <sup>2</sup> C-Compatible Serial Clock Input                                                                                                                                            |
| 21                            | AD0             | Programmable I <sup>2</sup> C Address Bit. AD[0] sets the I <sup>2</sup> C address of the device. User-selectable device address bit, LSB, LSB+1, MSB (see Figure 5).                     |
| 22                            | AD1             | Programmable I <sup>2</sup> C Address Bit. AD[1] sets the I <sup>2</sup> C address of the device. User-selectable device address bit, LSB, LSB+1, MSB (see Figure 5).                     |
| 23                            | AD2             | Programmable I <sup>2</sup> C Address Bit. AD[2] sets the I <sup>2</sup> C address of the device. User-selectable device address bit, LSB, LSB+1, MSB (see Figure 5).                     |
| 26                            | SW3[4]          | Switch 3 I/O 4                                                                                                                                                                            |
| 27                            | SW3[3]          | Switch 3 I/O 3                                                                                                                                                                            |
| 28                            | SW3[2]          | Switch 3 I/O 2                                                                                                                                                                            |
| 29                            | SW3[1]          | Switch 3 I/O 1                                                                                                                                                                            |
| 30                            | SW3[0]          | Switch 3 I/O 0                                                                                                                                                                            |
| 31, 50                        | EFN             | ESD Protection. Connect EFN with an external 0.1μF capacitor to GND for ±15kV ESD HBM protection. The capacitor from EFN to GND provides an additional discharge path for the ESD energy. |
| 35                            | SW2[4]          | Switch 2 I/O 4                                                                                                                                                                            |
| 36                            | SW2[3]          | Switch 2 I/O 3                                                                                                                                                                            |
| 37                            | SW2[2]          | Switch 2 I/O 2                                                                                                                                                                            |
| 38                            | SW2[1]          | Switch 2 I/O 1                                                                                                                                                                            |
| 39                            | SW2[0]          | Switch 2 I/O 0                                                                                                                                                                            |
| 42                            | SW1[4]          | Switch 1 I/O 4                                                                                                                                                                            |
| 43                            | SW1[3]          | Switch 1 I/O 3                                                                                                                                                                            |
| 44                            | SW1[2]          | Switch 1 I/O 2                                                                                                                                                                            |

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## Pin Description (continued)

| PIN | NAME    | FUNCTION                                                                                                                                                                                       |
|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 45  | SW1[1]  | Switch 1 I/O 1                                                                                                                                                                                 |
| 46  | SW1[0]  | Switch 1 I/O 0                                                                                                                                                                                 |
| 47  | N.C.    | No Connection. Not internally connected.                                                                                                                                                       |
| 51  | SW0[4]  | Switch 0 I/O 4                                                                                                                                                                                 |
| 52  | SW0[3]  | Switch 0 I/O 3                                                                                                                                                                                 |
| 53  | SW0[2]  | Switch 0 I/O 2                                                                                                                                                                                 |
| 54  | SW0[1]  | Switch 0 I/O 1                                                                                                                                                                                 |
| 55  | SW0[0]  | Switch 0 I/O 0                                                                                                                                                                                 |
| 58  | DA0/DO0 | Direct-Control Bit I/O. In mode 0, DA0/DO0 is set as an input, DA0, to control switch connections. In mode 1, DA0/DO0 is set as an output, DO0. The output bits are used to drive the MAX3845. |
| 59  | DA1/DO1 | Direct-Control Bit I/O. In mode 0, DA1/DO1 is set as an input, DA1, to control switch connections. In mode 1, DA1/DO1 is set as an output, DO1. The output bits are used to drive the MAX3845. |
| 60  | DA2/DO2 | Direct-Control Bit I/O. In mode 0 DA2/DO2 is set as an input, DA2, to control switch connections. In mode 1, DA2/DO2 is set as an output, DO2. The output bits are used to drive the MAX3845.  |
| 61  | DB0/DO3 | Direct-Control Bit I/O. In mode 0 DB0/DO3 is set as an input, DB0, to control switch connections. In mode 1, DB0/DO3 is set as an output, DO3. The output bits are used to drive the MAX3845.  |
| 62  | DB1     | Direct-Control Bit I/O. In mode 0, DB1 is set as an input. In mode 1, DB1 is high impedance.                                                                                                   |
| 63  | DB2     | Direct-Control Bit I/O. In mode 0, DB2 is set as an input. In mode 1, DB2 is high impedance.                                                                                                   |
| EP  | EP      | Exposed Pad. Connect exposed pad to ground. For enhanced thermal dissipation, connect EP to a copper area as large as possible. Do not use EP as a sole ground connection.                     |

## Detailed Description

The MAX4814E provides routing for low-frequency DVI/HDMI signals. The MAX4814E is a bidirectional 2:4 DVI/HDMI switch. Each switch consists of five single-pole/single-throw (SPST) channels. The channels have a low  $3\Omega$  (typ) on-resistance to route +5V and drain, and three channels to route data. Channels A0, A4, B0, B4, SW\_0, and SW\_4 have a  $3\Omega$  (typ) on-resistance to route +5V and drain, and the remaining channels A1–A3, B1–B3, SL0\_3, and SW\_1 have a  $12\Omega$  (typ) on-resistance to route data. The device features a mode input to control the device using direct-control logic inputs or an I<sup>2</sup>C interface. Connect MODE to GND to control the device using the direct-control bits. Connect MODE to V<sub>DD</sub> to control the device using I<sup>2</sup>C. In I<sup>2</sup>C mode, the MAX4814E controls the MAX3845 (see Figure 5).

## Analog Signal Levels

Signal inputs over the full voltage range (0V to V<sub>DD</sub>) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional. Therefore, switch A<sub>+</sub>, switch B<sub>+</sub>, and switch SW<sub>+</sub> can be either inputs or outputs.

## Switch Control

The MAX4814E features a mode input to control the device through either an I<sup>2</sup>C interface or through direct-control logic inputs. Connect MODE to GND (mode 0) to control the device using the direct-control inputs DA<sub>+</sub> and DB<sub>+</sub> (see Table 1 and Figure 6). Connect MODE to V<sub>DD</sub> (mode 1) to control the device using the I<sup>2</sup>C interface.

## Direct Control Method (Mode 0)

In mode 0, DA0/DO0 becomes input DA0, DA1/DO1

## MAX4814E

MAX4814E



used as the enable for switch A, and DB2 is used as the enable for switch B. Connecting DA2 to V<sub>DD</sub> enables switch A, and connecting DA2 to GND disables switch A. Connecting DB2 to V<sub>DD</sub> enables switch B, and connecting DB2 to GND disables switch B. Inputs DA0 and

used as the enable for switch A, and DB2 is used as the enable for switch B. Connecting DA2 to V<sub>DD</sub> enables switch A, and connecting DA2 to GND disables switch A. Connecting DB2 to V<sub>DD</sub> enables switch B, and connecting DB2 to GND disables switch B. Inputs DA0 and

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

DA1 select the connections of switch A to switch SW\_ and inputs DB0 and DB1. Select the connections of switch B to SW\_. See Table 3a for the pin configuration and Table 3b for a complete summary.

## I<sup>2</sup>C Interface Method (Mode 1)

In mode 1, the switch connections are controlled through the I<sup>2</sup>C interface. Inputs SDA and SCL program registers R0 and R1. Register R0, bits [7 to 2], select the connection of switch A and switch B to switch SW\_ (see the *I<sup>2</sup>C Registers and Bit Descriptions* section).

The bits of register R1 transfer data to the output DO\_. The data on output DO\_ is used to communicate with the MAX3845. In mode 1, DA0/DO0 becomes output DO0, DA1/DO1 becomes output DO1, DA2/DO2 becomes output DO2, and DB0/DO3 becomes output DO3. DB1 and DB2 are high impedance. See Table 3a for the pin configuration. See Table 4 for register R1 to DO\_ output mapping.

## I<sup>2</sup>C Registers and Bit Descriptions

Two internal registers (R0 and R1) program the MAX4814E. Table 2 lists both registers, their addresses, and power-up default states. Both registers are read/write registers.

In register R0, bit BAEN is used as the enable for switch A, and bit BBEN is used as the enable for switch B. Writing 1 to bit BAEN enables switch A; and writing 0 to bit BAEN disables switch A. Writing 1 to bit BBEN enables switch B, and writing 0 to bit BBEN disables switch B. BASEL1 and BASEL0 select the connections of switch A to switch SW\_, while BBSEL1 and BBSEL0

select the connections of switch B to switch SW\_, as summarized in Table 6.

## I<sup>2</sup>C Register R0 Two LSB Bits

The two LSBs are hard coded as 00. Register R0 ignores any value written to the two LSBs; anytime register R0 is read the hard-coded values are returned.

## Bank A Enable (BAEN) and Bank B Enable (BBEN) Bits

1 = Enable

0 = Disable

## Bank A Select (BASEL1/BASEL0) and Bank B Select (BBSEL1/BBSEL0) Bits

Bits BASEL1 and BASEL0 select the switch SW\_ that switch A is connected to. Bits BBSEL1 and BBSEL0 select the switch SW\_ that switch B is connected to (see Table 6).

## Power-On Default States

When power is applied to the MAX4814E internal power-on reset (POR), circuitry sets registers R0 and R1 to their default states. Register R0 is set to all zeros, or 00h, and register R1 is set to 10101010, or AAh, as shown in Table 2.

Having all zeros in register R0 disables both banks A and B; see Table 6 for register R0 to switch mapping. Setting register R1 to AAh forces the outputs at DO\_ to be high impedance.

**Note:** The output, DO\_ is used to communicate with the MAX3845 when the MAX4814E is being used without its companion. The MAX3845 and the MAX4814E use the I<sup>2</sup>C interface (MODE = 1). All DO\_ outputs need to be connected through a 10kΩ resistor to GND.

**Table 1. Mode Configuration**

| INPUT PIN | OPERATION                                                                                                                                                      |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MODE      |                                                                                                                                                                |
| 0         | Puts the device in mode 0. The direct-control inputs DA_ and DB_ control the switches.                                                                         |
| 1         | Puts the device in mode 1. The switches are controlled by the I <sup>2</sup> C interface. DO_ becomes an active output. Inputs DB1 and DB2 are high impedance. |

**Table 2. I<sup>2</sup>C Register Map**

| REGISTER | BIT                      |             |                          |             |                          |             |                          |             | ADDRESS | POWER-UP     |     |
|----------|--------------------------|-------------|--------------------------|-------------|--------------------------|-------------|--------------------------|-------------|---------|--------------|-----|
|          | 7                        | 6           | 5                        | 4           | 3                        | 2           | 1                        | 0           |         | BINARY       | HEX |
| R0       | BBEN                     | BBSEL1      | BBSEL0                   | BAEN        | BASEL1                   | BASEL0      | X                        | X           | 0x00    | 0000<br>0000 | 00  |
| R1       | DO3<br>High<br>Impedance | DO3<br>Data | DO2<br>High<br>Impedance | DO2<br>Data | DO1<br>High<br>Impedance | DO1<br>Data | DO0<br>High<br>Impedance | DO0<br>Data | 0x01    | 1010<br>1010 | AA  |

X = Hardwired code, not programmable by user.

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

**Table 3a. Input/Output Configurations for DA\_, DB\_, and DO\_**

| MODE | PIN CONFIGURATION |             |             |             |                |                |
|------|-------------------|-------------|-------------|-------------|----------------|----------------|
|      | DA0/DO0           | DA1/DO1     | DA2/DO2     | DB0/DO3     | DB1            | DB2            |
| 0    | DA0, Input        | DA1, Input  | DA2, Input  | DB0, Input  | DB1, Input     | DB2, Input     |
| 1    | DO0, Output       | DO1, Output | DO2, Output | DO3, Output | High Impedance | High Impedance |

**Table 3b. Mode 0 Direct-Control Configurations**

| PIN CONNECTION | OPERATION                                                                           |
|----------------|-------------------------------------------------------------------------------------|
| DA2            |                                                                                     |
| 0              | Bank A switches are disabled                                                        |
| 1              | Bank A switches are enabled. Switch A connections depend on the DA0 and DA1 inputs. |

| PIN CONNECTION | OPERATION                                                                           |
|----------------|-------------------------------------------------------------------------------------|
| DB2            |                                                                                     |
| 0              | Bank B switches are disabled                                                        |
| 1              | Bank B switches are enabled. Switch B connections depend on the DB0 and DB1 inputs. |

| PIN CONNECTION |     |     |     | OPERATION        |                     |
|----------------|-----|-----|-----|------------------|---------------------|
| DB1            | DB0 | DA1 | DA0 |                  |                     |
| 0              | 0   | 0   | 0   | Connect A to SW0 | B is high impedance |
| 0              | 0   | 0   | 1   | Connect A to SW1 | Connect B to SW0    |
| 0              | 0   | 1   | 0   | Connect A to SW2 | Connect B to SW0    |
| 0              | 0   | 1   | 1   | Connect A to SW3 | Connect B to SW0    |
| 0              | 1   | 0   | 0   | Connect A to SW0 | Connect B to SW1    |
| 0              | 1   | 0   | 1   | Connect A to SW1 | B is high impedance |
| 0              | 1   | 1   | 0   | Connect A to SW2 | Connect B to SW1    |
| 0              | 1   | 1   | 1   | Connect A to SW3 | Connect B to SW1    |
| 1              | 0   | 0   | 0   | Connect A to SW0 | Connect B to SW2    |
| 1              | 0   | 0   | 1   | Connect A to SW1 | Connect B to SW2    |
| 1              | 0   | 1   | 0   | Connect A to SW2 | B is high impedance |
| 1              | 0   | 1   | 1   | Connect A to SW3 | Connect B to SW2    |
| 1              | 1   | 0   | 0   | Connect A to SW0 | Connect B to SW3    |
| 1              | 1   | 0   | 1   | Connect A to SW1 | Connect B to SW3    |
| 1              | 1   | 1   | 0   | Connect A to SW2 | Connect B to SW3    |
| 1              | 1   | 1   | 1   | Connect A to SW3 | B is high impedance |

**Note:** When switch A and switch B are connected to the same SW\_, switch A takes precedence and switch B is high impedance.

## I<sup>2</sup>C Interface

The MAX4814E features an I<sup>2</sup>C interface using a repeated start. The MAX4814E I<sup>2</sup>C interface refers to the I<sup>2</sup>C bus specification (version 2.1, Jan 2000).

## Device Address

The MAX4814E has selectable device addresses through external inputs. The slave address consists of four fixed bits (B7–B4, set to 0111) followed by three pin-programmable bits (AD2–AD0), as shown on Table 7.

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

**Table 4. I<sup>2</sup>C Register R1 (0X01) to DO\_ Mapping**

| PIN  | REGISTER R1 (0x01) |       |       |       |       |       |       |       | OUTPUT PIN CONFIGURATION |      |
|------|--------------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------|
| MODE | BIT 7              | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |                          |      |
| 1    | —                  | —     | —     | —     | —     | —     | 0     | 0     | DO0                      | 0    |
| 1    | —                  | —     | —     | —     | —     | —     | 0     | 1     | DO0                      | 1    |
| 1    | —                  | —     | —     | —     | —     | —     | 1     | X     | DO0                      | Hi-Z |
|      |                    |       |       |       |       |       |       |       |                          |      |
| 1    | —                  | —     | —     | —     | 0     | 0     | —     | —     | DO1                      | 0    |
| 1    | —                  | —     | —     | —     | 0     | 1     | —     | —     | DO1                      | 1    |
| 1    | —                  | —     | —     | —     | 1     | X     | —     | —     | DO1                      | Hi-Z |
|      |                    |       |       |       |       |       |       |       |                          |      |
| 1    | —                  | —     | 0     | 0     | —     | —     | —     | —     | DO2                      | 0    |
| 1    | —                  | —     | 0     | 1     | —     | —     | —     | —     | DO2                      | 1    |
| 1    | —                  | —     | 1     | X     | —     | —     | —     | —     | DO2                      | Hi-Z |
|      |                    |       |       |       |       |       |       |       |                          |      |
| 1    | 0                  | 0     | —     | —     | —     | —     | —     | —     | DO3                      | 0    |
| 1    | 0                  | 1     | —     | —     | —     | —     | —     | —     | DO3                      | 1    |
| 1    | 1                  | X     | —     | —     | —     | —     | —     | —     | DO3                      | Hi-Z |

X = Don't care.

**Table 5. I<sup>2</sup>C Register R0 (0x00)**

| REGISTER R0 (0x00) |        |        |       |        |        |       |       |
|--------------------|--------|--------|-------|--------|--------|-------|-------|
| BIT 7              | BIT 6  | BIT 5  | BIT 4 | BIT 3  | BIT 2  | BIT 1 | BIT 0 |
| BBEN               | BBSEL1 | BBSEL0 | BAEN  | BASEL1 | BASEL0 | X     | X     |

X = Hardwired, not programmed by user.

For example: If AD0, AD1, and AD2 are hardwired to ground, then the complete address is 0111000. The full address is defined as the seven most significant bits followed by the read/write bit. Set the read/write bit to 1 to configure the MAX4814E to read mode. Set the read/write bit to 0 to configure the MAX4814E to write mode. The address is the first byte of information sent to the MAX4814E after the START condition.

## Applications Information

### ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Switch A, switch B, and switch SW\_ are further protected against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD up to  $\pm 6\text{kV}$  without

damage. The ESD structures withstand high ESD in normal operation, and when the device is powered down. ESD protection can be tested in various ways. The ESD protection of switch A, switch B, and switch SW\_ are characterized for  $\pm 6\text{kV}$  (Human Body Model) using the MIL-STD-883.

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

### Human Body Model

Figure 7 shows the Human Body Model, and Figure 8 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a 1.5k $\Omega$  resistor.

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

Table 6. Switch Selection Truth Table

| DA_, DB_ INPUTS/REGISTER R0 BITS |                |                |              |                |                | SWITCH A AND B TO SW_ CONNECTIONS |             |             |             |             |             |             |             |
|----------------------------------|----------------|----------------|--------------|----------------|----------------|-----------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| DB2/<br>BBEN                     | DB1/<br>BBSEL1 | DB0/<br>BBSEL0 | DA2/<br>BAEN | DA1/<br>BASEL1 | DA0/<br>BASEL0 | B TO<br>SW3                       | B TO<br>SW2 | B TO<br>SW1 | B TO<br>SW0 | A TO<br>SW3 | A TO<br>SW2 | A TO<br>SW1 | A TO<br>SW0 |
| 0                                | X              | X              | 0            | X              | X              | —                                 | —           | —           | —           | —           | —           | —           | —           |
| 0                                | X              | X              | 1            | 0              | 0              | —                                 | —           | —           | —           | —           | —           | —           | 1           |
| 0                                | X              | X              | 1            | 0              | 1              | —                                 | —           | —           | —           | —           | —           | 1           | —           |
| 0                                | X              | X              | 1            | 1              | 0              | —                                 | —           | —           | —           | 1           | —           | —           | —           |
| 0                                | X              | X              | 1            | 1              | 1              | —                                 | —           | —           | —           | 1           | —           | —           | —           |
| 1                                | 0              | 0              | 0            | X              | X              | —                                 | —           | —           | 1           | —           | —           | —           | —           |
| 1                                | 0              | 0              | 1            | 0              | 0              | —                                 | —           | —           | 0           | —           | —           | —           | 1           |
| 1                                | 0              | 0              | 1            | 0              | 1              | —                                 | —           | —           | 1           | —           | —           | 1           | —           |
| 1                                | 0              | 0              | 1            | 1              | 0              | —                                 | —           | —           | 1           | —           | 1           | —           | —           |
| 1                                | 0              | 0              | 1            | 1              | 1              | —                                 | —           | —           | 1           | 1           | —           | —           | —           |
| 1                                | 0              | 1              | 0            | X              | X              | —                                 | —           | 1           | —           | —           | —           | —           | —           |
| 1                                | 0              | 1              | 1            | 0              | 0              | —                                 | —           | 1           | —           | —           | —           | —           | 1           |
| 1                                | 0              | 1              | 1            | 0              | 1              | —                                 | —           | 0           | —           | —           | —           | 1           | —           |
| 1                                | 0              | 1              | 1            | 1              | 0              | —                                 | —           | 1           | —           | —           | 1           | —           | —           |
| 1                                | 0              | 1              | 1            | 1              | 1              | —                                 | —           | 1           | —           | 1           | —           | —           | —           |
| 1                                | 1              | 0              | 0            | X              | X              | —                                 | 1           | —           | —           | —           | —           | —           | —           |
| 1                                | 1              | 0              | 1            | 0              | 0              | —                                 | 1           | —           | —           | —           | —           | —           | 1           |
| 1                                | 1              | 0              | 1            | 0              | 1              | —                                 | 1           | —           | —           | —           | —           | 1           | —           |
| 1                                | 1              | 0              | 1            | 1              | 0              | —                                 | 0           | —           | —           | —           | 1           | —           | —           |
| 1                                | 1              | 0              | 1            | 1              | 1              | —                                 | 1           | —           | —           | 1           | —           | —           | —           |
| 1                                | 1              | 1              | 0            | X              | X              | 1                                 | —           | —           | —           | —           | —           | —           | —           |
| 1                                | 1              | 1              | 0            | X              | X              | 1                                 | —           | —           | —           | —           | —           | —           | 1           |
| 1                                | 1              | 1              | 1            | 0              | 0              | 1                                 | —           | —           | —           | —           | —           | 1           | —           |
| 1                                | 1              | 1              | 1            | 0              | 1              | 1                                 | —           | —           | —           | —           | —           | 1           | —           |
| 1                                | 1              | 1              | 1            | 1              | 0              | 1                                 | —           | —           | —           | —           | 1           | —           | —           |
| 1                                | 1              | 1              | 1            | 1              | 1              | 0                                 | —           | —           | —           | 1           | —           | —           | —           |

— = Denotes no connection.

1 = Denotes switch connection.

0 = Denotes switch B is high impedance.

X = Don't care.

Table 7. MAX4814E Device Address

| B7    | B6 | B5 | B4 | B3            | B2  | B1  | B0  |
|-------|----|----|----|---------------|-----|-----|-----|
| 0     | 1  | 1  | 1  | AD2           | AD1 | AD0 | R/W |
| Fixed |    |    |    | User Selected |     |     | —   |

## Power-Supply Biasing and Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, since stresses beyond the listed ratings can cause permanent damage to the device. Always

sequence V<sub>DD</sub> on first, followed by the switch inputs and the logic inputs. Bypass at least one V<sub>DD</sub> input to ground with a 0.1μF capacitor as close as possible to the device. Use the smallest physical size possible for optimal performance.

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

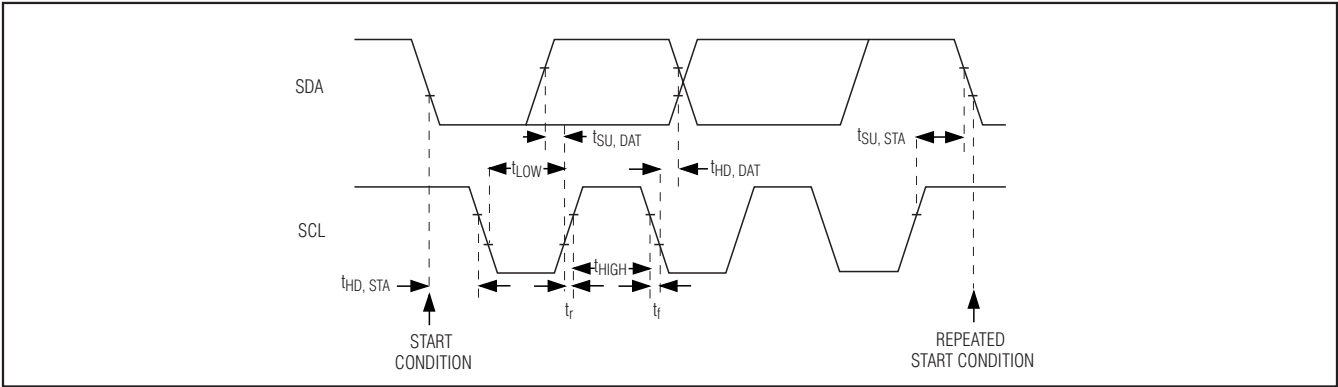


Figure 4. 2-Wire Interface Timing Diagram

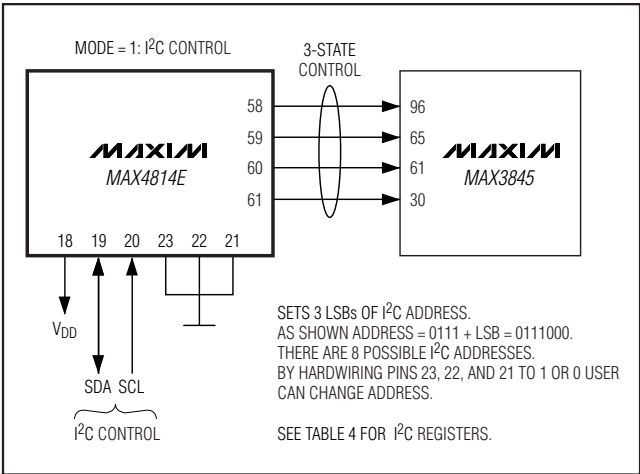


Figure 5. Mode 1: I²C Control

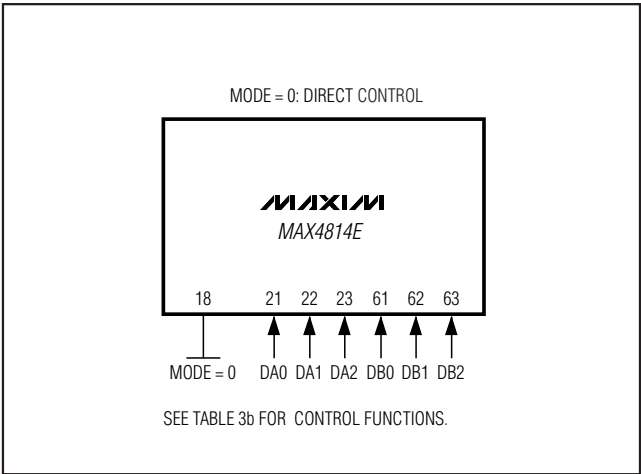


Figure 6. Mode 0: Direct Control

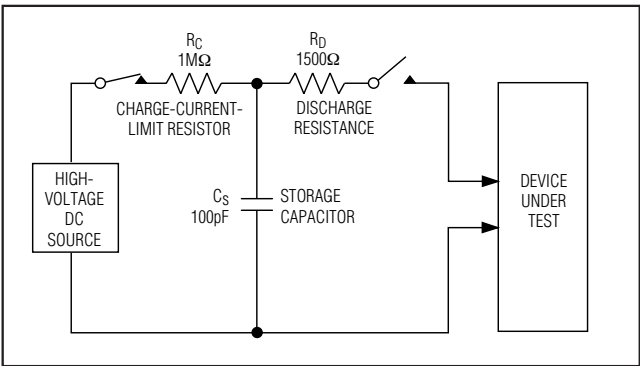


Figure 7. Human Body ESD Test Model

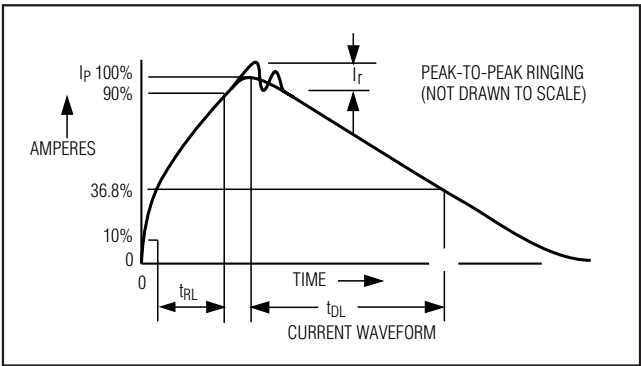
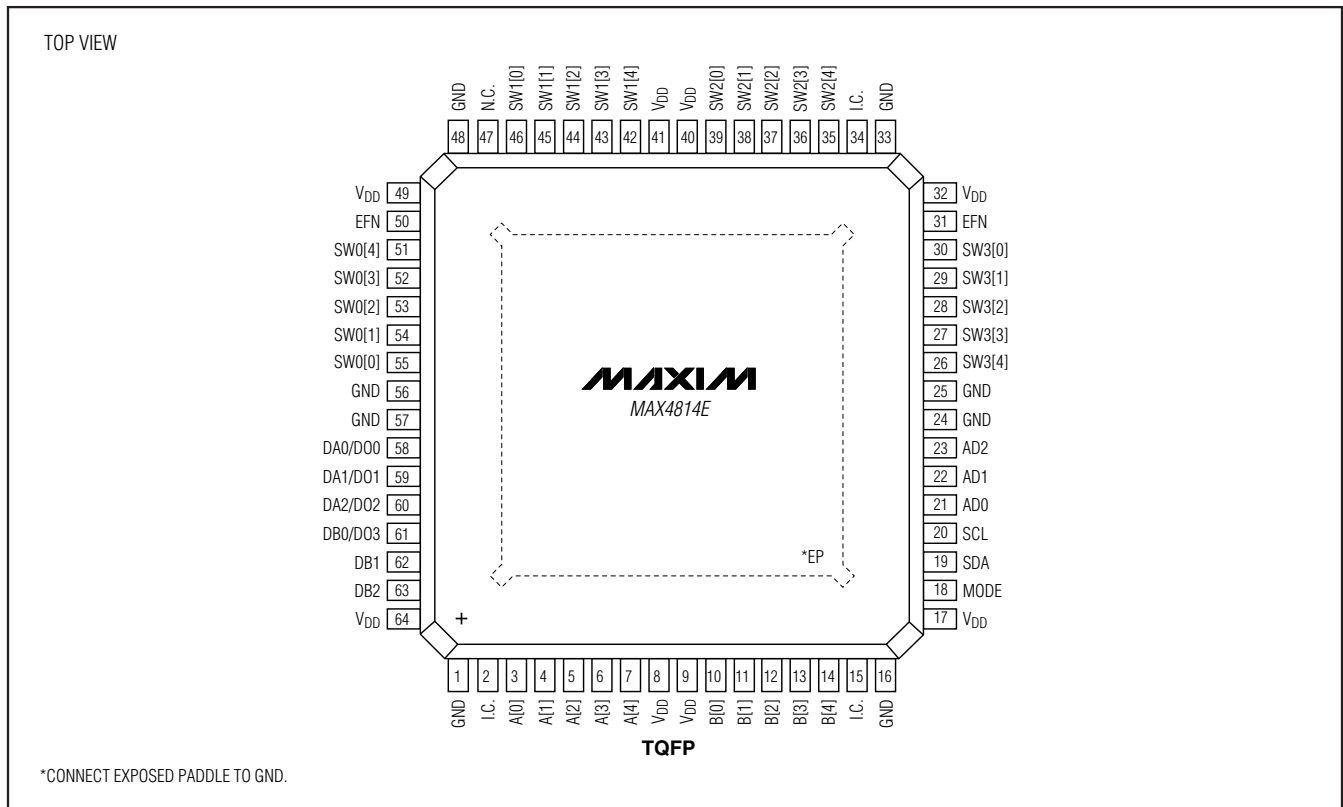


Figure 8. Human Body Current Waveform

# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## Pin Configuration

**MAX4814E**



It is also recommended to bypass more than one  $V_{DD}$  input. A good strategy is to bypass one  $V_{DD}$  input with a  $0.1\mu\text{F}$  capacitor and at least a second  $V_{DD}$  input with a  $1\text{nF}$  to  $10\text{nF}$  capacitor (use a 0603 or smaller physical size ceramic capacitor).

## Chip Information

PROCESS: BiCMOS

# MAX4814E

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# DVI/HDMI 2:4 Low-Frequency Fanout Switch

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

### NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE  $\square-H$  IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION ACD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

| SYMBOL         | JEDEC VARIATION               |       |
|----------------|-------------------------------|-------|
|                | ALL DIMENSIONS IN MILLIMETERS |       |
|                | ACD-HD                        |       |
|                | MIN.                          | MAX.  |
| A              | <i>~</i>                      | 1.20  |
| A <sub>1</sub> | 0.05                          | 0.15  |
| A <sub>2</sub> | 0.95                          | 1.05  |
| D              | 11.80                         | 12.20 |
| D <sub>1</sub> | 9.80                          | 10.20 |
| E              | 11.80                         | 12.20 |
| E <sub>1</sub> | 9.80                          | 10.20 |
| L              | 0.45                          | 0.75  |
| N              | 64                            |       |
| e              | 0.50 BSC.                     |       |
| b              | 0.17                          | 0.27  |
| b <sub>1</sub> | 0.17                          | 0.23  |
| c              | 0.09                          | 0.20  |
| c <sub>1</sub> | 0.09                          | 0.16  |
| X              | 4.70                          | 5.30  |
| Y              | 4.70                          | 5.30  |

-DRAWING NOT TO SCALE-

|                                                                                       |                      |      |     |
|---------------------------------------------------------------------------------------|----------------------|------|-----|
|  |                      |      |     |
| TITLE: PACKAGE OUTLINE,<br>64L TQFP, 10x10x1.0mm EP OPTION                            |                      |      |     |
| APPROVAL                                                                              | DOCUMENT CONTROL NO. | REV. |     |
|                                                                                       | 21-0084              | C    | 2/2 |

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