

January 1998

Fast CMOS 18-Bit Registers
Features

- Advanced 0.6 micron CMOS Technology
- These Devices are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16823T
 - High Output Drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
 - Power Off Disable Outputs Permit "Live Insertion"
 - Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$
- CD74FCT162823T
 - Balanced Output Drivers: $\pm 24mA$
 - Reduced System Switching Noise
 - Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$
- CD74FCT162H823T
 - Bus Hold Retains Last Active Bus State During Three-State
 - Eliminates the Need for External Pull-Up Resistors

Description

These devices are 18-bit wide registers with clock enable ($\overline{XCLKEN}$) and clear ($\overline{XCLR}$) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16823T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162823T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H823T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

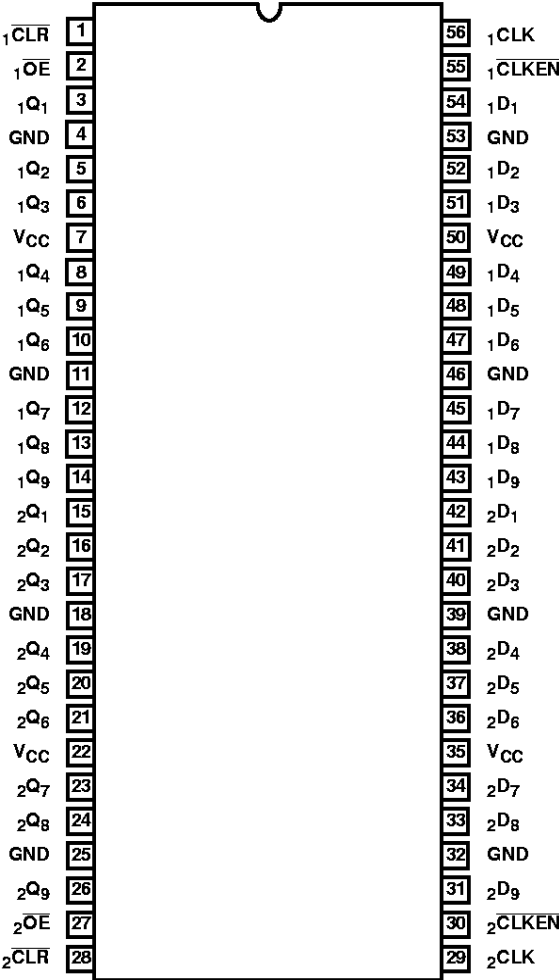
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823ETSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

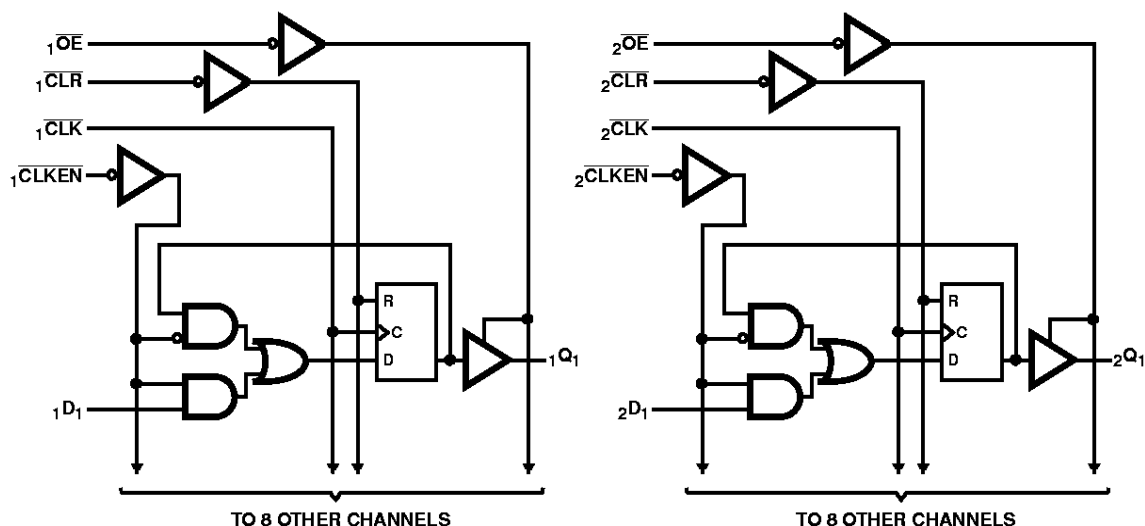
CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T

Pinout

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS
	$\overline{xOE}$	$\overline{xCLR}$	$\overline{xCLKEN}$	$xCLK$	xD_x	xQ_x
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q (Note 2)
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

NOTES:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
2. Output level before indicated steady-state input conditions were established.

Pin Descriptions

PIN NAME	DESCRIPTION
xD_x	Data Inputs (Note 3)
$xCLK$	Clock Inputs
$\overline{xCLKEN}$	Clock Enable Inputs (Active LOW)
$\overline{xCLR}$	Asynchronous Clear Inputs (Active LOW)
$\overline{xOE}$	Output Enable Inputs (Active LOW)
xQ_x	Three-State Outputs

NOTE:

3. For the CD74FCT162H823T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only -0.5V to 7.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
TSSOP Package 85
SSOP Package 70
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(Lead Tips Only)

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%							
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I _{IH}	Standard Input, V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input HIGH Current	I _{IH}	Standard I/O, V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input HIGH Current	I _{IH}	Bus Hold Input (Note 8) V _{CC} = Max	V _{IN} = V _{CC}	-	-	±100	μA
Input HIGH Current	I _{IH}	Bus Hold I/O (Note 8) V _{CC} = Max	V _{IN} = V _{CC}	-	-	±100	μA
Input LOW Current	I _{IL}	Standard Input, V _{CC} = Min	V _{IN} = GND	-	-	-1	μA
Input LOW Current	I _{IL}	Standard I/O, V _{CC} = Min	V _{IN} = GND	-	-	-1	μA
Input LOW Current	I _{IL}	Bus Hold Input (Note 8) V _{CC} = Min	V _{IN} = GND	-	-	±100	μA
Input LOW Current	I _{IL}	Bus Hold I/O (Note 8) V _{CC} = Min	V _{IN} = GND	-	-	±100	μA
Bus Hold Sustain Current	I _{BHH} , I _{BHL}	Bus Hold Input (Note 8) V _{CC} = Min	V _{IN} = 2.0V	-50	-	-	μA
			V _{IN} = 0.8V	50	-	-	μA
High Impedance Output Current (Three-State) (Note 9)	I _{OZH}	V _{CC} = Max	V _{OUT} = 2.7V	-	-	1	μA
	I _{OZL}	V _{CC} = Max	V _{OUT} = 0.5V	-	-	-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 6), V _{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I _O	V _{CC} = Max (Note 6), V _{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V _H			-	100	-	mV
CD74FCT16823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0mA	2.5	3.5	-	V
			I _{OH} = -15.0mA	2.4	3.5	-	V
			I _{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I _{OFF}	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		-	-	±100	μA

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS
CD74FCT162823T, CD74FCT162H823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range						
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0mA	2.4	3.3	- V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	-	0.3	0.55 V
Output LOW Current	I _{ODL}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 7)	60	115	150	mA
Output HIGH Current	I _{ODH}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 7)	-60	-115	-150	mA
CAPACITANCE T _A = 25°C, f = 1MHz						
Input Capacitance (Note 10)	C _{IN}	V _{IN} = 0V	-	4.5	6	pF
Output Capacitance (Note 10)	C _{OUT}	V _{OUT} = 0V	-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS						
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500 μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 11)	-	0.5	1.5 mA
Supply Current per Input per MHz (Note 12)	I _{CCD}	V _{CC} = Max, Outputs Open x _{OE} = x _{CLKEN} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	75	120 μA/MHz
Total Power Supply Current (Note 14)	I _C	V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle x _{OE} = x _{CLKEN} = GND f _I = 5MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	0.8	2.7 mA
			V _{IN} = 3.4V V _{IN} = GND	-	1.3	3.2 mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle x _{OE} = x _{CLKEN} = GND 18 Bits Toggling f _I = 2.5MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	4.2	7.1 (Note 13) mA
			V _{IN} = 3.4V V _{IN} = GND	-	9.2	22.1 (Note 13) mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
Propagation Delay $\overline{XCLK}$ to $\overline{XQX}$	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		$C_L = 300\text{pF}$ (Note 17) $R_L = 500\Omega$	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
Propagation Delay $\overline{XCLR}$ to $\overline{XQX}$	t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
Output Enable Time $\overline{XOE}$ to $\overline{XQX}$	t_{PZH}, t_{PZL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		$C_L = 300\text{pF}$ (Note 17) $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T

Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
Output Disable Time (Note 17) $\overline{XOE}$ to XQ_X	t_{PHZ} , t_{PLZ}	$C_L = 5\text{pF}$ (Note 17) $R_L = 500\Omega$	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
Setup Time HIGH or LOW, XD_X to $XCLK$	t_{SU}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	4.0	-	3.0	-	3.0	-	3.0	-	1.5	-	ns
Hold Time HIGH or LOW, XD_X to $XCLK$	t_H	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2.0	-	1.5	-	1.5	-	1.5	-	0	-	ns
Setup Time HIGH or LOW, $XCLKEN$ to $XCLK$	t_{SU}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	4.0	-	3.0	-	3.0	-	3.0	-	2.5	-	ns
Hold Time HIGH or LOW, $XCLKEN$ to $XCLK$	t_H	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2.0	-	0	-	0	-	0	-	0	-	ns
$XCLK$ Pulse Width HIGH or LOW (Note 17)	t_W	$C_L = 50\text{pF}$ $R_L = 500\Omega$	7.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
$XCLR$ Pulse Width LOW (Note 17)	t_W	$C_L = 50\text{pF}$ $R_L = 500\Omega$	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Recovery Time (Note 17) $XCLR$ to $XCLK$	t_{REM}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Output Skew (Note 18)	$t_{SK(O)}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Pins with Bus Hold are identified in the pin description.
- This specification does not apply to bidirectional functionalities with Bus Hold.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
All currents are in milliamperes and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.