



VND5160AJ-E

Double channel high side driver with analog current sense for automotive applications

Features

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 36V
Max on-state resistance (per ch.)	R_{ON}	160 m Ω
Current limitation (typ)	I_{LIMH}	5 A
Off state supply current	I_S	2 μ A ⁽¹⁾

1. Typical value with all loads connected.

■ General features

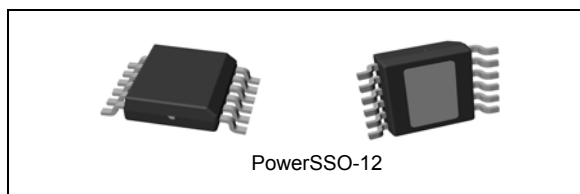
- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive

■ Diagnostic functions

- Proportional load current sense
- High current sense precision for wide range currents
- Current sense disable
- Thermal shutdown indication
- Very low current sense leakage

■ Protection

- Undervoltage shut-down
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shut down



- Reverse battery protection (see [Application schematic](#))
- Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5160AJ-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and Reel
PowerSSO-12	VND5160AJ-E	VND5160AJTR-E

Contents

1	Block diagram and pin description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	18
3	Application information	21
3.1	GND protection network against reverse battery	21
3.1.1	Solution 1 : resistor in the ground line (RGND only)	21
3.1.2	Solution 2 : diode (DGND) in the ground line	22
3.2	Load dump protection	22
3.3	MCU I/Os protection	22
3.4	Maximum demagnetization energy (VCC = 13.5V)	23
4	Package and PC board thermal data	24
4.1	PowerSSO-12™ thermal data	24
5	Package and packing information	27
5.1	ECOPACK® packages	27
5.2	Package mechanical data	27
5.3	Packing information	29
6	Revision history	30

List of tables

Table 1.	Device summary	1
Table 2.	Pin function	5
Table 3.	Suggested connections for unused and N.C. pins	6
Table 4.	Absolute maximum ratings	7
Table 5.	Thermal data	8
Table 6.	Power section	9
Table 7.	Switching (VCC=13V, Tj=25°C)	9
Table 8.	Logic input	10
Table 9.	Protection and diagnostics	10
Table 10.	Current sense (8V<VCC<16V)	11
Table 11.	Truth table.	15
Table 12.	Electrical transient requirements	16
Table 13.	Thermal parameters	26
Table 14.	PowerSSO-12™ mechanical data	28
Table 15.	Document revision history	30

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Current sense delay characteristics	12
Figure 5.	Delay response time between rising edge of output current and rising edge of current sense (CS enabled)	13
Figure 6.	I _{out} /I _{sense} vs. I _{out}	14
Figure 7.	Maximum current sense ratio drift vs load current	14
Figure 8.	Switching characteristics	15
Figure 9.	Output voltage drop limitation	15
Figure 10.	Waveforms	17
Figure 11.	Off state output current	18
Figure 12.	High level input current	18
Figure 13.	Input clamp voltage	18
Figure 14.	Input low level	18
Figure 15.	Input high level	18
Figure 16.	Input hysteresis voltage	18
Figure 17.	On state resistance vs. T _{case}	19
Figure 18.	On state resistance vs. V _{CC}	19
Figure 19.	Undervoltage shutdown	19
Figure 20.	Turn-On voltage slope	19
Figure 21.	I _{LIMH} vs. T _{case}	19
Figure 22.	Turn-Off voltage slope	19
Figure 23.	CS_DIS high level voltage	20
Figure 24.	CS_DIS clamp voltage	20
Figure 25.	CS_DIS low level voltage	20
Figure 26.	Application schematic	21
Figure 27.	Maximum turn-Off current versus inductance (for each channel)	23
Figure 28.	PowerSSO-12™ PC board	24
Figure 29.	R _{thj-amb} vs. PCB copper area in open box free air condition (one channel ON)	24
Figure 30.	PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)	25
Figure 31.	Thermal fitting model of a double channel HSD in PowerSSO-12™	25
Figure 32.	PowerSSO-12™ package dimensions	27
Figure 33.	PowerSSO-12™ tube shipment (no suffix)	29
Figure 34.	PowerSSO-12™ tape and reel shipment (suffix "TR")	29

1 Block diagram and pin description

Figure 1. Block diagram

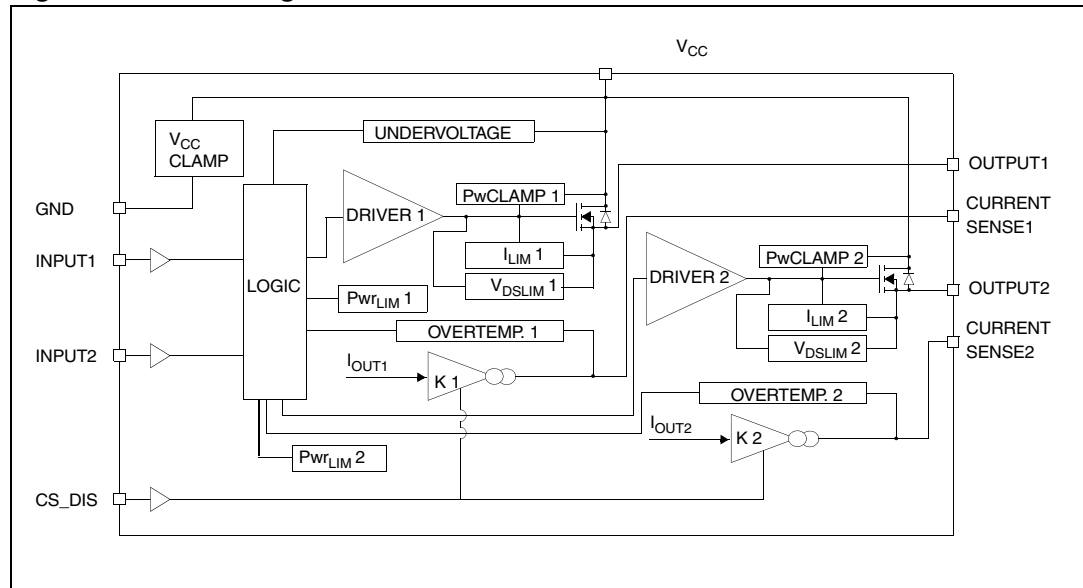
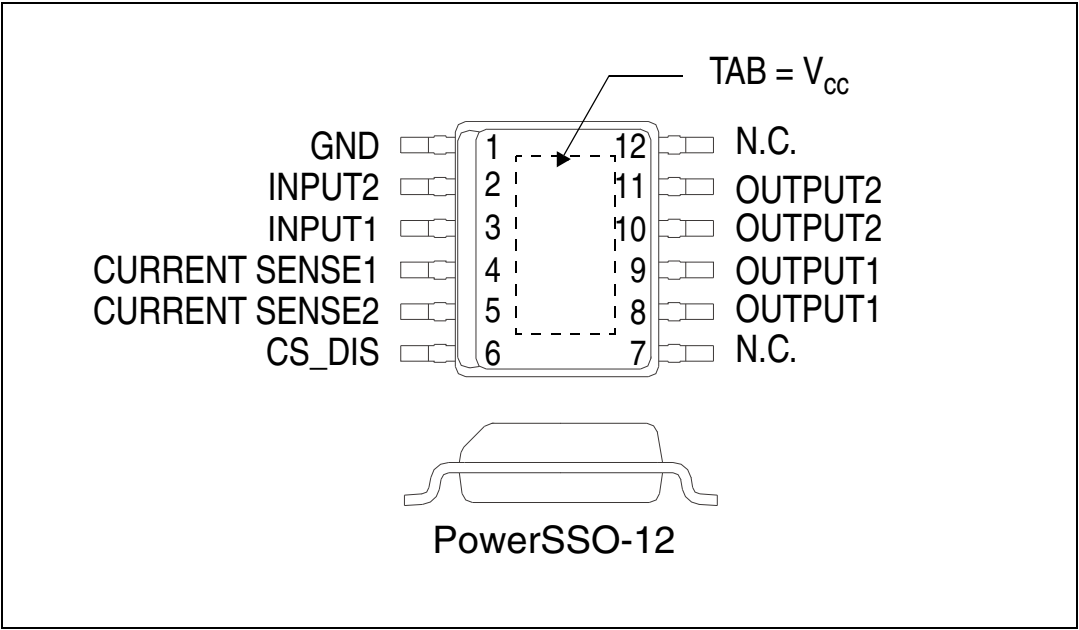


Table 2. Pin function

Name	Function
V _{CC}	Battery connection.
OUTPUT _n	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT _n	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE _n	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)



Note: The above pin configuration reflects the changes notified with PCN-APG-BOD/07/2886. The new pinout is backward compatible with existing PCB layouts where pins #7 and 12 are connected to Vcc. For new PCB designs, these pins should be left unconnected.

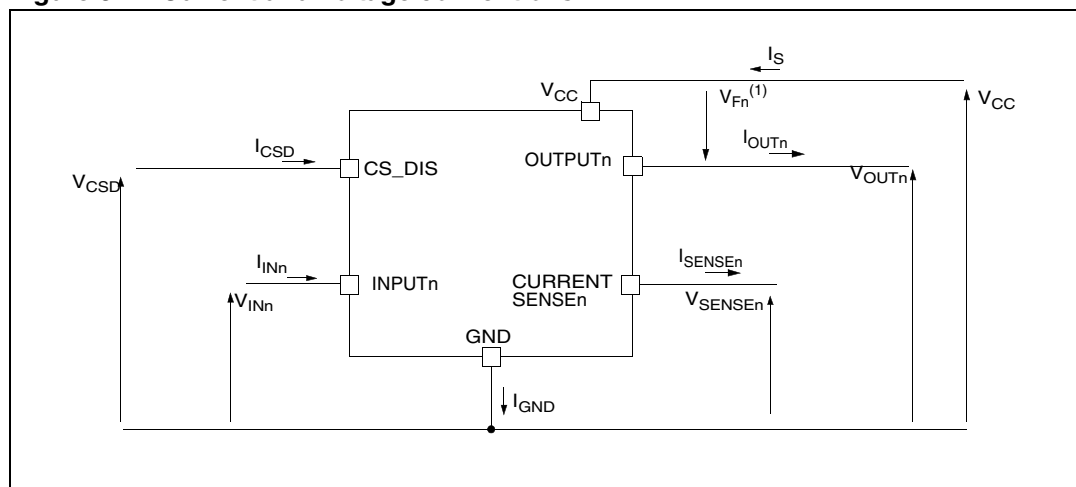
Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. ⁽¹⁾	X	X	X	X
To ground	Through 1kΩ resistor	X	N.R. ⁽¹⁾	Through 10kΩ resistor	Through 10kΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L=12mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_{OUT} = I_{limL}(Typ.)$)	34	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- CS_DIS	4000	V
	- OUTPUT	5000	V
	- V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value	Unit
R _{thj-case}	Thermal resistance junction-case (MAX) (With one channel ON)	8	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (MAX)	See Figure 29	°C/W

2.3 Electrical characteristics

The values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance ⁽¹⁾	$I_{OUT} = 0.5A$; $T_j = 25^{\circ}\text{C}$ $I_{OUT} = 0.5A$; $T_j = 150^{\circ}\text{C}$ $I_{OUT} = 0.5A$; $V_{CC} = 5V$; $T_j = 25^{\circ}\text{C}$			160 320 210	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off State; $V_{CC} = 13V$; $T_j = 25^{\circ}\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$ On State; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		2 ⁽²⁾ 3	5 ⁽²⁾ 6	μA mA
$I_{L(off)}$	Off state output current ⁽¹⁾	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}\text{C}$ $V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}\text{C}$	0 0	0.01	3 5	μA
V_F	Output - V_{CC} diode voltage ⁽¹⁾	$-I_{OUT} = 0.6A$; $T_j = 150^{\circ}\text{C}$			0.7	V

1. For each channel.

2. PowerMOS leakage included.

Table 7. Switching ($V_{CC} = 13V$, $T_j = 25^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn- On delay time	$R_L = 26\Omega$ (see Figure 8.)		10		μs
$t_{d(off)}$	Turn- Off delay time	$R_L = 26\Omega$ (see Figure 8.)		15		μs
$(dV_{OUT}/dt)_{on}$	Turn- On voltage slope	$R_L = 26\Omega$		See Figure 20.		V/μs
$(dV_{OUT}/dt)_{off}$	Turn- Off voltage slope	$R_L = 26\Omega$		See Figure 22.		V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 26\Omega$ (see Figure 8.)		0.03		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 26\Omega$ (see Figure 8.)		0.02		mJ

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1mA$ $I_{CSD} = -1mA$	5.5	-0.7	7	V V

Table 9. Protection and diagnostics⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC} = 13V$ $5V < V_{CC} < 36V$	3.8	5	7.5 7.5	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13V$; $T_R < T_J < T_{TSD}$		2		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}C$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}C$
V_{DEMAG}	Turn-Off output voltage clamp	$I_{OUT} = 1A$; $V_{IN} = 0$; $L = 20mH$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.03A$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ (see Figure 9.)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<VCC<16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	$I_{OUT}=0.025A$; $V_{SENSE}=0.5V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C...150^{\circ}C$	260	500	750	
K_1	I_{OUT}/I_{SENSE}	$I_{OUT}=0.35A$; $V_{SENSE}=0.5V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C...150^{\circ}C$	320	450	590	
		$I_{OUT}=0.35A$; $V_{SENSE}=0.5V$; $V_{CSD}=0V$; $T_j=25^{\circ}C...150^{\circ}C$	360	450	540	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT}=0.35A$; $V_{SENSE}=0.5V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C$ to $150^{\circ}C$	-13		+13	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT}=0.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C...150^{\circ}C$	360	440	540	
		$I_{OUT}=0.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=25^{\circ}C...150^{\circ}C$	380	440	510	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT}=0.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C$ to $150^{\circ}C$	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT}=1.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C...150^{\circ}C$	410	440	480	
		$I_{OUT}=1.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=25^{\circ}C...150^{\circ}C$	420	440	460	
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT}=1.5A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C$ to $150^{\circ}C$	-4		+4	%
I_{SENSE0}	Analog sense leakage current	$I_{OUT}=0A$; $V_{SENSE}=0V$; $V_{CSD}=5V$; $V_{IN}=0V$; $T_j=-40^{\circ}C...150^{\circ}C$	0		1	μA
		$V_{CSD}=0V$; $V_{IN}=5V$; $T_j=-40^{\circ}C...150^{\circ}C$	0		2	μA
		$I_{OUT}=0.6A$; $V_{SENSE}=0V$; $V_{CSD}=5V$; $V_{IN}=5V$; $T_j=-40^{\circ}C...150^{\circ}C$	0		1	μA
I_{OL}	Openload ON state current detection threshold	$V_{IN}=5V$, $I_{SENSE}=5\mu A$	1		5	mA
V_{SENSE}	Max analog sense output voltage	$I_{OUT}=1.5A$; $V_{CSD}=0V$;	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{CC}=13V$; $R_{SENSE}=3.9K\Omega$;		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	$V_{CC}=13V$; $V_{SENSE}=5V$;		8		mA

Table 10. Current sense (8V<VCC<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	$V_{\text{SENSE}} < 4\text{V}$, $0.08\text{A} < I_{\text{out}} < 1.5\text{A}$ $I_{\text{SENSE}} = 90\%$ of $I_{\text{SENSE max}}$ (see Figure 4.)		50	100	μs
t_{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	$V_{\text{SENSE}} < 4\text{V}$, $0.08\text{A} < I_{\text{out}} < 1.5\text{A}$ $I_{\text{SENSE}} = 10\%$ of $I_{\text{SENSE max}}$ (see Figure 4.)		5	20	μs
t_{DSENSE2H}	Delay response time from rising edge of INPUT pin	$V_{\text{SENSE}} < 4\text{V}$, $0.08\text{A} < I_{\text{out}} < 1.5\text{A}$ $I_{\text{SENSE}} = 90\%$ of $I_{\text{SENSE max}}$ (see Figure 4.)		80	150	μs
$\Delta t_{\text{DSENSE2H}}$	Delay response time between rising edge of output current and rising edge of current sense	$V_{\text{SENSE}} < 4\text{V}$, $I_{\text{SENSE}} = 90\%$ of I_{SENSEMAX} , $I_{\text{OUT}} = 90\%$ of I_{OUTMAX} $I_{\text{OUTMAX}} = 2\text{A}$ (see Figure 5)			20	μs
t_{DSENSE2L}	Delay response time from falling edge of INPUT pin	$V_{\text{SENSE}} < 4\text{V}$, $0.08\text{A} < I_{\text{out}} < 1.5\text{A}$ $I_{\text{SENSE}} = 10\%$ of $I_{\text{SENSE max}}$ (see Figure 4.)		100	250	μs

1. Parameter guaranteed by design; it is not tested.

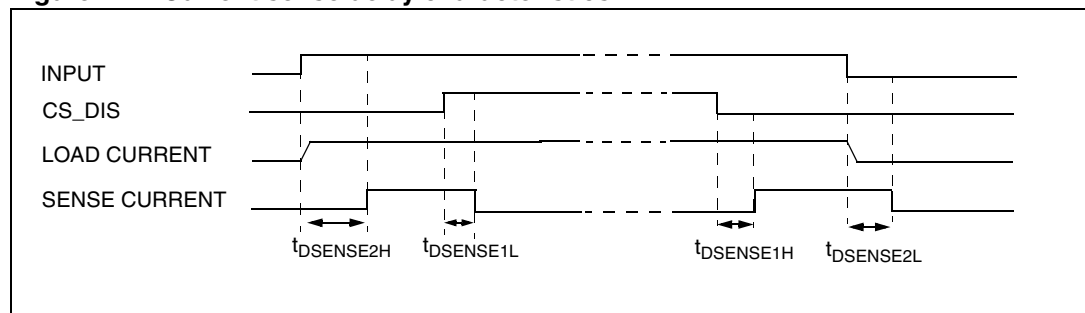
Figure 4. Current sense delay characteristics

Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

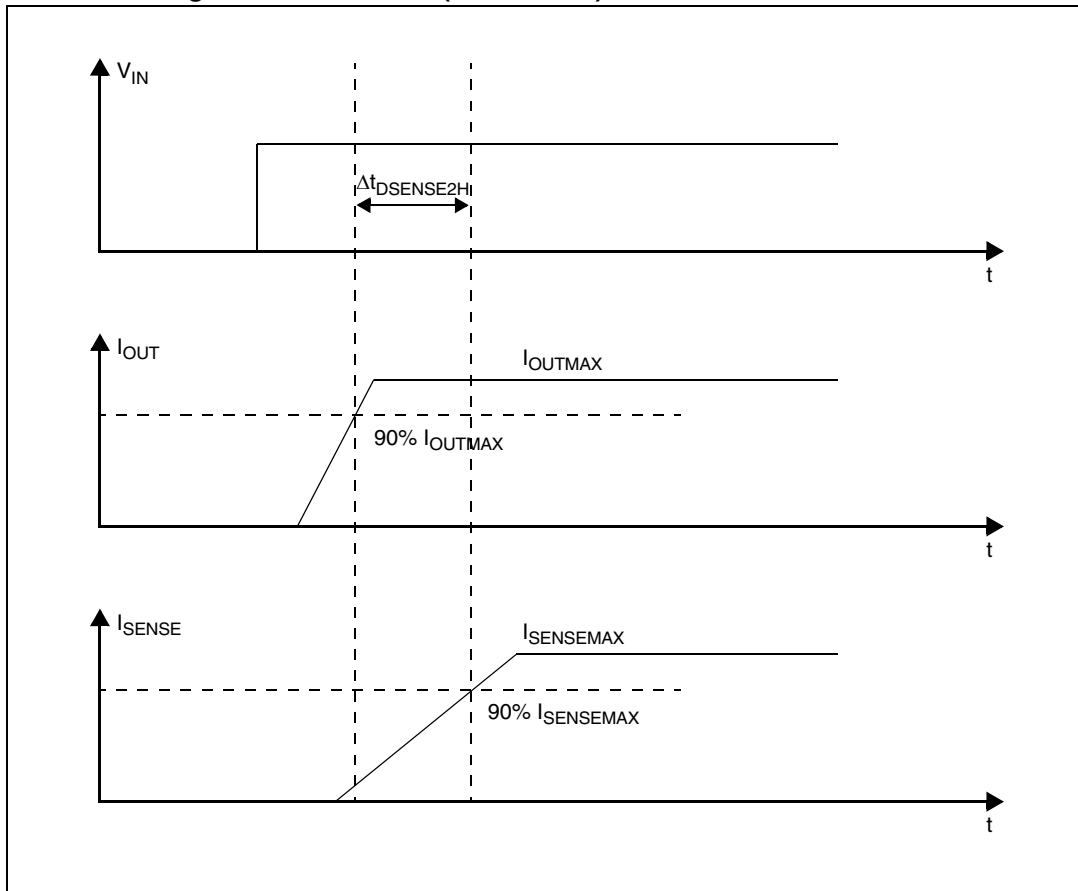


Figure 6. I_{out} / I_{sense} vs. I_{out} (see Table 10 for details)

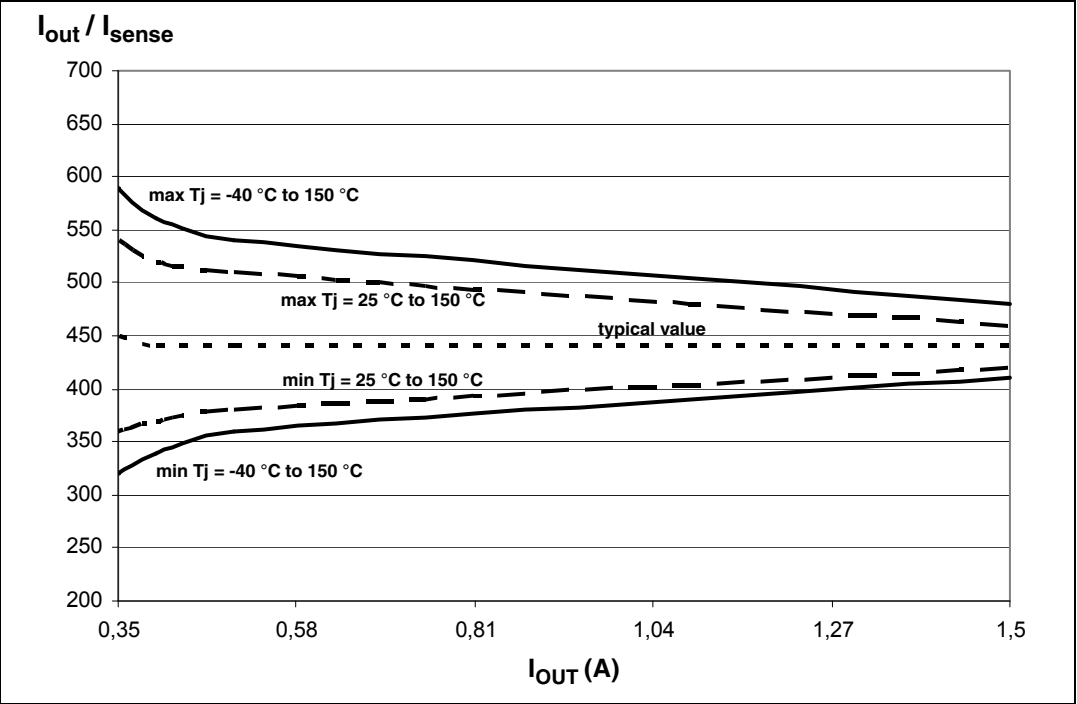
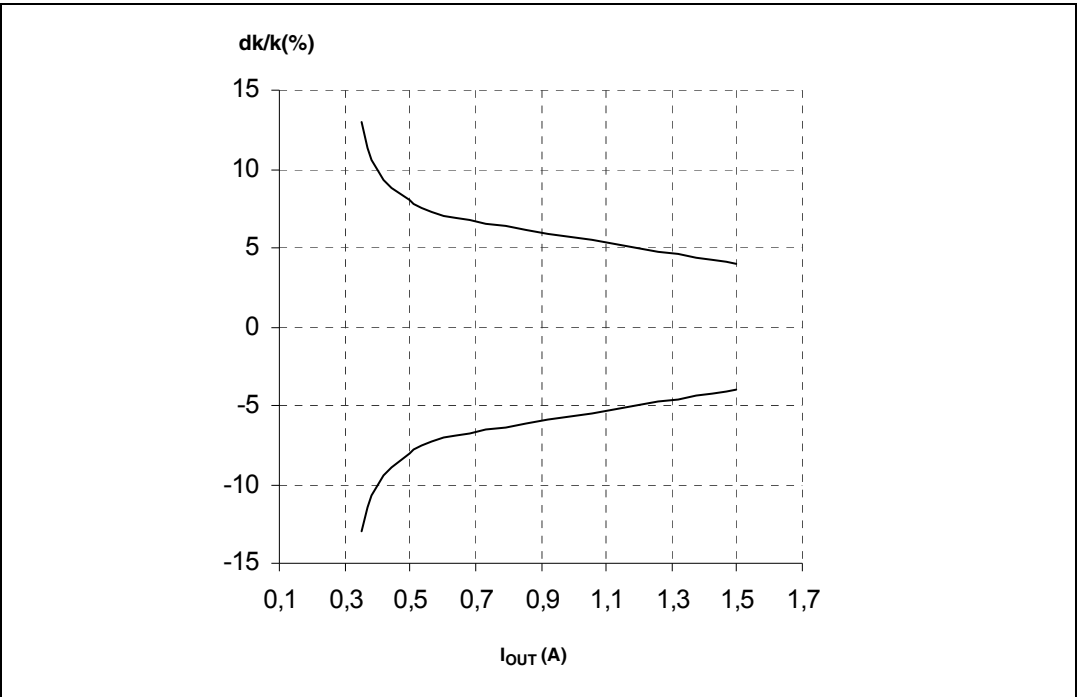


Figure 7. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	INPUT	OUTPUT	SENSE ($V_{CSD}=0V$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ($R_{SC} \leq 10\text{ m}\Omega$)	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

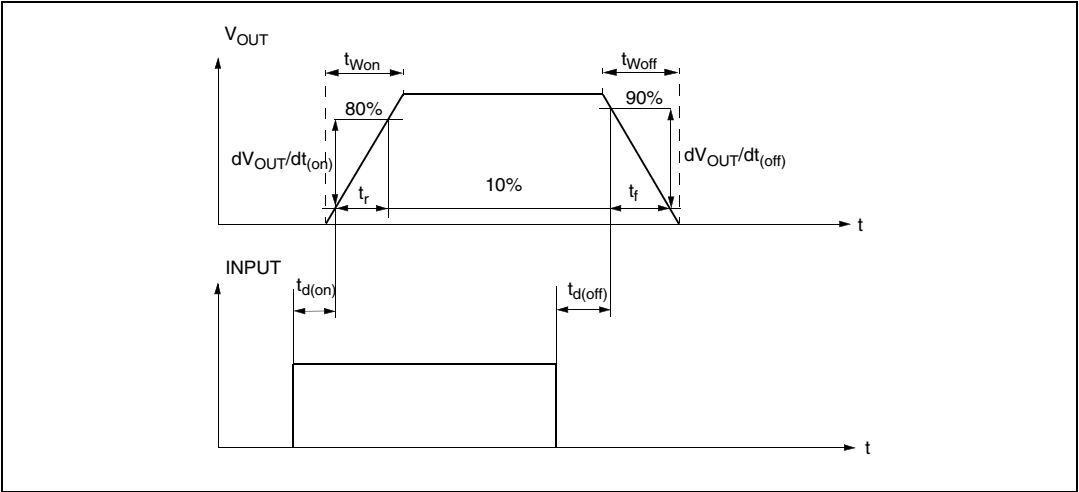


Figure 9. Output voltage drop limitation

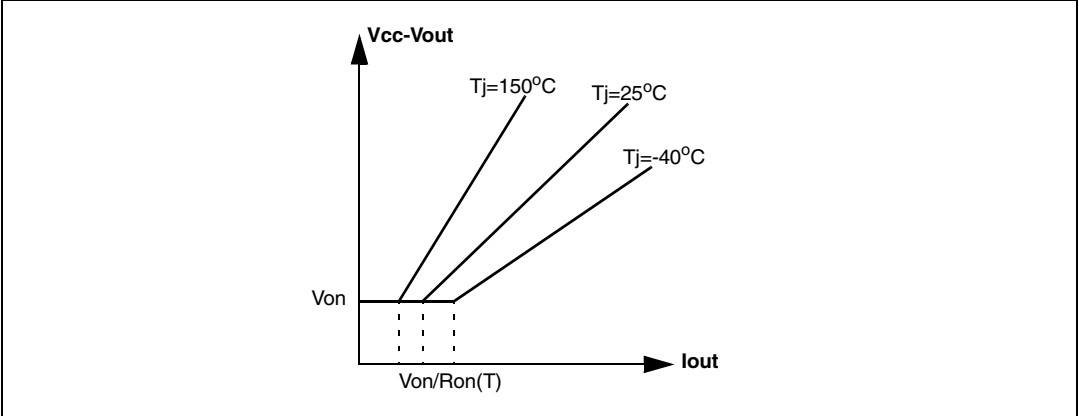


Table 12. Electrical transient requirements

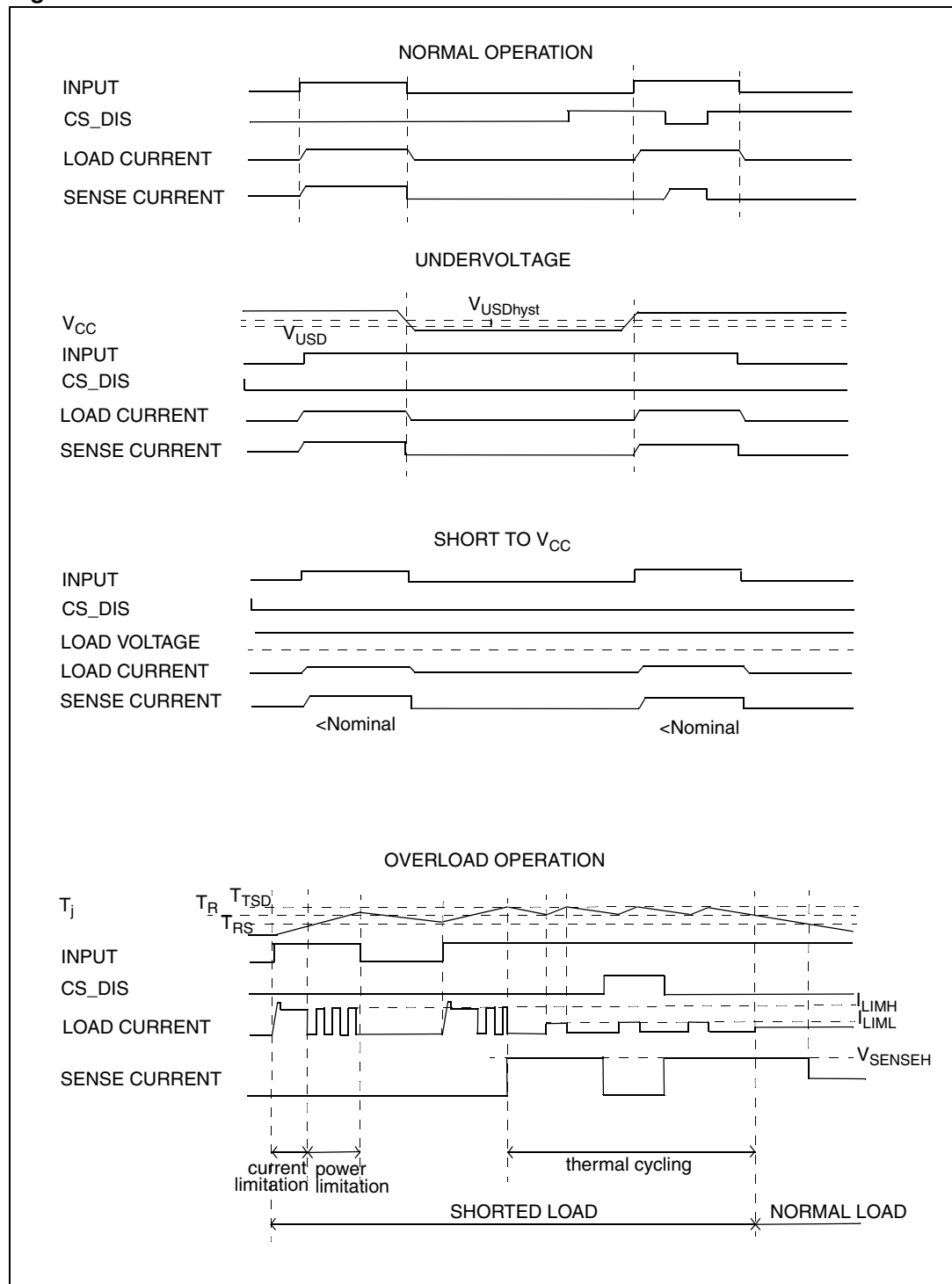
ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off state output current

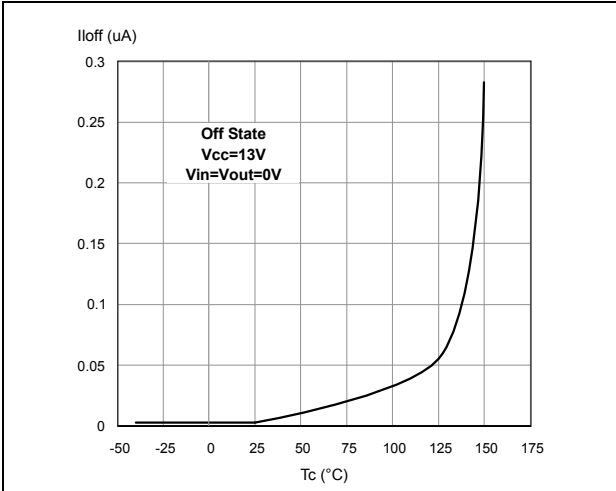


Figure 12. High level input current

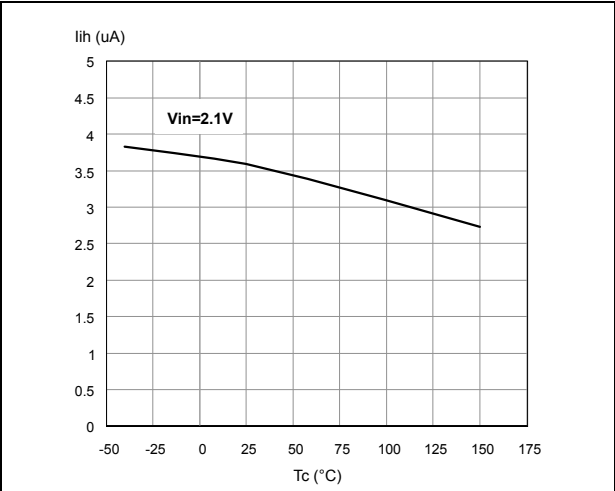


Figure 13. Input clamp voltage

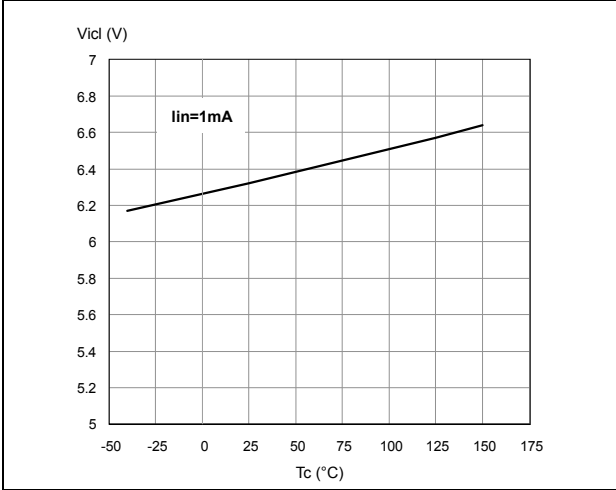


Figure 14. Input low level

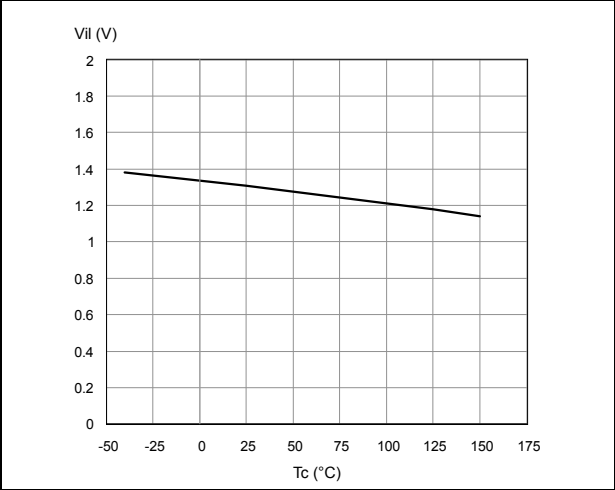


Figure 15. Input high level

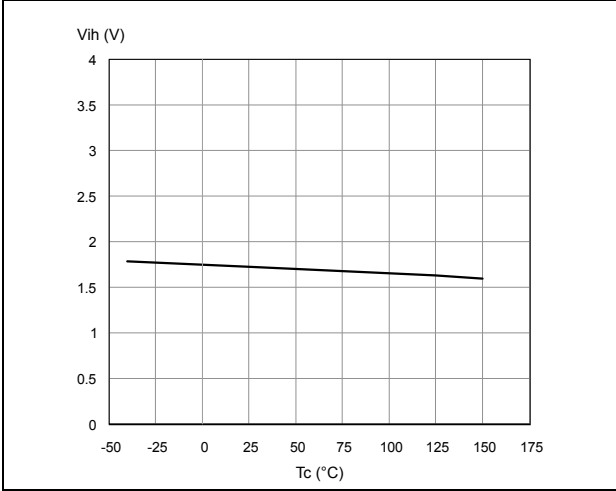


Figure 16. Input hysteresis voltage

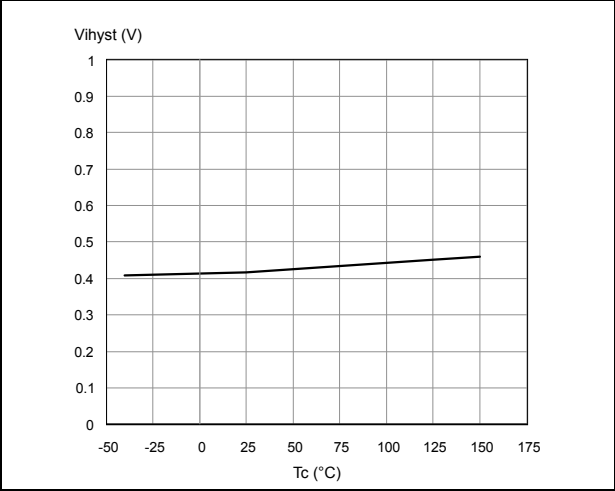


Figure 17. On state resistance vs. T_{case}

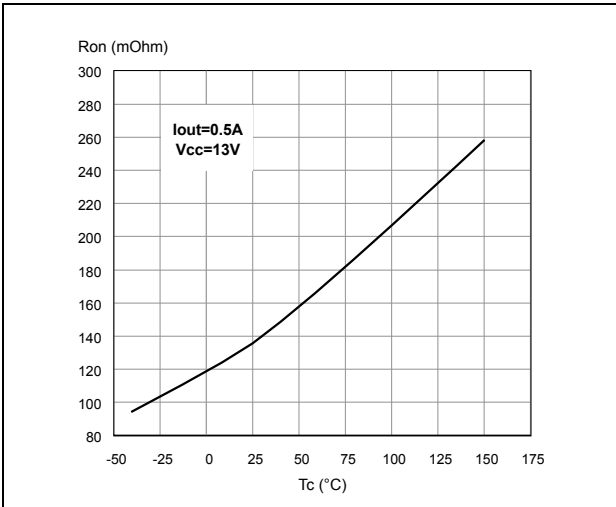


Figure 18. On state resistance vs. V_{CC}

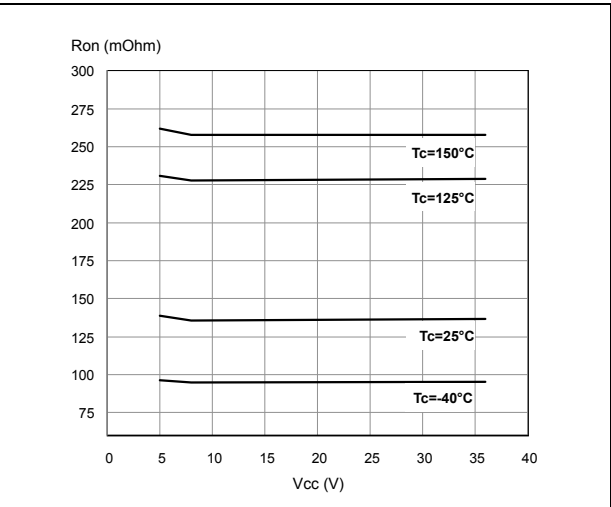


Figure 19. Undervoltage shutdown

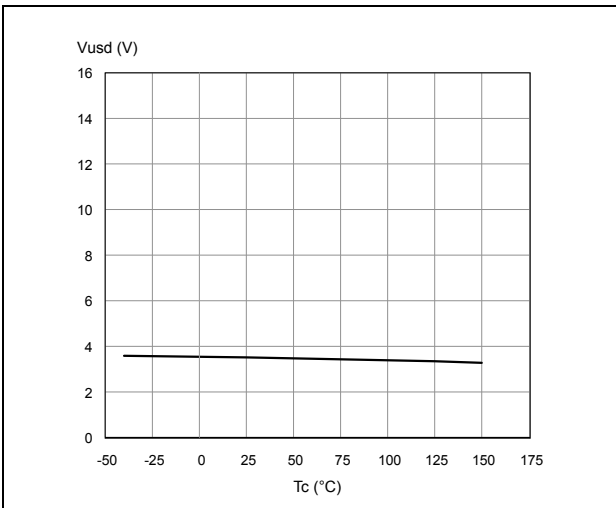


Figure 20. Turn-On voltage slope

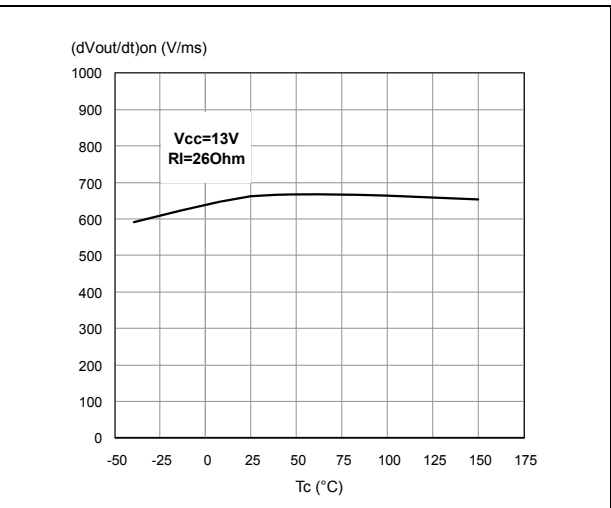


Figure 21. I_{LIMH} vs. T_{case}

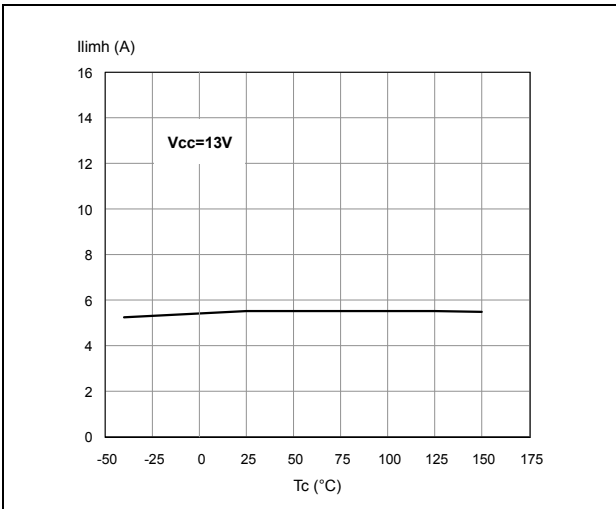


Figure 22. Turn-Off voltage slope

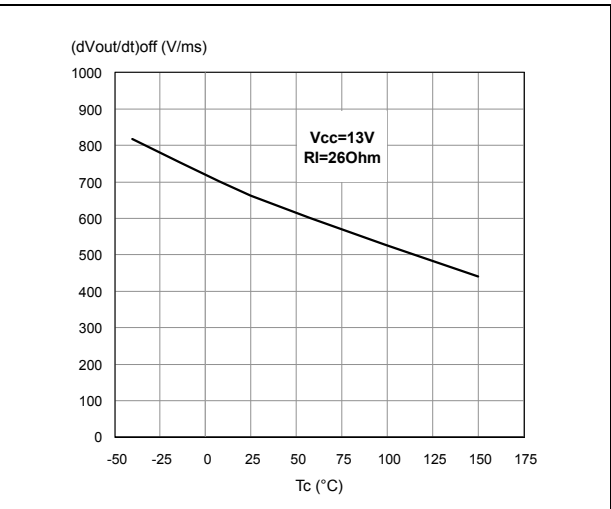


Figure 23. CS_DIS high level voltage

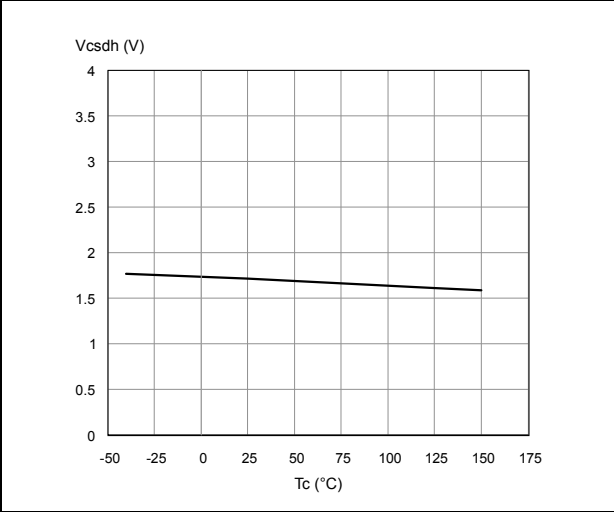


Figure 24. CS_DIS clamp voltage

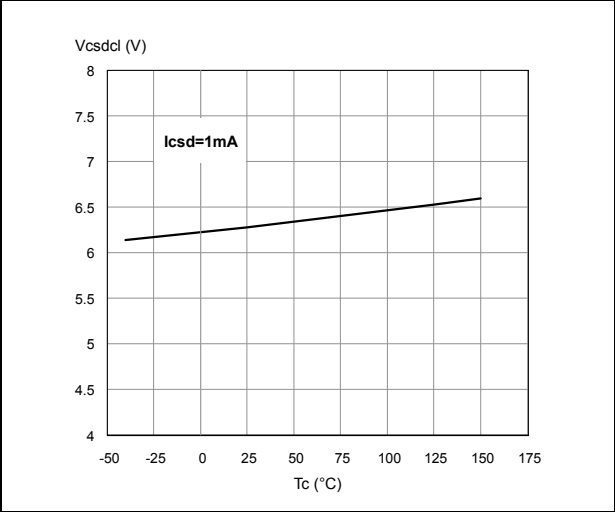
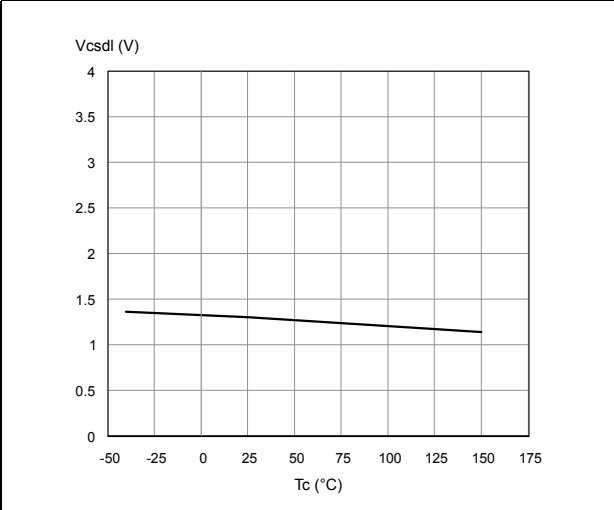
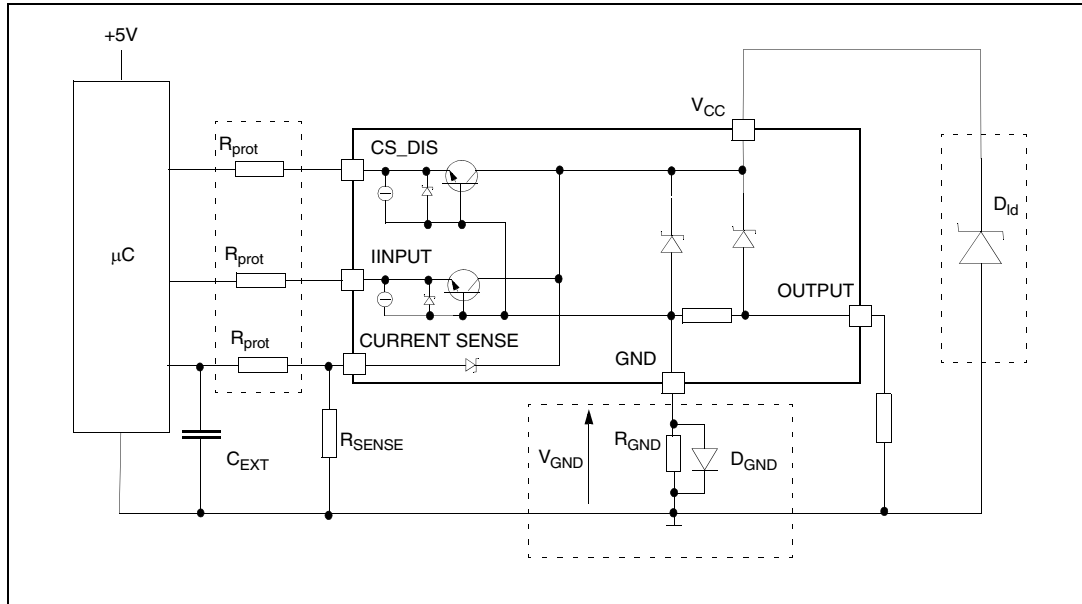


Figure 25. CS_DIS low level voltage



3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1 : resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2 : diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

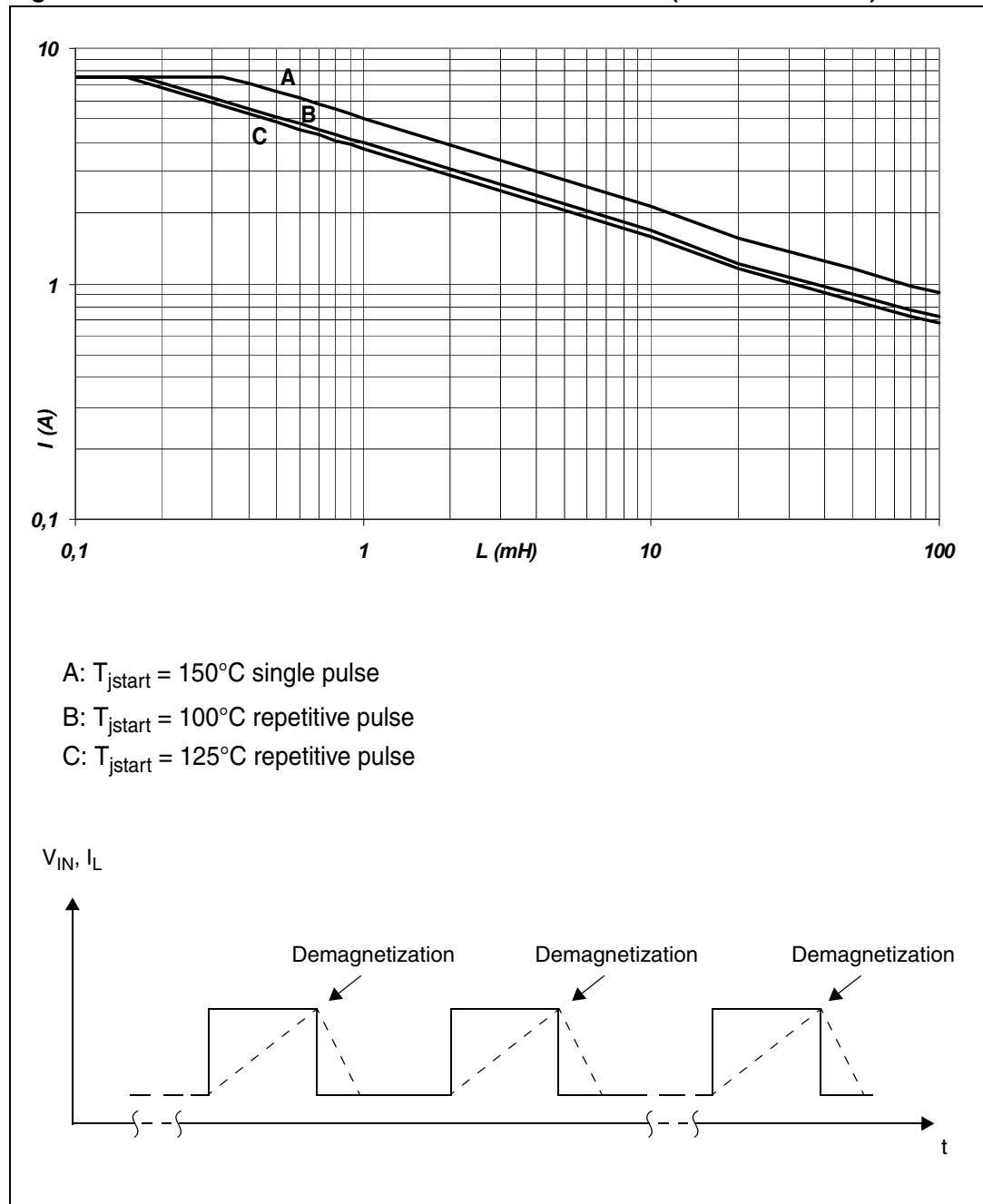
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega.$$

Recommended values: $R_{prot}=10k\Omega$, $C_{EXT}=10nF$.

3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 27. Maximum turn-Off current versus inductance (for each channel)



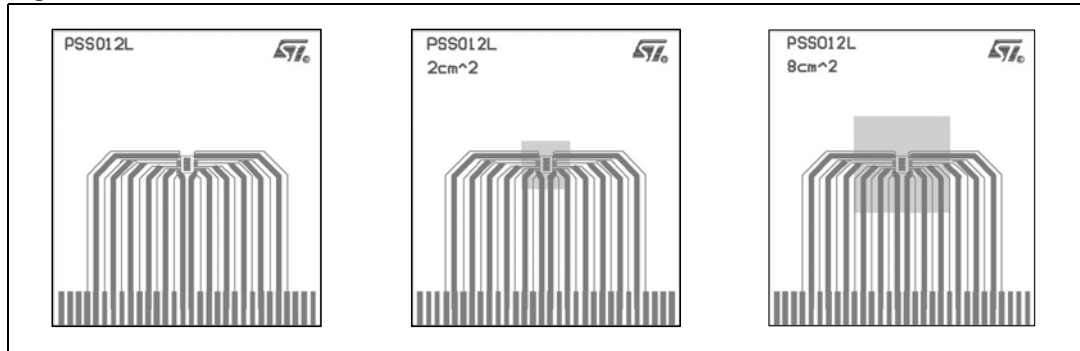
Note: Values are generated with $R_L = 0 \Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Note:

Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70μm (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 29. $R_{thj-amb}$ vs. PCB copper area in open box free air condition (one channel ON)

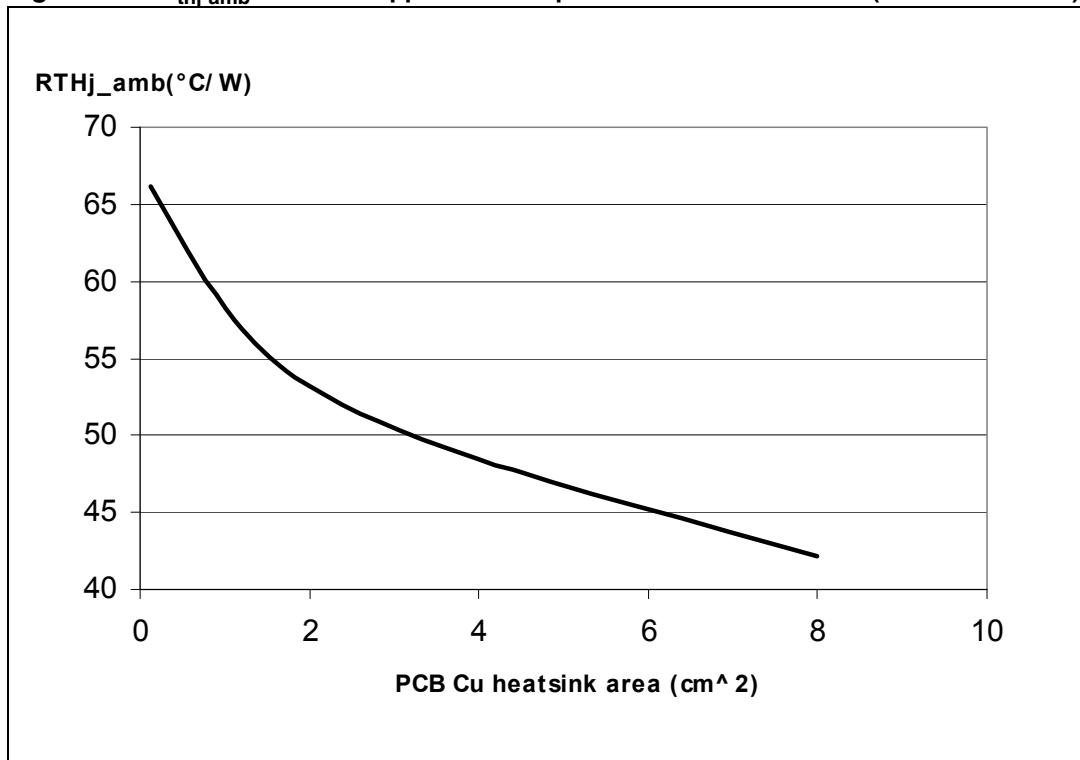
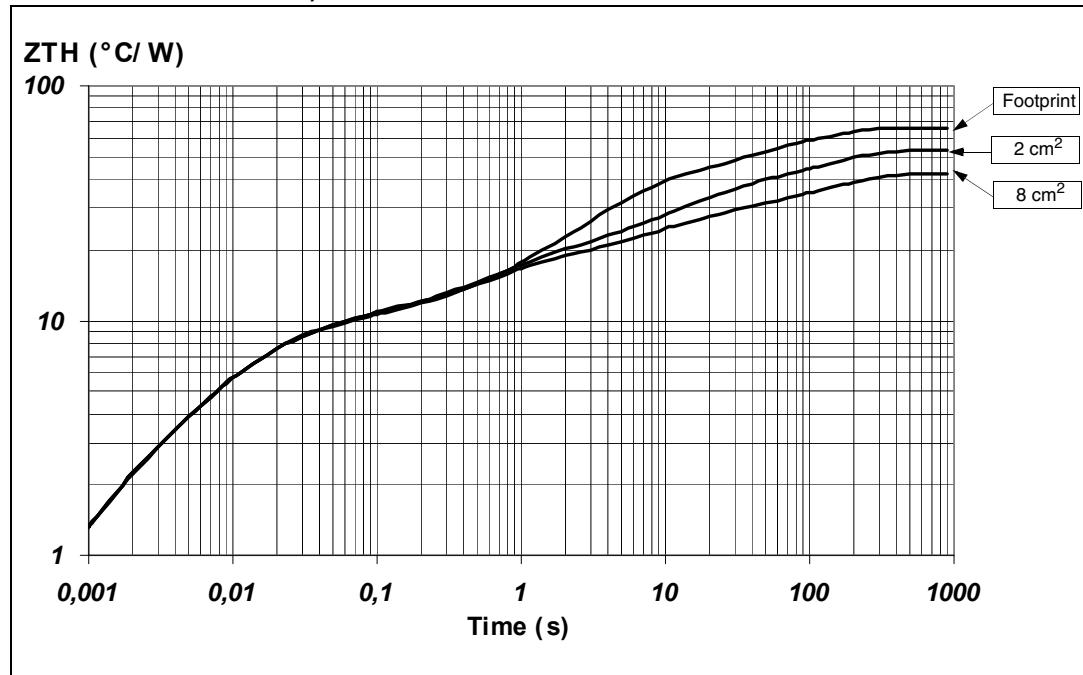


Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)

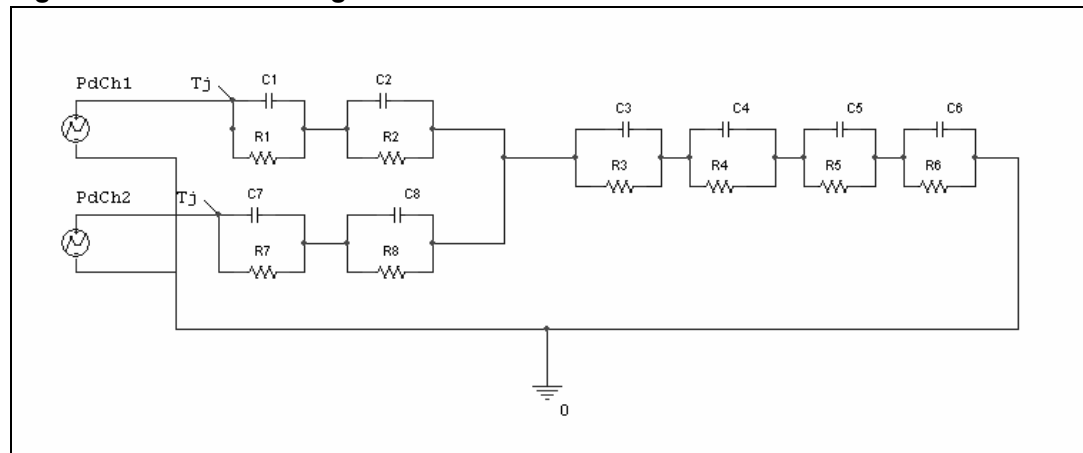


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ (a)



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1= R7 (°C/W)	1.2		
R2= R8 (°C/W)	6		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.0008		
C2= C8 (W.s/°C)	0.0016		
C3 (W.s/°C)	0.0166		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 Package mechanical data

Figure 32. PowerSSO-12™ package dimensions

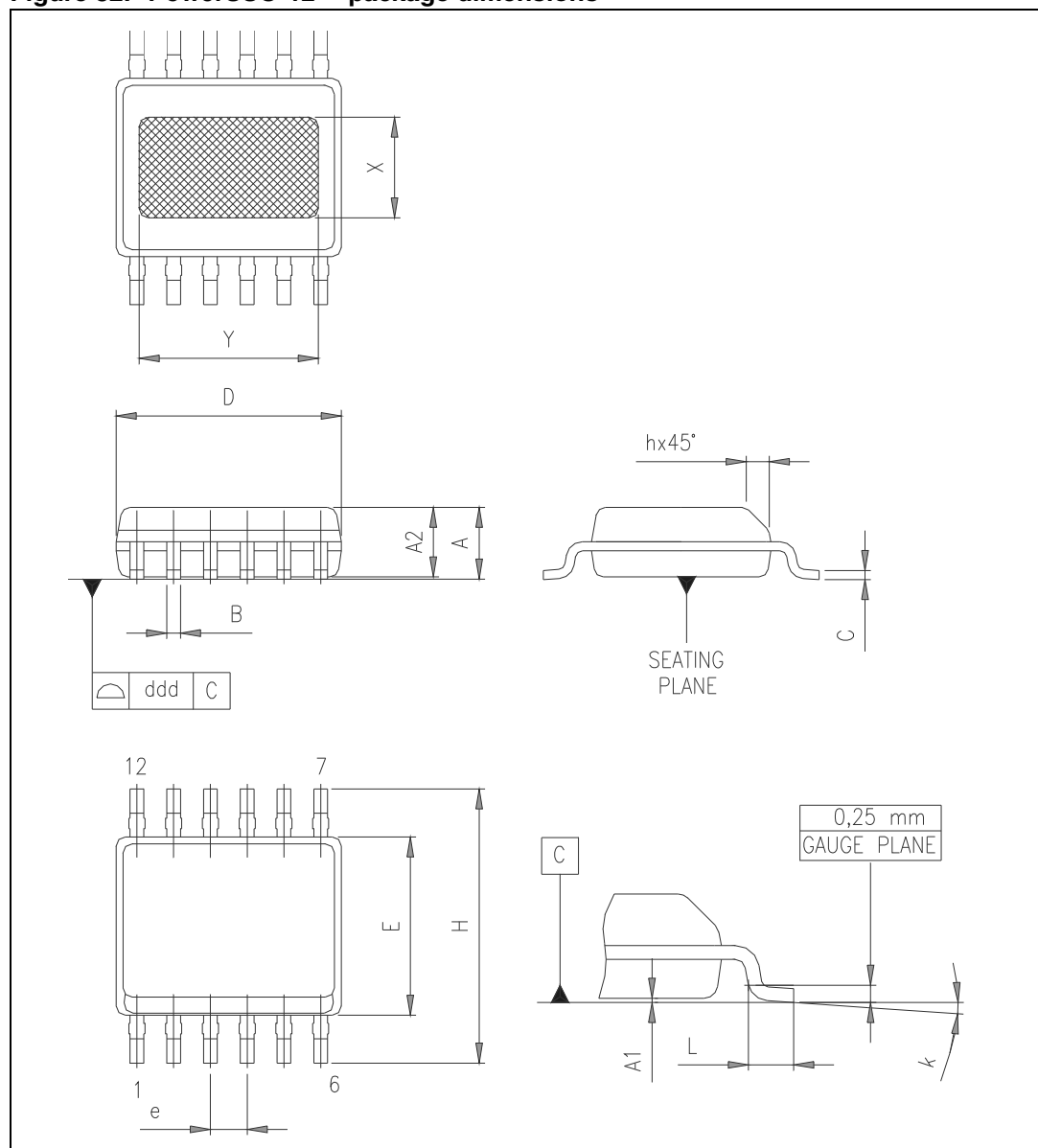


Table 14. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.3 Packing information

Figure 33. PowerSSO-12™ tube shipment (no suffix)

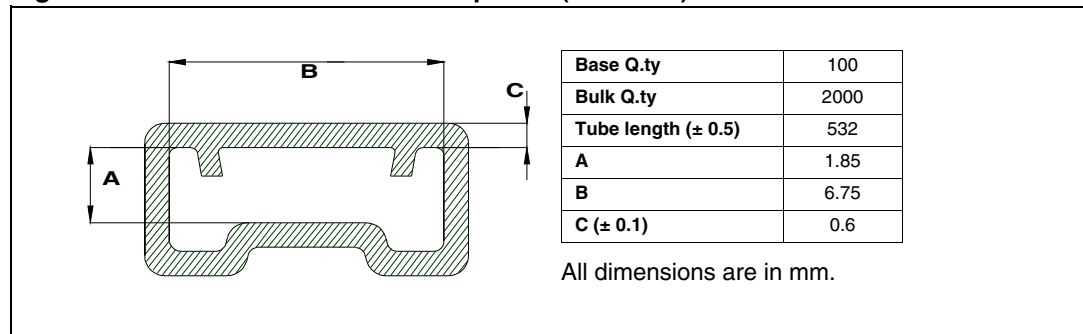
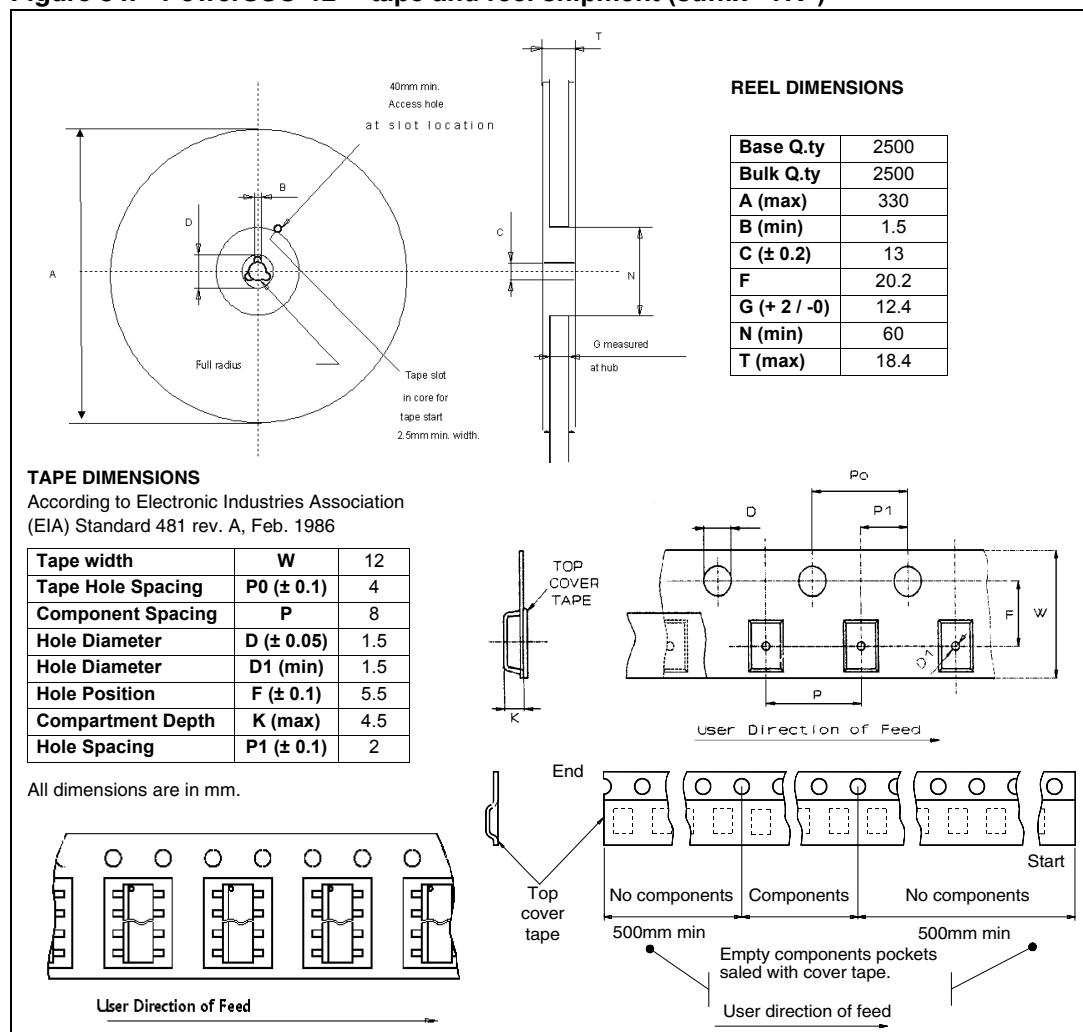


Figure 34. PowerSSO-12™ tape and reel shipment (suffix “TR”)



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
13-Sep-2004	1	Initial release.
10-Apr-2006	2	Layout changed. Major update to Section 2: Electrical specifications .
01-Mar-2007	3	Reformatted. Contents, List of tables and List of figures added. Added Section 3.4: Maximum demagnetization energy (VCC = 13.5V) . ECOPACK [®] package information added.
10-Dec-2007	4	Document reformatted and restructured. Updated Figure 2: Configuration diagram (top view) : pins 7-12 left unconnected (N.C) and added note. Table 4: Absolute maximum ratings : corrected E _{MAX} value from 14 to 34 mJ. Added Figure 5: Delay response time between rising edge of output current and rising edge of current sense (CS enabled) . Updated Figure 6: I_{out}/ I_{sense} vs. I_{out} (see Table 10 for details) . Added Figure 7: Maximum current sense ratio drift vs load current . Updated Table 10: Current sense (8V<VCC<16V) : – changed t _{DSENSE2H} max value from 300 μs to 150 μs. – added dk1/k1, dk2/k2, dk3/k3, Δt _{DSENSE2H} , I _{OL} parameters. Table 12: Electrical transient requirements : updated test level values III and IV for test pulse 5b and notes. Updated Section 4.1: PowerSSO-12™ thermal data : – changed Figure 29: R_{thj-amb} vs. PCB copper area in open box free air condition (one channel ON) . – changed Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON) . – Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™ : added note. – updated Table 13: Thermal parameters : R3 value changed from 7 to 3 °C/W. R4 values changed from 10 /10 /9 to 8 /8 /7 °C/W. C3 value changed from 0.05 to 0.0166 W.s/°C.
12-Feb-2008	5	Corrected typing error in Table 10: Current sense (8V<VCC<16V) : changed I _{OL} test condition from V _{IN} = 0V to V _{IN} = 5V.
24-Sep-2013	6	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com