



Hex D-Type Positive Edge-Triggered Flip-Flop With Common Clear and Clock

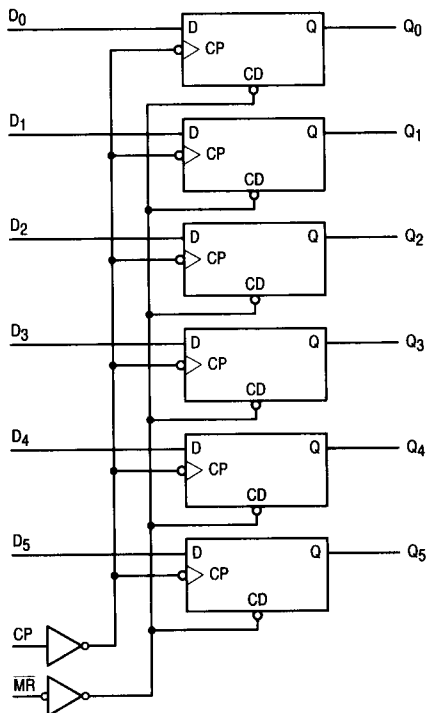
ELECTRICALLY TESTED PER:
MIL-M-38510/34107

The 54F174 is a high-speed Hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transitions. The device has a Master Reset to simultaneously clear all flip-flops.

The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of the Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset

LOGIC DIAGRAM



Military 54F174



AVAILABLE AS:

- 1) JAN: JM38510/34107BXA
- 2) SMD: N/A
- 3) 883: 54F174/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
MR	1	1	2	GND
Q0	2	2	3	OPEN
D0	3	3	4	VCC
D1	4	4	5	VCC
Q1	5	5	7	OPEN
D2	6	6	8	VCC
Q2	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	VCC
Q3	10	10	13	OPEN
D3	11	11	14	VCC
Q4	12	12	15	OPEN
D4	13	13	17	VCC
D5	14	14	18	VCC
Q5	15	15	19	OPEN
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

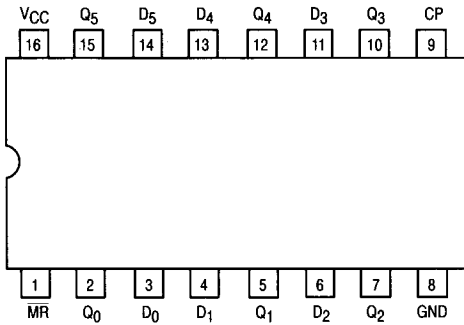
TRUTH TABLE

Inputs	Outputs
@ t_n , MR = H	@ $t_n + 1$
D_n	Q_n
H	H
L	L

t_n = Bit time before clock pulse
 $t_n + 1$ = Bit time after clock pulse
 H = HIGH Voltage Level
 L = LOW Voltage Level

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CONNECTION DIAGRAM



LOGIC SYMBOL

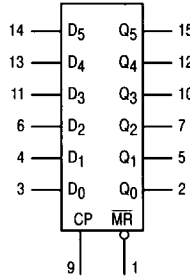
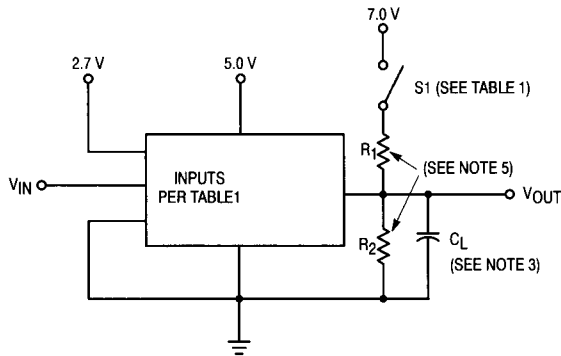


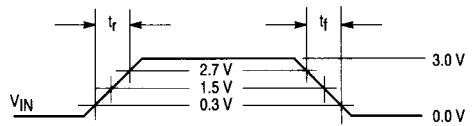
Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

AC TEST CIRCUIT



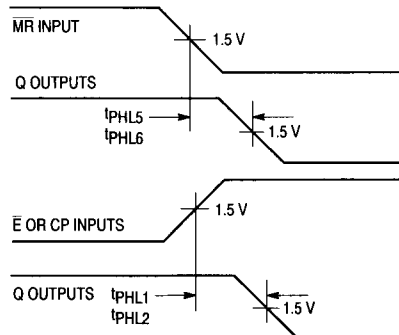
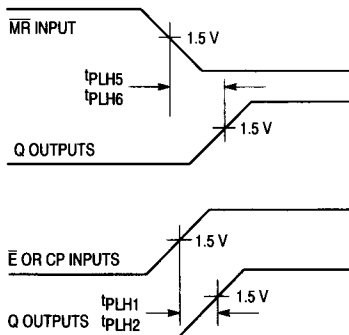
WAVEFORM



NOTES:

1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, $PRR \leq 1.0$ MHz.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 8 V, or open).
3. $C_L = 50$ pF $\pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2 = 499 \Omega \pm 5.0\%$

WAVEFORMS



Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = –1.0 mA, V _{IN} = 2.0 V, MR = 5.5 V, CP = (See Note 1).
V _{OL}	Logical “0” Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} =20 mA, V _{IH} = 2.0 V, V _{IL} = 0.8 V, MR = 5.5 V, CP = (See Note 1).
V _{IC}	Input Clamping Voltage		–1.2					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{IL}	Logical “0” Input Current	–0.03	–0.6	–0.03	–0.6	–0.03	–0.6	mA	V _{CC} = 5.5 V, V _{IL} = 0.5 V, other inputs are open.
I _{ILL}	Logical “0” Input Current — MR & CP	–0.06	–1.2	–0.06	–1.2	–0.06	–1.2	mA	V _{CC} = 5.5 V, V _{ILL} = 0.5 V, other inputs are open.
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 4.5 V, MR = 0 V, CP = (See Note 2), other inputs are open, V _{OUT} = 2.5 V.
I _{OS}	Output Short Circuit Current	–60	–150	–60	–150	–60	–150	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, CP = (See Note 2), MR = 4.5 V, other input = 0 V, V _{OUT} = 0 V.
I _{CC}	Power Supply Current		45		45		45	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs).
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
t _s (H) t _s (L)	Set Up Time, High or Low D _n to CP	4.0		4.0		4.0		ns	V _{CC} = 5.0 V, (Information only, No Testing Required).
t _h (H) t _h (L)	Hold Time, High or Low D _n to CP	1.0		1.0		1.0		ns	V _{CC} = 5.0 V, (Information only, No Testing Required).
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, (Repeat at) V _{CC} = 5.5 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output CP to Q _n	1.5	11	1.0	13	1.0	13	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω ± 5.0%.
t _{PLH1}	Propagation Delay /Data-Output CP to Q _n	1.5	9.0	1.0	11	1.0	11	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω ± 5.0%.
t _{PHL5}	Propagation Delay /Data-Output MR to Q _n	1.5	15	1.0	17	1.0	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω ± 5.0%.
t _{PHL6}	Propagation Delay /Data-Output MR to Q _n	1.0	15	1.0	17	1.0	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω ± 5.0%.
f _{MAX}	Maximum Clock Frequency	90		70		70		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω ± 5.0%.

NOTES:

1. Apply all voltages, then apply 0 V, 3.0 V, 0 V to CP, then make measurements.
2. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurements.
3. f_{MAX} minimum limit specified is the input pulse. The output frequency shall be 1/2 the input frequency.
4. Inputs need to be in the proper configuration for specified output conditions.