

DS481 Low Power RS-485/RS-422 Multipoint Transceiver with Sleep Mode

Check for Samples: [DS481](#)

FEATURES

- Meets TIA/EIA RS-485 Multipoint Standard
- Sleep Mode Reduces I_{CC} to 0.2 μA
- Guaranteed Full Load Output Voltage (V_{OD3})
- Low Quiescent Current: 200 μA typ
- -7V to +12V Common-mode Input Voltage Range
- TRI-STATE Outputs on Driver and Receiver
- AC Performance:
 - Driver Transition Time: 25 ns typ
 - Driver Propagation Delay: 40 ns typ
 - Driver Skew: 1 ns typ
 - Receiver Propagation Delay: 200 ns typ
 - Receiver Skew: 20 ns typ
- Half-duplex Flow Through Pinout
- Operates From a Single 5V Supply
- Allows up to 64 Transceivers on the Bus
- Current-limiting and Thermal Shutdown for Driver Overload Protection
- Industrial Temperature Range Operation
- Pin and Functional Compatible with MAX481C and MAX481E

DESCRIPTION

The DS481 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.0 Mbps (see [Applications Information](#)).

The transceiver draws 200 μA of supply current when unloaded or 0.2 μA when in the automatic sleep mode. Sleep mode is activated by inactivity on the enables (DE and RE⁽¹⁾). Holding DE = L and RE⁽¹⁾ = H for greater than 600 ns will enable the sleep mode. The DS481 operates from a single +5V supply.

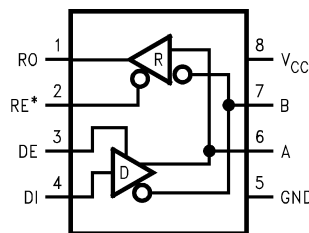
The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

The DS481 is available in a surface mount package and is characterized for Industrial temperature range operation.

(1) Non Terminated, Open Input only

Connection and Logic Diagram



*Non Terminated, Open Input only

Figure 1. SOIC Package



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Table 1. Pin Descriptions

Pin Name	Number	DESCRIPTION
RO	1	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI $\geq$ DO ⁽¹⁾ /RI ⁽¹⁾ by 200 mV, RO will be HIGH. If DO/RI $\leq$ DO ⁽¹⁾ /RI ⁽¹⁾ by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
RE ⁽¹⁾	2	Receiver Output Enable: When RE ⁽¹⁾ is LOW the receiver output is enabled. When RE ⁽¹⁾ is HIGH, the receiver output is in TRI-STATE (OFF). When RE ⁽¹⁾ is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
DE	3	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE ⁽¹⁾ is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
DI	4	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO ⁽¹⁾ /RI ⁽¹⁾ will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO ⁽¹⁾ /RI ⁽¹⁾ is LOW.
GND	5	Ground Connection.
DO/RI	6	Driver Output/Receiver Input, 485 Bus Pin.
DO ⁽¹⁾ /RI ⁽¹⁾	7	Driver Output/Receiver Input, 485 Bus Pin.
V _{CC}	8	Positive Power Supply Connection: Recommended operating range for V _{CC} is +4.75V to +5.25V.

(1) Non Terminated, Open Input only

Truth Table

DRIVER SECTION				
RE ⁽¹⁾	DE	DI	A	B
X ⁽²⁾	H	H	H	L
X ⁽²⁾	H	L	L	H
X ⁽²⁾	L	X ⁽²⁾	Z ⁽²⁾	Z ⁽²⁾ (3)
RECEIVER SECTION				
RE ⁽¹⁾	DE	A-B		RO
L	L	$\geq +0.2V$		H
L	L	$\leq -0.2V$		L
H	X ⁽²⁾	X ⁽²⁾		Z ⁽²⁾ (3)
L	L	OPEN ⁽¹⁾		H

(1) Non Terminated, Open Input only

(2) X = indeterminate

Z = TRI-STATE

(3) Device enters sleep mode if enable conditions are held > 600 ns, DE = L and RE = H. RE is Non Terminated and Open Input only.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})	+12V
Enable Input Voltage (RE ⁽³⁾ , DE)	–0.5V to ($V_{CC} + 0.5V$)
Driver Input Voltage (DI)	–0.5V to ($V_{CC} + 0.5V$)
Driver Output Voltage (A, B)	–14V to +14V
Receiver Input Voltage (A, B)	–14V to +14V
Receiver Output Voltage (RO)	–0.5V to ($V_{CC} + 0.5V$)
Maximum Package Power Dissipation @ +25°C	
D0008A Package	1.19W
Derate D0008A Package 9.5 mW/°C above +25°C	
Maximum Package Power Dissipation @ +70°C	
D0008A Package	0.76W
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range	
(Soldering, 4 sec.)	+260°C
ESD (HBM)	≥2 kV

- (1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Non Terminated, Open Input only

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Operating Free Air				
Temperature (T_A)				
DS481T	–40	+25	+85	°C
Bus Common Mode Voltage	–7		+12	V

Electrical Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified ^{(1) (2)}

Parameter			Test Conditions	Pin A, B	Min	Typ	Max	Units
V _{OD1}	Differential Driver Output Voltage	(No Load)			1.5		5	V
V _{OD2}	Differential Driver Output Voltage with Load	R _L = 50Ω, (RS422), Figure 2			2	2.8		V
		R _L = 27Ω, (RS485), Figure 2			1.5	2.3	5	V
ΔV _{OD}	Change in Magnitude of Output Differential Voltage	R _L = 27Ω or 50Ω ⁽³⁾					0.2	V
V _{OD3}	Differential Driver Output Voltage—Full Load with Max V _{CM}	R1 = 54Ω, R2 = 375Ω V _{TEST} = -7V to +12V, Figure 3			1.5	2.0	5	V
V _{OC}	Driver Common-Mode Output Voltage	R _L = 27Ω or 50Ω, Figure 2			0		3	V
ΔV _{OC}	Change in Magnitude of Common-Mode Output Voltage	R _L = 27Ω or 50Ω, Figure 2 ⁽³⁾					0.2	V

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD1/2/3}$ and V_{ID} .
- (2) All typicals are given for: $V_{CC} = +5.0V$, $T_A = +25^\circ C$.
- (3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input changes state.

Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified ⁽¹⁾ ⁽²⁾

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V _{IH}	Input High Voltage			DI, DE, RE ⁽⁴⁾	2.0			V
V _{IL}	Input Low Voltage						0.8	V
I _{IN1}	Input Current	V _{IN} = 0V or V _{CC}					±2	μA
I _{IN2}	Input Current ⁽⁵⁾ DE = 0V, V _{CC} = 0V or 5.25V	V _{IN} = +12V	DS481T	A, B	0	190	500	μA
		V _{IN} = -7V			0	-100	-400	μA
V _{TH}	Receiver Differential Threshold Voltage	-7V ≤ V _{CM} ≤ +12V			-0.2		0.2	V
ΔV _{TH}	Receiver Input Hysteresis	V _{CM} = 0V				70		mV
V _{OH}	Receiver Output High Voltage	I _O = -4 mA, V _{ID} = 0.2V		RO	3.5			V
V _{OL}	Receiver Output Low Voltage	I _O = 4 mA, V _{ID} = -0.2V					0.5	V
I _{OZR}	TRI-STATE Output Current at Receiver	0.4V ≤ V _O ≤ 2.4V					±1	μA
R _{IN}	Receiver Input Resistance	-7V ≤ V _{IN} ≤ +12V	DS481T	A, B	24			kΩ
I _{CC}	No-Load Supply Current ⁽⁶⁾	DE = V _{CC} , RE ⁽⁴⁾ = 0V or V _{CC}		V _{CC}		200	500	μA
		DE = 0V, RE ⁽⁴⁾ = 0V or V _{CC}				200	500	μA
I _{CCX}	Sleep Mode Supply Current	DE = GND RE ⁽⁴⁾ = V _{CC} (Figure 15)		V _{CC}		0.2	10	μA
I _{OSD1}	Driver Short Circuit Current, V _O = HIGH	-7V ≤ V _O ≤ +12V		A, B			250	mA
I _{OSD2}	Driver Short Circuit Current, V _O = LOW	-7V ≤ V _O ≤ +12V					-250	mA
I _{OSR}	Receiver Short Circuit Current	V _O = GND		RO	7		85	mA

(4) Non Terminated, Open Input only.

(5) I_{IN2} includes the receiver input current and driver TRI-STATE leakage current.

(6) Supply current specification is valid for loaded transmitters when DE = 0V or enabled (DE = H) with no load.

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified ⁽¹⁾ ⁽²⁾ ⁽³⁾

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLHD}	Driver Differential Propagation Delay—Low to High	$R_L = 54\Omega$, $C_L = 100\text{ pF}$	10	40	80	ns
t_{PHLD}	Driver Differential Propagation Delay—High to Low		10	39	80	ns
t_{SKEW}	Differential Skew $ t_{PHLD} - t_{PLHD} $		0	1	10	ns
t_r	Driver Rise Time		3	25	50	ns
t_f	Driver Fall Time		3	25	50	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100\text{ pF}$		50	200	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100\text{ pF}$		65	200	ns
t_{LZ}	Driver Disable from Output Low	$C_L = 15\text{ pF}$		80	200	ns
t_{HZ}	Driver Disable from Output High	$C_L = 15\text{ pF}$		80	200	ns
t_{PSH}	Driver Enable from Sleep Mode to Output High	$C_L = 100\text{ pF}$ ⁽⁴⁾ (Figure 6, Figure 7)	70	98	250	ns
t_{PSL}	Driver Enable from Sleep Mode to Output Low	$C_L = 100\text{ pF}$ ⁽⁴⁾ (Figure 8, Figure 9)	70	98	250	ns
t_{PLHD}	Receiver Differential Propagation Delay—Low to High	$C_L = 15\text{ pF (RO)}$	30	190	400	ns
t_{PHLD}	Receiver Differential Propagation Delay—High to Low		30	210	400	ns
t_{SKEW}	Differential Skew $ t_{PHLD} - t_{PLHD} $		0	20	50	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15\text{ pF}$		45	150	ns
t_{ZL}	Receiver Enable to Output Low			40	150	ns
t_{LZ}	Receiver Disable from Output Low			50	150	ns
t_{HZ}	Receiver Disable from Output High			55	150	ns
t_{PSH}	Receiver Enable from Sleep Mode to Output High	$C_L = 15\text{ pF}$ ⁽⁴⁾ (Figure 12, Figure 14)	70	97	250	ns
t_{PSL}	Receiver Enable from Sleep Mode to Output Low	$C_L = 15\text{ pF}$ ⁽⁴⁾ (Figure 12, Figure 13)	70	95	250	ns
t_{SLEEP}	Time to Sleep (Device)	DE = L and RE ⁽⁵⁾ = H (Figure 15)	50		600	ns
f_{max}	Maximum Data Rate	⁽⁶⁾	2.0			Mbps

(1) All typicals are given for: $V_{CC} = +5.0V$, $T_A = +25^\circ C$.

(2) $f = 1\text{ MHz}$, t_r and $t_f \leq 6\text{ ns}$, $Z_O = 50\Omega$.

(3) C_L includes jig and probe capacitance.

(4) For enable from sleep mode delays DE = L and RE = H for greater than 600 ns prior to test (device is in sleep mode). RE is Non Terminated, Open Input only.

(5) Non Terminated, Open Input only

(6) f_{max} is the guaranteed data rate for 50 ft of twisted pair cable. f_{max} may be conservatively determined from the ratio of driver transition time (t_r) to the data rate unit interval ($1/f_{max}$). Using a 10% ratio yields $f_{max} = (0.1)/50\text{ ns} = 2.0\text{ Mb/s}$. Higher data rates may be supported by allowing larger ratios.

PARAMETER MEASUREMENT INFORMATION

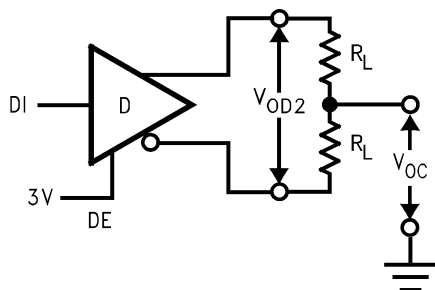
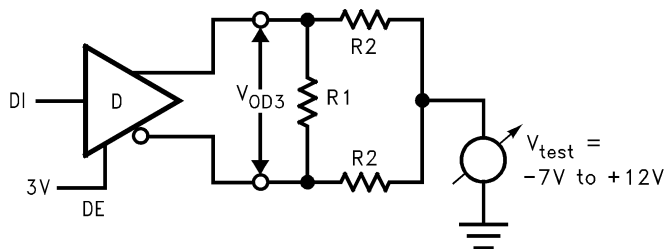
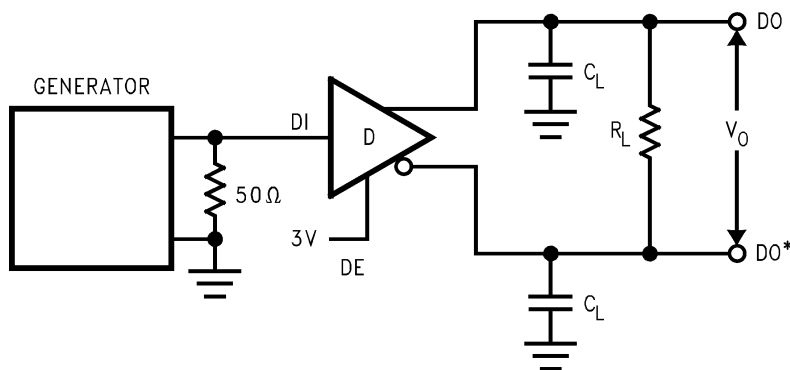
Figure 2. V_{OD} Figure 3. V_{OD3} 

Figure 4.

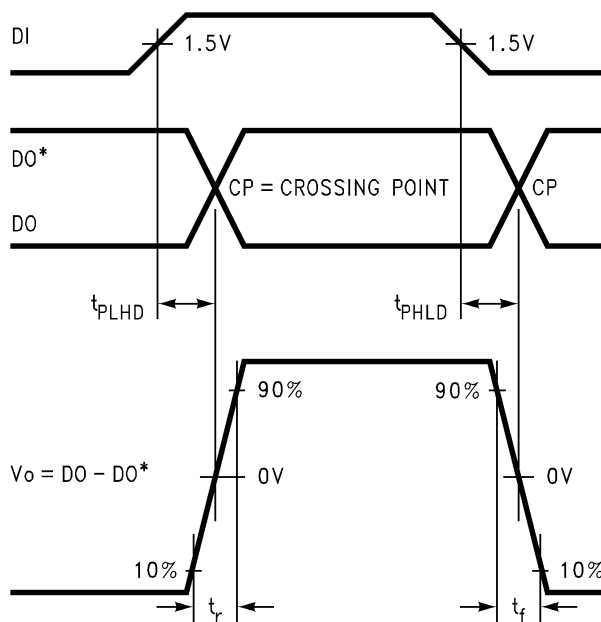


Figure 5.

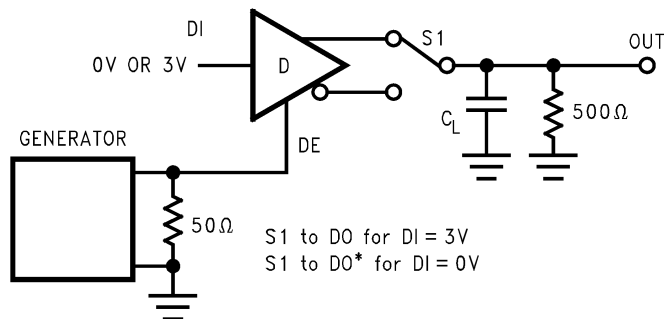


Figure 6.

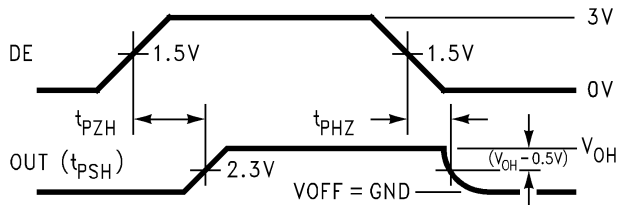


Figure 7.

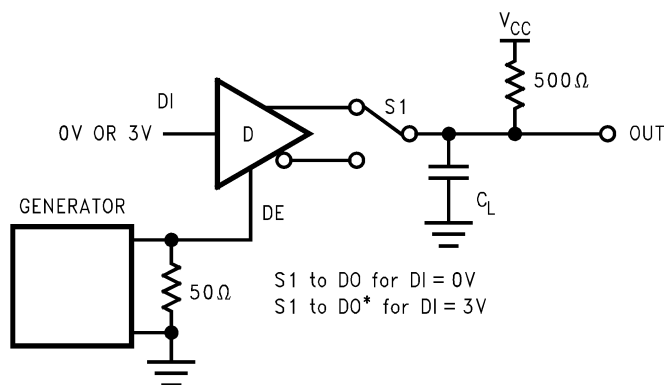


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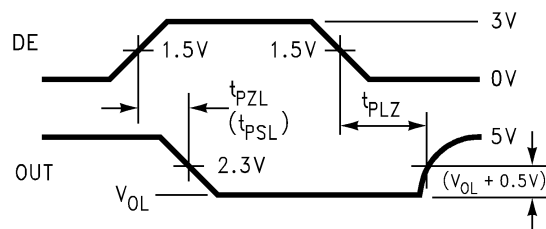


Figure 9.

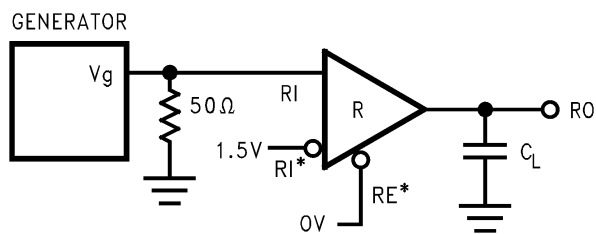


Figure 10.

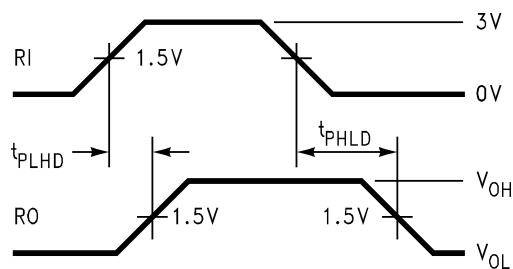


Figure 11.

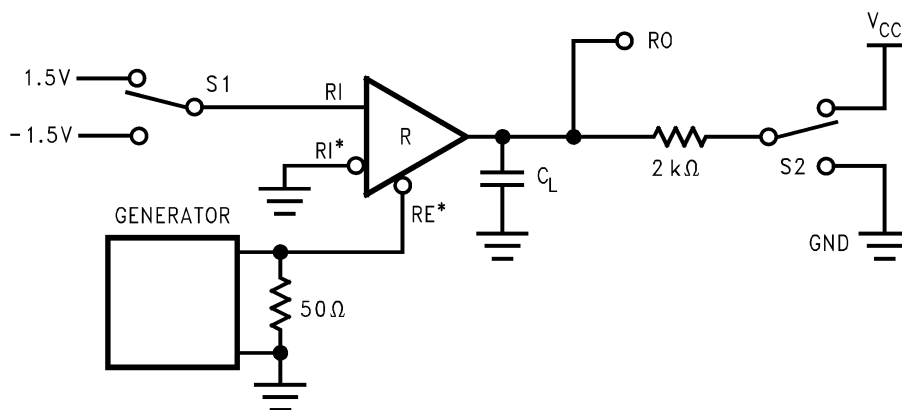


Figure 12.

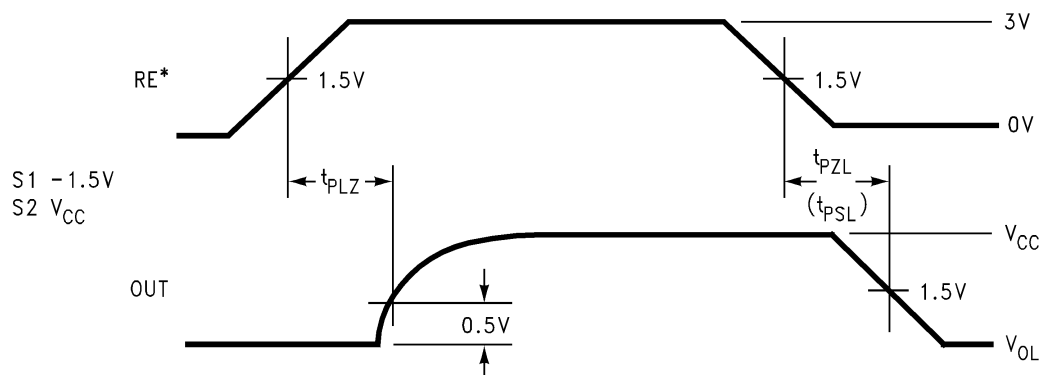


Figure 13.

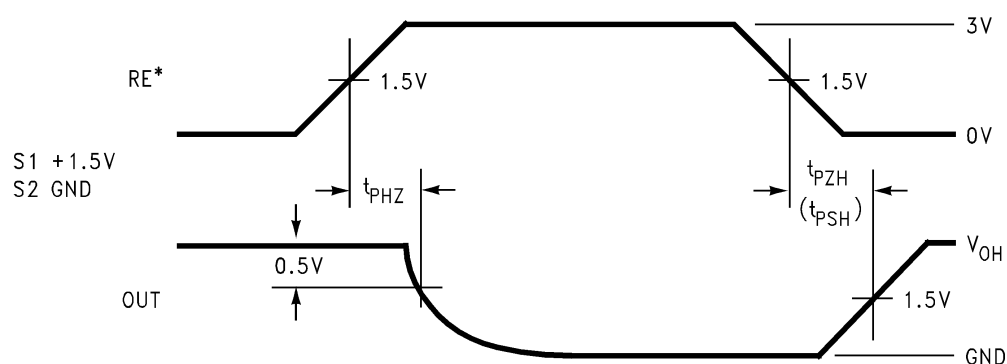
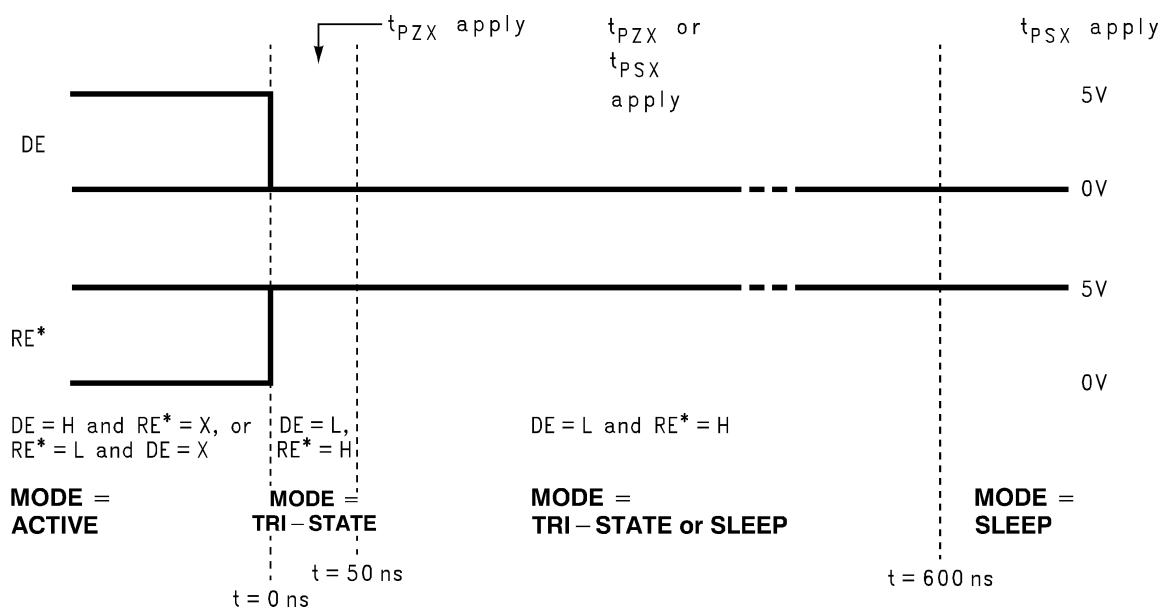


Figure 14.



*Note: Non Terminated, Open Input only

Figure 15. Entering Sleep Mode Conditions (modes and exit parameters shown)

Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from -7V to $+12\text{V}$. The top border extending from -3V at 0 mA to $+12\text{V}$ at $+1\text{ mA}$ is defined as one unit load. Likewise, the bottom border extending from $+5\text{V}$ at 0 mA to -7V at -0.8 mA is also defined as one unit load (see Figure 16). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes.

The DS481 has $\frac{1}{2}$ unit load and will allow up to 64 nodes guaranteed over temperature.

For a $\frac{1}{2}$ UL device the top and bottom borders shown in Figure 16 are scaled. Both 0 mA reference points at $+5\text{V}$ and -3V stay the same. The other reference points are $+12\text{V}$ at $+0.5\text{ mA}$ for the top border and -7V at -0.4 mA for the bottom border (see Figure 16). Again, both 0 mA reference points at $+5\text{V}$ and -3V stay the same. The other reference points are $+12\text{V}$ at $+0.25\text{ mA}$ for the top border and -7V at -0.2 mA for the bottom border (see Figure 16).

The advantage of the $\frac{1}{2}$ UL device is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS481 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

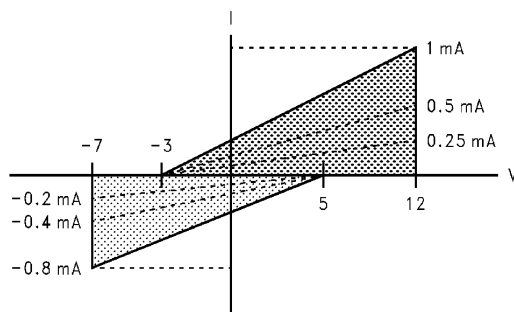


Figure 16. Input Current vs Input Voltage Operating Range

Sleep Mode

The DS481 features an automatic sleep mode that allows the device to save power when not transmitting data. Since the sleep mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the RE⁽⁷⁾ pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode after 50 ns. The DS481 is guaranteed to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the RE⁽⁷⁾ pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to datasheet specifications t_{PSL} and t_{PSH} and compare with t_{PZL} and t_{PZH} for timing differences.

The benefit of the DS481 is definitely its power savings. When active the device has a maximum I_{CC} of $500\text{ }\mu\text{A}$. When in sleep mode the device has a maximum I_{CC} of only $10\text{ }\mu\text{A}$, which is 50 times less power than when active. The I_{CC} when the device is active is already very low but when in sleep mode the I_{CC} is ultra low.

(7) Non Terminated, Open Input only

APPLICATIONS INFORMATION

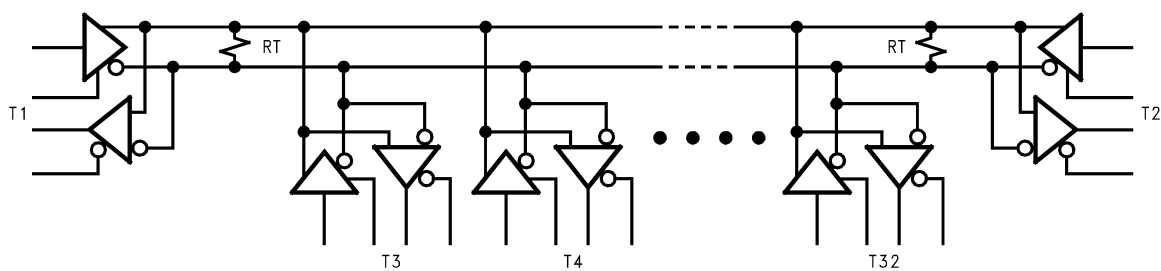


Figure 17. Multipoint RS-485 Application

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B

Page

- Changed layout of National Data Sheet to TI format [10](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS481TM/NOPB	LIFEBUY	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS481 TM	
DS481TMX/NOPB	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS481 TM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

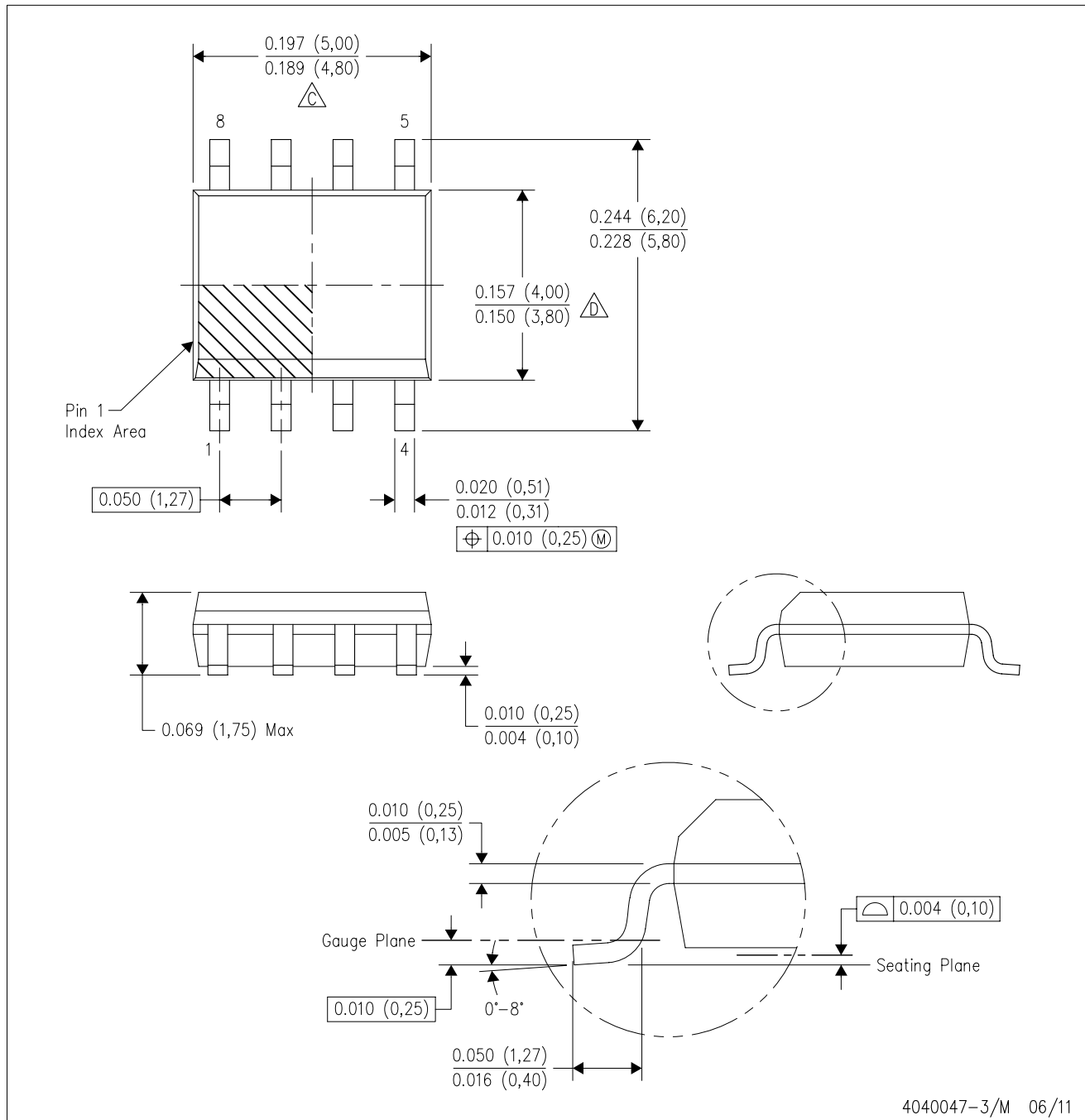
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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