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FSA839 — Low-Voltage, 0.8Ω SPDT Analog Switch with Power-Off Isolation

Features

- Power-Off Isolation (V_{CC}=0 V)
- 0.8 Ω Maximum On Resistance (R_{ON}) for 4.5 V V_{CC}
- 0.25 Ω Maximum R_{ON} Flatness for 4.5 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Fast Turn-On and Turn-Off Times
- Control Input Switching Thresholds Independent of V_{CC}
- Break-Before-Make Enable Circuitry
- 0.4 mm WLCSP Packaging
- ESD Performance
  - HBM per JESD22-A114, I/O to GND: 8 kV
  - CDM per JESD22-C101: 500 V
  - IEC61000-4-2 Contact / Air: 8 kV / 15 kV

Applications

- Cellular Phone
- Portable Media Player
- PDA

Description

The FSA839 is a high-performance Single-Pole / Double-Throw (SPDT) analog switch for audio applications driven by low-voltage (1.8 V) baseband processors or ASICs. The device features ultra-low R_{ON} of 0.8 Ω (maximum) at 4.5 V V_{CC} and operates over the wide V_{CC} range of 1.65 V to 5.5 V. The device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation.

The FSA839 interfaces between the low-voltage ASIC and regular audio amplifiers and CODECs operating up to a 5.5 V supply range. The control circuitry allows for 1.8 V (typical) signals on the control pin (Sel).

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA839UCX	-40°C to +85°C	N3	6-Ball WLCSP, 0.4 mm Pitch	Tape and Reel

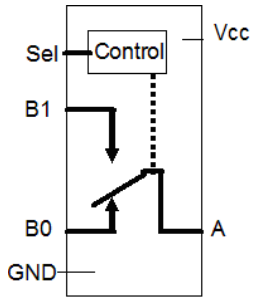
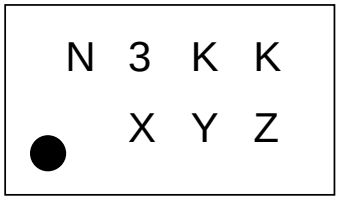


Figure 1. Analog Symbol

October-2017, Rev. 2
Publication Order Number:
FSA839/D

Marking Information



KK = Lot Run Code
X = Year
Y = Work Week
Z = Assembly Site

Figure 2. Top Mark with Pin 1 Orientation

Ball Configuration

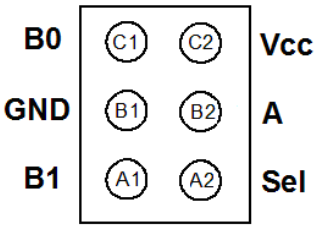


Figure 3. Pin Assignments (Bottom View)

Ball Definitions

Ball	Name	Description
A1	B1	Data Port (Normally Open)
B1	GND	Ground
C1	B0	Data Ports (Normally Closed)
C2	V_{CC}	Supply Voltage
B2	A	Common Data Port
A2	Sel	Control Input

Truth Table

Control Input (Sel)	Function
LOW	B0 connected to A
HIGH	B1 connected to A

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6.5	V
V_{SW}	Switch Voltage[1]		-0.5	V_{CC} + 0.5	V
V_{IN}	Input Voltage[1]		-0.5	6.5	V
I_{IK}	Input Diode Current			-50	mA
I_{SW}	Switch Current (Continuous)			200	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1 ms Duration, <10% Duty Cycle)			400	mA
P_D	Power Dissipation at 85°C			180	mW
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	I/O to GND: A		8	kV
		All Pins		2	
	Charged Device Model (JEDEC: JESD22-C101)			500	V
	Machine Model (JEDEC: JESD22-A115)			100	V
	IEC6100-4-2 Discharge System Test Performed on ON Semiconductor's FSA859 Applications Testing Board	Contact		8	kV
		Air		15	

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	5.50	V
SEL	Control Input Voltage	0	1.95	V
V_{SW}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
θ_{JA}	Thermal Resistance, Still Air		350	°C/W

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			T_A=-40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High	1.65 to 5.50					1.0		V
V_{IL}	Input Voltage Low	1.65 to 5.50						0.57	V
I_{IN}	Control Input Leakage	1.95 to 5.50	V_{Sel}=0	-2		2	-20	20	nA
$I_{NO(0FF)}$, $I_{NC(OFF)}$,	Off-Leakage Current of Port B0 and B1[5]	5.50	A=1 V, 4.5 V B0 or B1=4.5, 1 V	-10		10	-50	50	nA
		3.60	A=1 V, 3.0V B0 or B1=3.0, 1V	-10		10	-50	50	
		2.70	A=0.5 V, 2.3 V B0 or B1=2.3, 0.5V	-10		10	-50	50	
		1.95	A=0.3 V, 1.65 V B0 or B1=1.65 ,0.3 V	-5		5	-20	20	
$I_{NO(On)}$, $I_{NC(On)}$	On-Leakage Current of Port B0 and B1[5]	5.50	A=Floating B0 or B1=4.5, 1V	-20		20	-100	100	nA
		3.60	A=Floating B0 or B1=3.0, 1 V	-10		10	-20	20	
		2.70	A=Floating B0 or B1=2.3, 0.5 V	-10		10	-20	20	
		1.95	A=Floating B0 or B1=1.65, 0.3 V	-5		5	-20	20	
$I_{A(ON)}$	On Leakage Current of Port A[5]	5.50	A=1 V, 4.5 V; B0 or B1=1 V, 4.5 V, or Floating	-20		20	-100	100	nA
		3.60	A=1V, 3.0VB0 or B1=1V, 3.0V, or Floating	-10		10	-20	20	
		2.70	A=0.5 V, 2.3 V, B0 or B1=0.5 V, 2.3 V, or Floating	-10		10	-20	20	
		1.95	A=0.3 V, 1.65 V; B0 or B1=0.3 V, 1.65 V, or Floating	-5		5	-20	20	
I_{OFF}	Power Off Leakage Current of Port A & Port B[5]	0	A=0 to 5.5 V B0 or B1=0 to 5.5 V	-1.00	0.01	1.00	-5.00	5.00	µA
R_{PD}	Sel Internal Pull-Down Resistor	1.65 to 1.95			2.0				MΩ
I_{CC}	Quiescent Supply Current	5.50	V_{IN}, V_{SEL} =0 or V_{CC}, I_{OUT}=0			100		500	nA

		3.60	V_{IN}, V_{SEL} =0 or V_{CC}, I_{OUT}=0			75		300	
		2.70	V_{IN}, V_{SEL} =0 or V_{CC}, I_{OUT}=0			50		250	
		1.95	V_{IN}, V_{SEL} =0 or V_{CC}, I_{OUT}=0			25		150	

Continued on the following page…

DC Electrical Characteristics (Continued)

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			T_A=-40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
I_{CCT}	Increase in I_{CC} per Control Input	5.50	V_{Sel} = 1.8 V		26	40		50	µA
		3.60	V_{Sel} = 1.8 V		5	15		20	
		2.70	V_{Sel} = 1.8 V		1	5		10	
		1.95	V_{Sel} = 1.8 V		0.01	1.00		3.00	
I_{CCZ}	Supply Current Sleep	5.50	V_{IN}, V_{Sel} = Floating			0.5		1.0	µA
R_{ON}	Switch On Resistance(2,5)	4.50	I_{OUT}=-100 mA, B0 or B1=2.5 V		0.50	0.75		0.80	Ω
		3.00	I_{OUT}=-100 mA, B0 or B1=2.0 V		0.75	0.90		1.20	
		2.25	I_{OUT}=-100 mA, B0 or B1=1.8 V		1.0	1.3		1.6	
		1.65	I_{OUT}=-100 mA, B0 or B1=1.2 V		2.5	5.0		7.0	
ΔR_{ON}	On Resistance Matching Between Channels(3,5)	4.50	I_{OUT}=-100 mA, B0 or B1=2.5 V		0.05	0.10		0.10	Ω
		3.00	I_{OUT}=-100 mA, B0 or B1=2.0 V		0.10	0.15		0.15	
		2.25	I_{OUT}=-100 mA, B0 or B1=1.8 V		0.15	0.20		0.20	
		1.65	I_{OUT}=-100 mA, B0 or B1=1.2 V		0.15	0.40		0.40	
$R_{FLAT(ON)}$	On Resistance Flatness(4,5)	4.50	I_{OUT}=-100 mA, B0 or B1=1.0V, 1.5 V, 2.5 V		0.075	0.250		0.250	Ω
		3.00	I_{OUT}=-100 mA, B0 or B1=0.8 V, 2.0 V		0.1	0.3		0.3	
		2.25	I_{OUT}=-100 mA, B0 or B1=0.8 V, 1.8 V		0.25	0.50		0.60	
		1.65	I_{OUT}=-100mA, B0 or B1=0.6 V, 1.2 V		3.5				

Notes:

2. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
3. $\Delta R_{ON}=R_{ON}$ maximum – R_{ON} minimum; measured at identical V_{CC}, temperature, and voltage.
4. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
5. Guaranteed by characterization, not production tested for V_{CC}=1.65 – 1.95 V.

AC Electrical Characteristics

All typical value are at V_{CC}=1.8 V, 2.5 V, 3.0 V, and 5.0 V at 25°C unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			T_A=-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time[6]	4.50 to 5.50	B0 or B1=V_{CC}, R_L=50 Ω, C_L=35 pF	1.0	12.0	25.0	1.0	30.0	ns	Figure 4
		3.00 to 3.60		5.0	15.0	30.0	3.0	35.0		
		2.30 to 2.70		5.0	20.0	35.0	5.0	40.0		
		1.65 to 1.95		10.0	50.0	70.0	10.0	75.0		
t_{OFF}	Turn-Off Time[6]	4.50 to 5.50	B0 or B1=V_{CC}, R_L=50 Ω, C_L=35 pF	1.0	9.5	20.0	1.0	25.0	ns	Figure 4
		3.00 to 3.60		1.0	9.0	20.0	1.0	25.0		
		2.30 to 2.70		2.0	10.0	20.0	2.0	25.0		
		1.65 to 1.95		2.0	28.0	40.0	2.0	50.0		
t_{BBM}	Break-Before-Make Time[7]	4.50 to 5.50	B0 or B1=V_{CC}/2, R_L=50 Ω, C_L=35 pF	1.0	10.0	12.0	0.1	14.0	ns	Figure 5
		3.00 to 3.60		1.0	14.0	16.0	1.0	17.0		
		2.30 to 2.70		1.0	21.0	25.0	1.0	27.0		
		1.65 to 1.95			35.0		2.0	50.0		
Q	Charge Injection	5.50	C_L=1.0 nF, V_{GEN}=0 V, R_{GEN}=0 Ω		70				pC	Figure 7
		3.30			40					
		2.50			30					
		1.65			10					
OIRR	Off Isolation	1.8 to 5.0	f=1 MHz, R_L=50 Ω		-55				dB	Figure 6
Xtalk	Crosstalk	1.8 to 5.0	f=1 MHz, R_L=50 Ω		55				dB	Figure 6
BW	-3 db Bandwidth	5.50	R_L=50 Ω		60				MHz	Figure 9
		3.30			60					
		2.50			55					
		1.65			50					
THD	Total Harmonic Distortion	1.80	R_L=600 Ω, V_{IN}=0.5 V_{PP}, f=20 Hz to 20 kHz		.02				%	Figure 10
		5.00			.001					
PSRR	Power Supply Rejection Ratio	3.3	f=217 Hz on V_{CC} at 500 mvpp		-23				dB	Figure 11

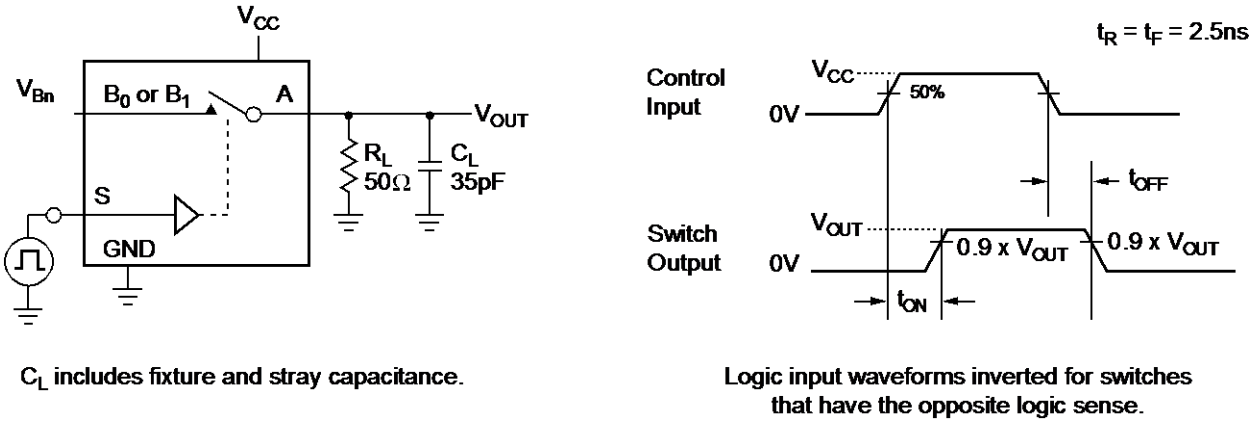
Notes:

6. Guaranteed by characterization, not production tested for V_{CC}=1.65 – 1.95 V.
7. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			Unit
				Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	0	f=1 MHz		3.2		pF
C_{OFF}	B Port Off Capacitance	1.65 to 5.50	f=1 MHz		50		pF
C_{ON}	A Port On Capacitance	1.65 to 5.50	f=1 MHz		150		pF

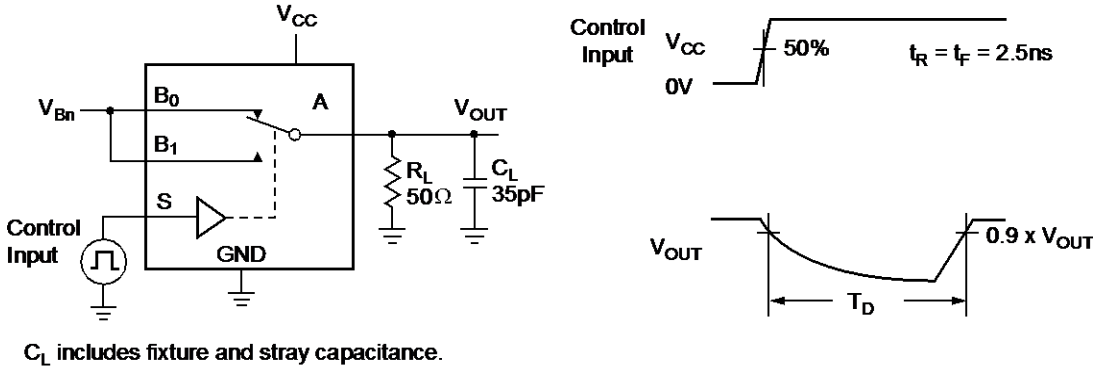
Test Diagrams



C_L includes fixture and stray capacitance.

Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 4. Turn On / Off Timing



C_L includes fixture and stray capacitance.

Figure 5. Break-Before-Make Timing

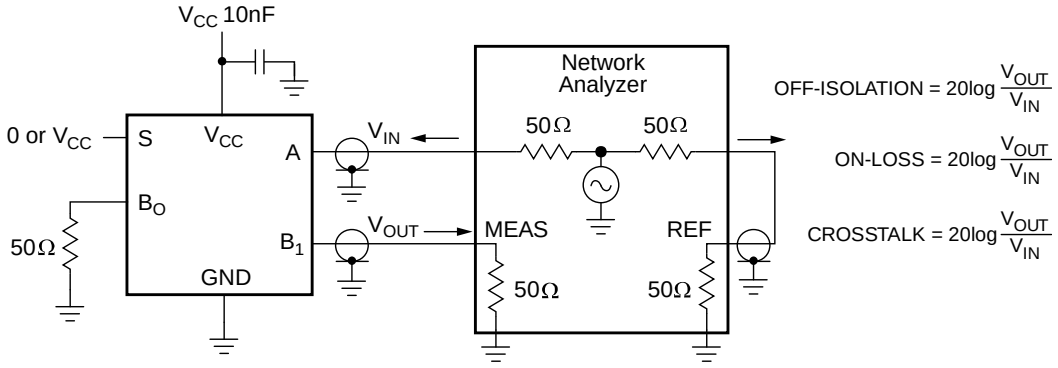


Figure 6. Off Isolation and Crosstalk

Test Diagrams (Continued)

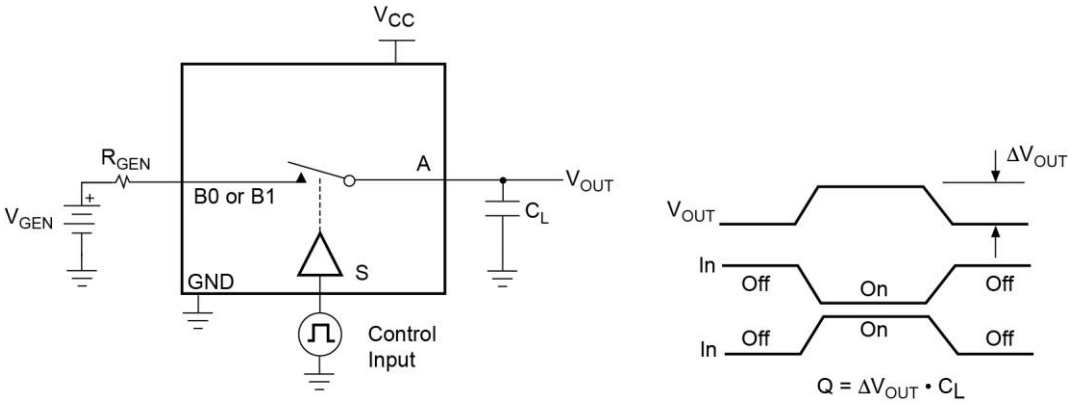


Figure 7. Charge Injection

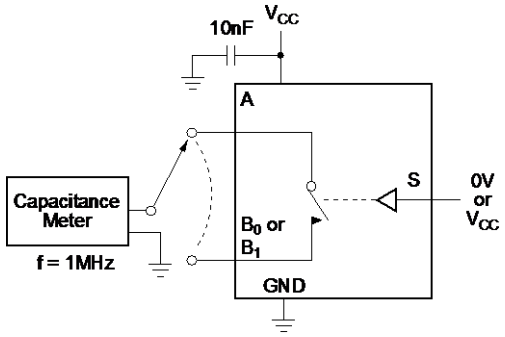


Figure 8. On / Off Capacitance Measurement Setup

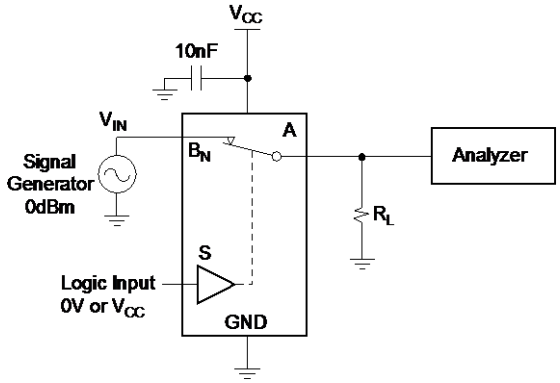


Figure 9. Bandwidth

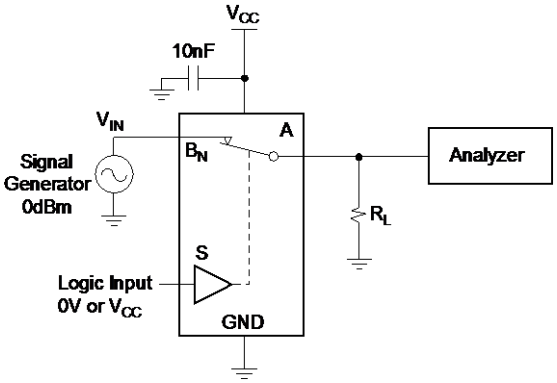


Figure 10. Harmonic Distortion

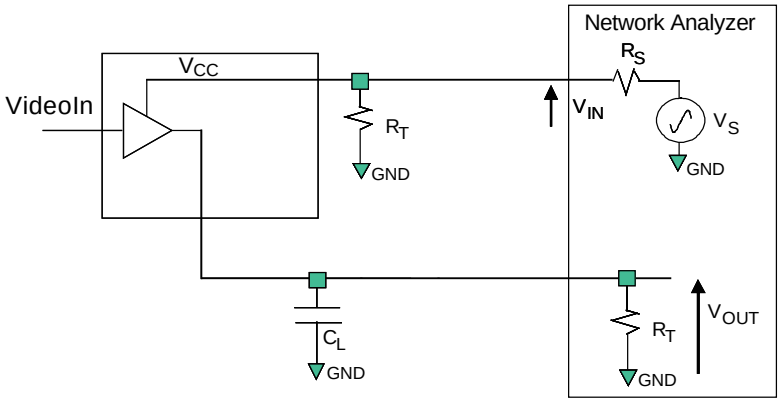
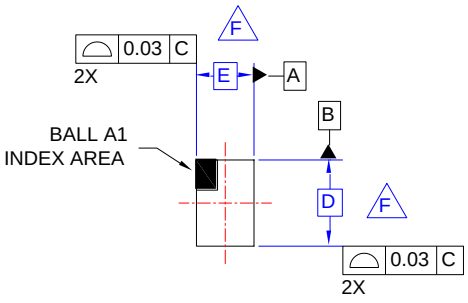


Figure 11. PSRR

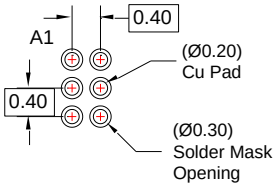
Product Specific Dimensions

Product	D	E	X	Y
FSA839UCX	1.160 ±.030	0.760 ±.030	0.180	0.180

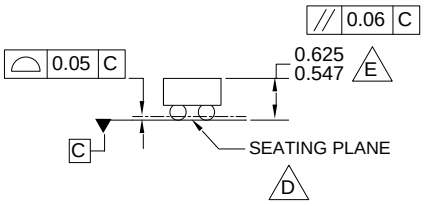
Physical Dimensions

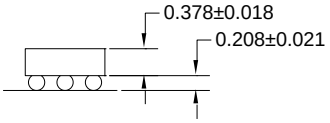


TOP VIEW

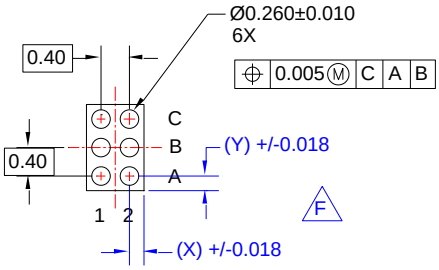


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 1994.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006ACrev4.

Figure 12. 6-Ball, WLCSP 0.4 mm Pitch

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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