

CD74FCT16511T, CD74FCT162511T

**Fast CMOS 16-Bit Registered/Latched
Transceivers with Parity**

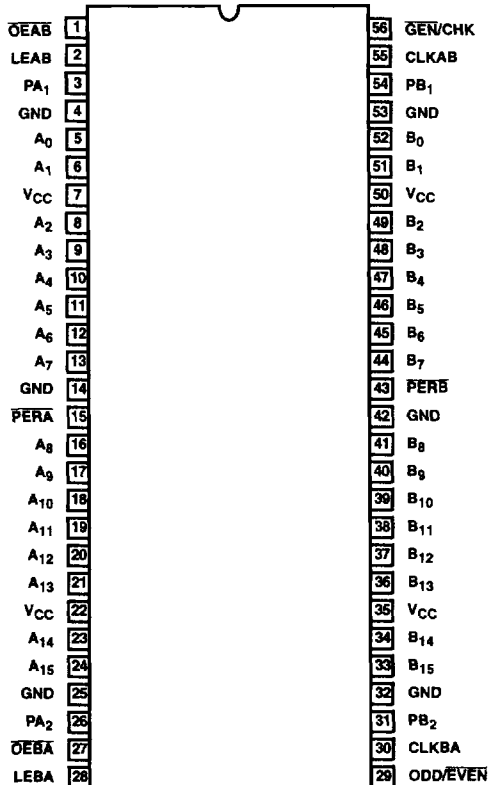
December 1996

Features

- These Devices are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16511T
 - High Output Drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
 - Power Off Disable Outputs Permit "Live Insertion"
 - Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$
- CD74FCT162511T
 - Balanced Output Drivers: $\pm 24mA$
 - Open Drain Parity Error Allows Wire-OR
 - Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Pinout

CD74FCT16511T, CD74FCT162511T (SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16511T and CD74FCT162511T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The CD74FCT16511T and CD74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the OEXX control pins.

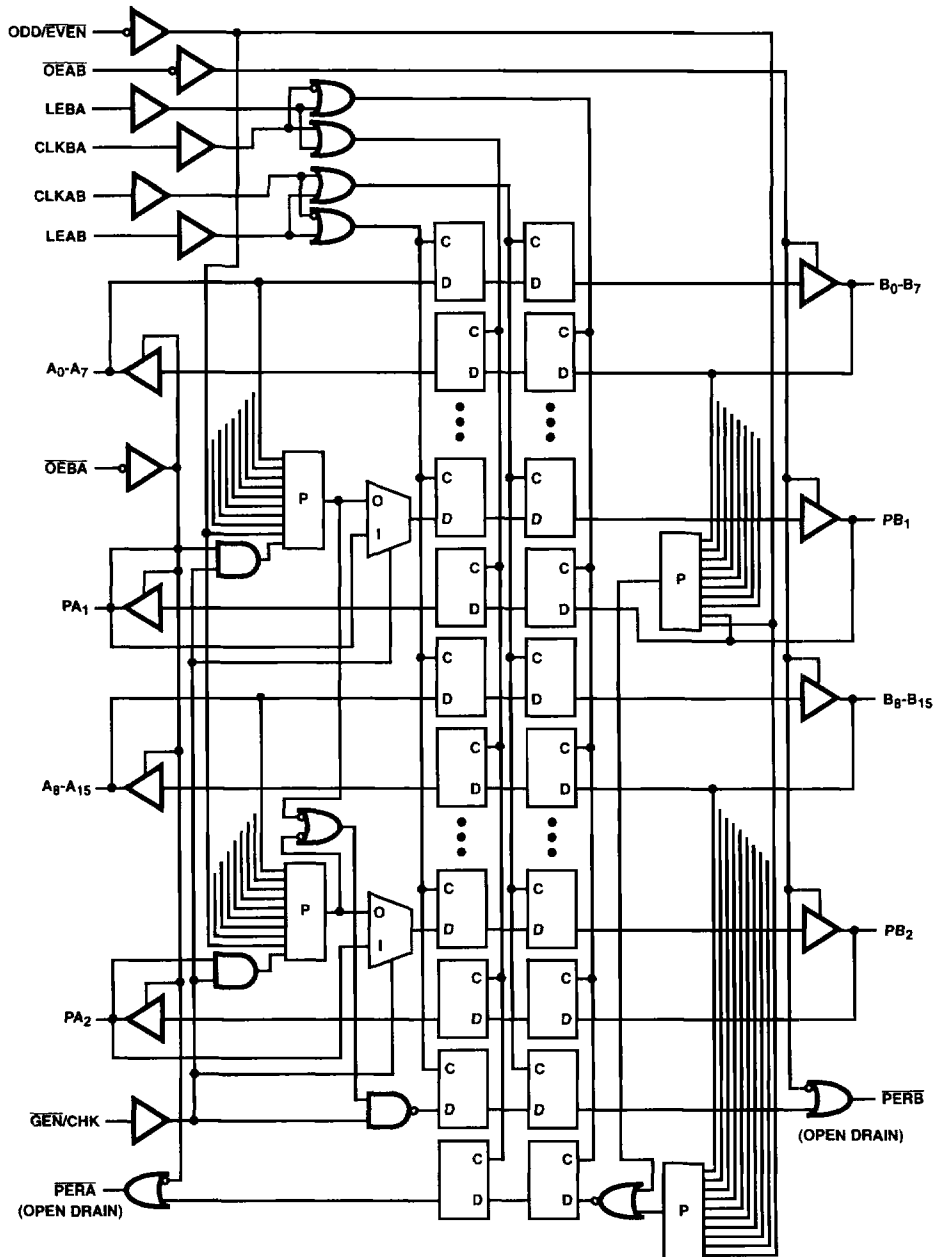
The operation in A-to-B direction is controlled by LEAB, CLKAB and OEAB control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and OEBA control pins. GEN/CHK is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/EVEN select is common between the two directions by using the corresponding control lines except for the ODD/EVEN control.

Ordering Information

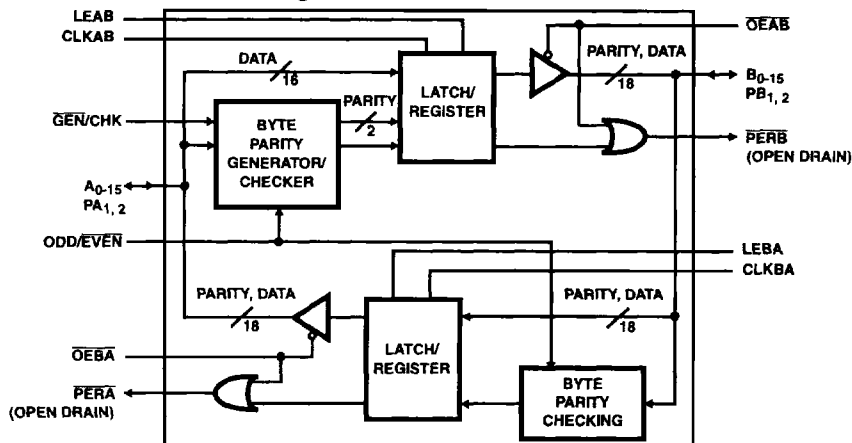
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16511TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Functional Block Diagram



Simplified Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS				OUTPUT BUFFERS
OEAB	LEAB	CLKAB	A _x	B _x
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B (Note 3)
L	L	H	X	B (Note 4)

NOTES:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
Z = High Impedance
↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A flow control is the same, except using OEBA, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

TRUTH TABLE (PARITY GENERATION) (NOTES 5, 6, 7, 8, 9)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A ₀ - A ₇	ODD/EVEN	PB ₁
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

5. Conditions shown are for GEN/CHK = L, OEAB = L, OEBA = H.
6. A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
7. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
8. Conditions shown are for the byte A₀-A₇. The byte A₈-A₁₅ is similar but will output the parity on PB₂.
9. The error flag PERB will remain in a high state during parity generation.

TRUTH TABLE (PARITY CHECKING) (NOTES 10, 11, 12, 13)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A ₀ - A ₇ AND PA ₁ (NOTE 14)	ODD/EVEN	PB ₁
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H (Note 15)
0, 2, 4, 6 or 8	L	H (Note 15)
0, 2, 4, 6 or 8	H	L

10. Conditions shown are for GEN/CHK = H, OEAB = L, OEBA = H.
11. A-to-B parity checking is shown. B-to-A parity checking is same but uses OEBA = L, OEAB = H and errors will be indicated on PERA.
12. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. (PB₁ = PA₁)
13. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
14. Conditions shown are for the byte A₀-A₇ and PA₁. The byte A₈-A₁₅ and PA₂ is same.
15. The parity error flag PERB is a combined flag for both bytes A₀-A₇ and A₈-A₁₅. If a parity error occurs on either byte PERB will go low.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEB A}$	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
A _X	A-to-B Data Inputs or B-to-A Three State Outputs
B _X	B-to-A Data Inputs or B-to-A Three State Outputs
ODD/ $\overline{EVEN}$ (Note 16)	Parity Mode Selection Input
$\overline{GEN/CHK}$ (Note 16)	A-to-B Port Generate or Check Mode Input
PA _X (Note 17)	A-to-B Parity Input, B-to-A Parity Output
PB _X	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
V _{CC}	Power

NOTES:

16. ODD/ $\overline{EVEN}$ and $\overline{GEN/CHK}$ should be tied to V_{CC} or GND with no resistor for optimum results.
17. The PA_X pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

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Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only -0.5V to 7.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

18. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 18) θ_{JA} (°C/W)
TSSOP Package 85
SSOP Package 70
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(Lead Tips Only)

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS		MIN	(NOTE 20) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%							
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current (Input Pins)	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input HIGH Current (I/O Pins)	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	-1	μA
Input LOW Current (Input Pins)	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	1	μA
Input LOW Current (I/O Pins)	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
High Impedance Output Current	I _{OZH}	V _{CC} = Max	V _{OUT} = 2.7V	-	-	1	μA
	I _{OZL}	V _{CC} = Max	V _{OUT} = 0.5V	-	-	-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current (I/O Pins)	I _{OS}	V _{CC} = Max (Note 21), V _{OUT} = GND		-80	-140	-225	mA
Output Drive Current (I/O Pins)	I _O	V _{CC} = Max (Note 21), V _{OUT} = 2.5V		-50	-	-180	mA
Output Leakage Current (Open Drain)	I _{OFF}	V _{CC} = Max, V _{OUT} = 4.5V		-	-	±100	μA
Input Hysteresis -	V _H			-	100	-	mV
CD74FCT16511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0mA	2.5	3.5	-	V
			I _{OH} = -15.0mA	2.4	3.5	-	V
			I _{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I _{OFF}	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		-	-	±100	μA
CD74FCT162511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I _{ODL}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 21)		60	115	150	mA
Output HIGH Current	I _{ODH}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 21)		-60	-115	-150	mA

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D.D. 5V FCT BAL-
AND HIGH DRIVE

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Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS	MIN	(NOTE 20) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$						
Input Capacitance (Note 22)	C_{IN}	$V_{IN} = 0\text{V}$	-	4.5	6.0	pF
I/O Capacitance (Note 22)	$C_{I/O}$	$V_{OUT} = 0\text{V}$	-	5.5	8.0	pF
Open Drain Capacitance (Note 22)	C_O	$V_{OUT} = 0\text{V}$	-	4.5	6.0	pF
POWER SUPPLY SPECIFICATIONS						
Quiescent Power Supply Current	I_{CCL} , I_{CCH} , I_{CCZ}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	500 μA
Supply Current per Input at TTL HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 23)	-	0.5	1.5 mA
Supply Current per Input per MHz (Note 24)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open $\overline{OEAB} = \text{GND}$ $\overline{OEBA} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	75	120 $\mu\text{A}/\text{MHz}$
Total Power Supply Current (Note 26)	I_C	$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $\overline{LEAB} = \overline{OEAB} = \text{GND}$ $\overline{OEBA} = V_{CC}$ $f_I = 5\text{MHz}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.8	1.7 mA (Note 25)
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.3	3.2 mA (Note 25)
		$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $\overline{LEAB} = \overline{OEAB} = \text{GND}$ $\overline{OEBA} = V_{CC}$ $f_I = 2.5\text{MHz}$ 18 Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.8	6.5 mA (Note 25)
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	9.0	21.8 mA (Note 25)

Switching Specifications Over Operating Range (Propagation Delays)

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T		AT		UNITS
			(NOTE 28) MIN	MAX	(NOTE 28) MIN	MAX	
Propagation Delay PAX to PBX	t_{PLH} t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	6.5	1.5	5.7	ns
Propagation Delay AX to BX or BX to AX , PBX to PAX	t_{PLH} t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	6.5	1.5	5.0	ns
Propagation Delay AX to PBX	t_{PLH} t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	9.0	1.5	7.5	ns
Propagation Delay AX to $\overline{PERB}$, PAX to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10.5	1.5	9.0	ns
			1.5	9.5	1.5	8.0	ns
Propagation Delay BX to $\overline{PERA}$, PBX to $\overline{PERA}$	t_{PLH} (Note 29) t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10.5	1.5	9.0	ns
			1.5	9.5	1.5	8.0	ns
Propagation Delay $\overline{LEBA}$ to AX and PAX , $\overline{LEAB}$ to BX and PBX	t_{PLH} t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	6.0	1.5	5.6	ns
Propagation Delay $\overline{LEBA}$ to $\overline{PERA}$, $\overline{LEAB}$ to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	7.5	1.5	7.0	ns
			1.5	6.5	1.5	6.0	ns

Switching Specifications Over Operating Range (Propagation Delays) (Continued)

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T		AT		UNITS
			(NOTE 28) MIN	MAX	(NOTE 28) MIN	MAX	
Propagation Delay CLKBA to A _X and PA _X CLKAB to B _X and PB _X	t _{PLH} t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	6.0	1.5	5.6	ns
Propagation Delay CLKBA to PERA CLKAB to PERB	t _{PLH} (Note 29) t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	7.5	1.5	7.0	ns
			1.5	6.5	1.5	6.0	ns
Output Enable Time OEBA to A _X and PA _X OEAB to B _X and PB _X	t _{PZH} t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	6.0	ns
Output Disable Time (Note 30) OEBA to A _X and PA _X OEAB to B _X and PB _X	t _{PHZ} t _{PLZ}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	5.6	ns
Parity ERROR Enable OEBA to PERA, OEAB to PERB	t _{PLZ} (Note 29) t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	6.0	1.5	6.0	ns
			1.5	6.0	1.5	6.0	ns
ODD/EVEN to PERB	t _{PLH} t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	10.0	ns
			1.5	10.0	1.5	10.0	ns
ODD/EVEN to PB _X	t _{PLH} t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	10.0	ns

Switching Specifications Over Operating Range (Setup Times)

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS				T		AT		UNITS
						MIN	MAX	MIN	MAX	
Setup Time HIGH or LOW A _X to CLKAB	t _{SU}	GEN/CHK LOW	PB _X valid	C _L = 50pF R _L = 500Ω	6.5	-	4	-	-	ns
			PB _X not valid		3	-	3	-	-	ns
		GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	4	-	-	ns
			PERB not valid		3	-	3	-	-	ns
Setup Time PA _X to CLKAB	t _{SU}	GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	4	-	-	ns
			PERB not valid		3	-	3	-	-	ns
Setup Time B _X to CLKBA PB _X to CLKBA	t _{SU}		PERA valid	C _L = 50pF R _L = 500Ω	6.5	-	4	-	-	ns
			PERA not valid		3	-	3	-	-	ns
Setup Time A _X to LEAB	t _{SU}	CLKAB LOW GEN/CHK LOW	PB _X valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	-	ns
			PB _X not valid		3	-	3	-	-	ns
		CLKAB LOW GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	-	ns
			PERB not valid		3	-	3	-	-	ns
		CLKAB HIGH GEN/CHK LOW	PB _X valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	-	ns
			PB _X not valid		3	-	3	-	-	ns
		CLKAB HIGH GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	-	ns
			PERB not valid		3	-	3	-	-	ns

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Switching Specifications Over Operating Range (Setup Times) (Continued)

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS			T		AT		UNITS
					MIN	MAX	MIN	MAX	
Setup Time P _{Ax} to LEAB	t _{SU}	CLKAB LOW GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	ns
			PERB not valid		3	-	3	-	ns
		CLKAB HIGH GEN/CHK HIGH	PERB valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	ns
			PERB not valid		3	-	3	-	ns
Setup Time B _X to LEBA PB _X to LEBA	t _{SU}	CLKBA LOW	PERA valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	ns
			PERA not valid		3	-	3	-	ns
		CLKAB HIGH	PERA valid	C _L = 50pF R _L = 500Ω	6.5	-	3.5	-	ns
			PERA not valid		3	-	3	-	ns

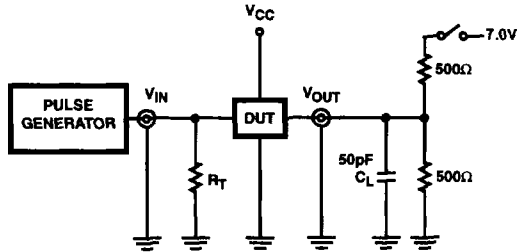
Switching Specifications Over Operating Range (Hold Times)

DESCRIPTION	SYMBOL	(NOTE 27) CONDITIONS	T		AT		UNITS
			MIN	MAX	MIN	MAX	
Hold Time HIGH or LOW A _X to LEAB, B _X to LEBA	t _H	C _L = 50pF R _L = 500Ω	1	-	1	-	ns
Hold Time HIGH or LOW P _{Ax} to LEAB	t _H		1	-	1	-	ns
Hold Time HIGH or LOW P _{Bx} to LEBA	t _H		1	-	1	-	ns
Hold Time A _X to CLKAB, P _{Ax} to CLKAB	t _H		1	-	1	-	ns
Hold Time B _X to CLKBA, P _{Bx} to CLKBA	t _H		1	-	1	-	ns
LEAB or LEBA Pulse Width HIGH (Note 30)	t _W		3	-	3	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 30)	t _W		3	-	3	-	ns

NOTES:

19. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
20. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
21. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
22. This parameter is determined by device characterization but is not production tested.
23. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
24. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
25. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
26. I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_{CC} = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.
27. See test circuit and wave forms.
28. Minimum limits are guaranteed but not tested on Propagation Delays.
29. On Open Drain Outputs t_{PLH} is measured up to V_{OUT} = V_{OL} + 0.3V.
30. This parameter is guaranteed but not production tested.
31. "Not Valid" means the setup time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.

Test Circuits and Waveforms



NOTE:

32. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{\text{OUT}} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

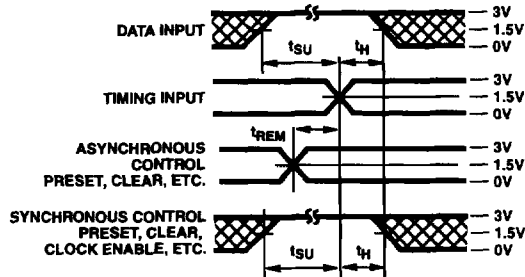


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION

TEST	SWITCH
$t_{\text{PLZ}}, t_{\text{PZL}}$	Closed
$t_{\text{PHZ}}, t_{\text{PZH}}, t_{\text{PLH}}, t_{\text{PHL}}$	Open

DEFINITIONS:

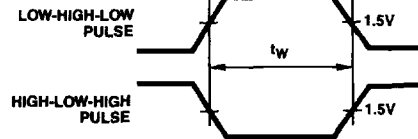
 C_L = Load capacitance, includes jig and probe capacitance. R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

FIGURE 3. PULSE WIDTH

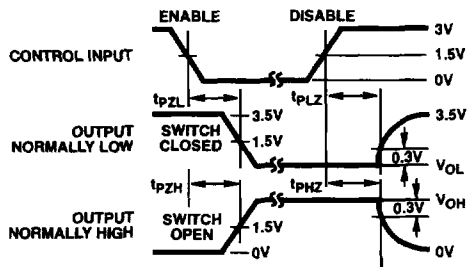


FIGURE 4. ENABLE AND DISABLE TIMING

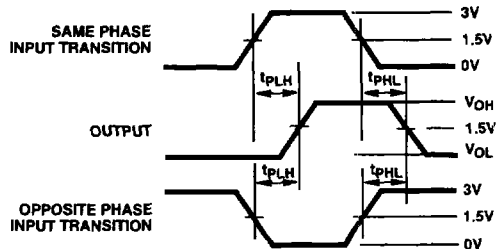


FIGURE 5. PROPAGATION DELAY

5

D.D. 5V FCT BAL.
AND HIGH DRIVE