32-Channel, 128-Level Amplitude Gray-Shade Display Column Driver

Features

- HVCMOS® technology
- 5.0V CMOS inputs
- Capable of 128 levels of gray shading
- Modulation voltage up to +80V
- 24MHz data throughput rate
- 32 outputs per device (can be cascaded)
- Pin-programmable shift direction (DIR)
- D/A conversion cycle time is 20µs
- Diodes in output structure allow usage in energy recovery systems
- Available in 3-sided 64-lead gull wing package

Applications

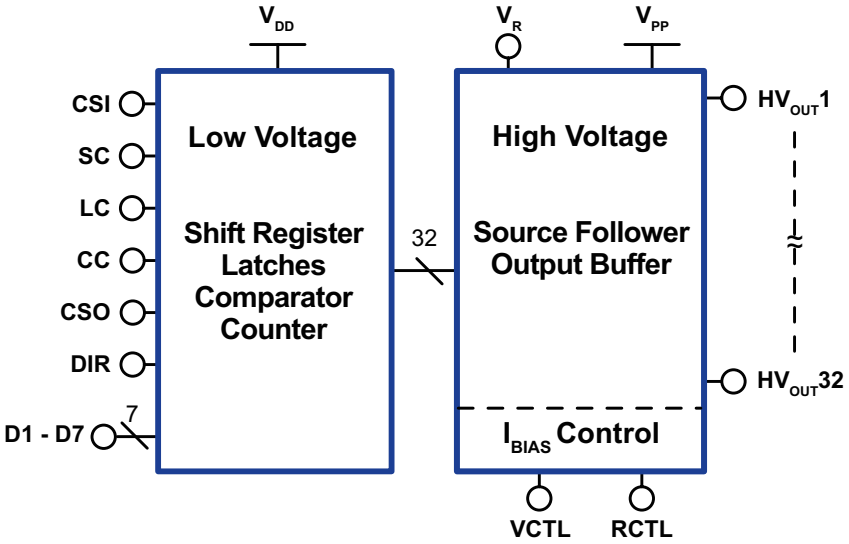
- Electroluminescent Displays
- Polycholesteric Displays

General Description

The HV633 is a 32-channel driver IC for gray shade display use. It is designed to produce varying output voltages between 3.0 - 80V. This amplitude modulation at the output is facilitated by an external ramp voltage V_R. See Theory of Operation for detailed explanation.

This device consists of dual 16-bit shift registers, 32 data latches and comparators, and control logic to preform 128 levels of gray shading. There are 7 bits of data inputs. Data is shifted through the shift registers at both edges of the clock, resulting in a data transfer rate of twice that of the shift clock frequency. When the DIR pin is high, CSI/CSO is the input/output for the chip select pulse. When DIR is low, CSI/CSO is the output/input for the chip select pulse. When the DIR pin is high, it allows the HV633 to shift data in the counter-clockwise direction when viewed from the top of the package. When the DIR pin is low, data is shifted in the clockwise direction. The output circuitry allows the energy which is stored in the output capacitance to be returned to V_{PP} through the body diode of the output transistor.

Functional Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV633PG-G	64-Lead PQFP	66/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

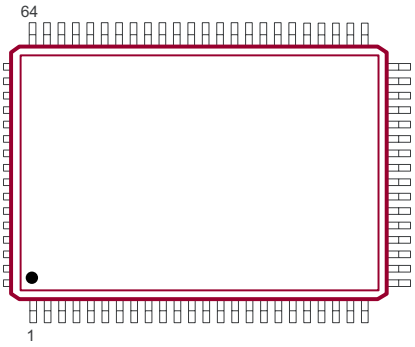
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.5V
Supply voltage, V_{PP}	-0.5V to +90V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[1]	1.5A
Operating temperature range	0°C to +125°C
Storage temperature range	-65°C to +150°C
Continuous total power dissipation[2]	2.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to 125°C at 20mW/°C.*

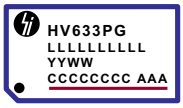
Pin Configuration



64-Lead PQFP
(top view)

Product Marking

Top Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
____ = "Green" Packaging

Package may or may not include the following marks: Si or

64-Lead PQFP

Typical Thermal Resistance

Package	θ_{ja}
64-Lead PQFP	41°C/W

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units
V_{DD}	Low-voltage digital supply voltage	4.5	5.0	5.5	V
	Low-voltage analog supply voltage				
V_{IH}	High-level input voltage (analog & digital)	V_{DD} -1	-	V_{DD}	V
V_{IL}	Low-level input voltage (analog & digital)	0	-	1.0	V
V_{BIAS}	I_{PP} control circuit bias voltage	-2.0	0	-	V
V_{CTL}	I_{PP} control circuit control voltage	-	0	2.0	V
V_{PP}	High voltage supply	-0.3	-	80	V
V_R	Ramp voltage	0	-	V_{PP} -2	V
f_{SC}	Shift clock operating frequency (at V_{DD} = 5.5V)	-	-	12	MHz

Electrical Characteristics *(over recommended operating conditions at T_A = 25°C unless otherwise noted)*

Low Voltage DC Characteristics (Digital)

Sym	Parameter	Min	Typ[1]	Max	Units	Conditions
I_{DD}	V_{DD} supply current	-	12	20	mA	f_{SC} = 12MHz, f_{CC} = 12MHz
I_{DDQ}	Quiescent V_{DD} supply current	-	-	200	µA	All V_{IN} = 0V, V_{DD} = 5.5V
I_{IH}	High-level input current	-	1.0	50	µA	V_{IH} = V_{DD}
I_{IL}	Low-level input current	-	-1.0	-50	µA	V_{IL} = 0V
C_{IN}[2]	Input capacitance (D1 ~ D7, LC, SC, CC)	-	-	15	pF	V_{IN} = 0V, f = 1.0MHz
I_{OH}	High-level output current	-2.0	-	-	mA	V_{DD} = 4.5V, V_{OH} = 0.9V_{DD}
I_{OL}	Low-level output current	2.0	-	-	mA	V_{DD} = 4.5V, V_{OL} = 0.1V_{DD}

Notes:

1. *All typical values are at V_{DD} = 5.0V.*
2. *Guaranteed by design.*

Low Voltage DC Characteristics (Analog)

I_{DD}	V_{DD} supply current	-	-	500	µA	f_{SC} = 12MHz, f_{CC} = 12MHz
I_{DDQ}	Quiescent V_{DD} supply current	-	-	200	µA	All V_{IN} = 0V, V_{DD} = 5.5V

High Voltage Bias Circuit for Output Variation Control

I_{PP}	V_{PP} supply current for bias circuit	-	2.0	-	mA	Depending on external bias circuit, see Table 1.

High Voltage DC Characteristics

I_{AOH}	High-voltage analog output source current	See performance curves			mA	V_{PP} = 80V. See Test Circuit
I_{AOL}	High-voltage analog output sink current	See performance curves			mA	V_{PP} = 80V, V_{DD} = 4.5V, V_{AO} = 2.0V
ΔV_O	Maximum delta voltage between high voltage outputs of the same level	-	-	±0.2	V	At all gray levels

AC Characteristics *(V_{DD} = 5.5V, T_A = 25°C)*

Logic Timing

f_{SC}	Shift clock operating frequency	-	-	12	MHz	---
f_{DIN}	Data-in frequency	-	-	24	MHz	---
t_{SS}	CSI/CSO pulse to shift clock setup time	-	40	-	ns	---
t_{HS}	CSI/CSO pulse to shift clock hold time	-	0	-	ns	---
t_{WA}	CSI pulse width	-	49	-	ns	---
t_{DS}	Data to shift clock setup time	-	20	-	ns	---
t_{DH}	Data to shift clock hold time	-	0	-	ns	---
t_{WD}	Data-in pulse width	-	24	-	ns	---
t_{WLC}	Load count pulse width	-	98	-	ns	---
t_{DLCR}	Load count to ramp delay	1.0	-	-	µs	---
t_{DRCC}[3]	Ramp to count clock delay	0.47	-	-	µs	---
t_{DSL}	Shift clock to load count delay time	-	98	-	ns	---

Logic Timing *(cont.)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{CSC}	Shift clock cycle time	98	-	-	ns	---
t_{WSC}	Shift clock pulse width	49	-	-	ns	---
t_{CCC}	Count clock cycle time	98	-	-	ns	---
t_{WCC}	Count clock pulse width	49	-	-	ns	---

V_R Timing

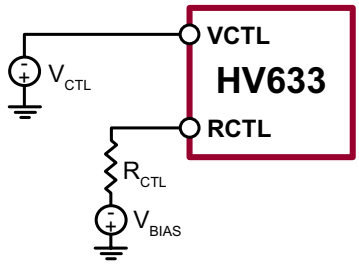
t_{CR}	Cycle time of ramp signal	15	-	-	µs	---
t_{RR}	Ramp rise time	10.6	-	-	µs	---
t_{HR} [4]	Ramp hold time	2.0	-	15	µs	---
t_{FR}	Ramp fall time	3.0	-	-	µs	C_{LOAD} = 1nF

Notes:

3. *Count clock starts counting after 0.47µs min. This is equivalent to a time duration for a linear ramp V_R to ramp from 0 to 3.0V, assuming the minimum value of t_{RR}, ramp size time of 12µs for V_R = 80V.*
4. *The maximum ramp hold time may be longer than 15 µs, but the output voltage HV_{OUT} will droop due to leakage.*

Table 1: Schemes to control I_{PP} bias current, typical I_{PP}

Option 1				Option 2			
V_{BIAS} (V)	V_{CTL} (V)	R_{CTL} (kΩ)	I_{PP} (mA)	V_{BIAS} (V)	V_{CTL} (V)	R_{CTL} (kΩ)	I_{PP} (mA)
0	0.1	56	2.0	-1.0	0	56	4.0
0	1.0	56	7.0	-2.0	0	56	5.5



Function Table

Function	DIR	Data In (D1 - D7)	CSI	CSO	SC	LC	CC	V_R	HV_{OUT}
Shift data from $HV_{OUT}1$ to $HV_{OUT}32$	H	Data	⎍	Output	⎍	L	L	L	Data → $HV_{OUT}1$ → ...→ $HV_{OUT}32$
Shift data from $HV_{OUT}32$ to $HV_{OUT}1$	L	Data	Output	⎍	⎍	L	L	L	Data → $HV_{OUT}32$ → ...→ $HV_{OUT}1$
Load shift register	X	X	Pre-defined by 1 or 2		⎍	L	L	L	-
Load counter	X	X			L	⎍	L	L	-
Counting/voltage conversion	X	X			L	L	⎍	Initiates V_R	-

Notes:

L = Low logic level

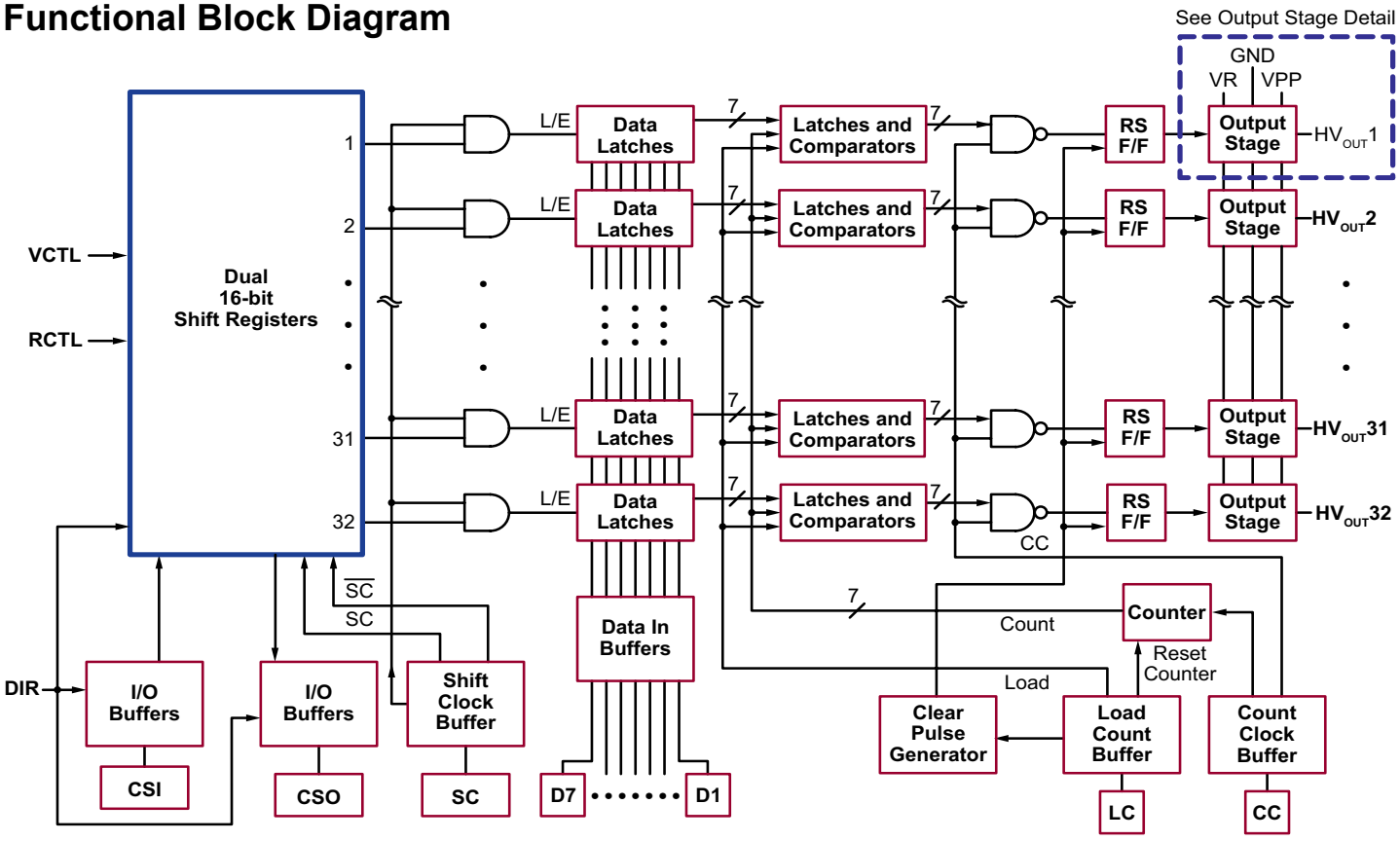
H = High logic level

⎍ *= Low to high transition*

⎍ *= Transition of both edges*

X = Don't care

Functional Block Diagram

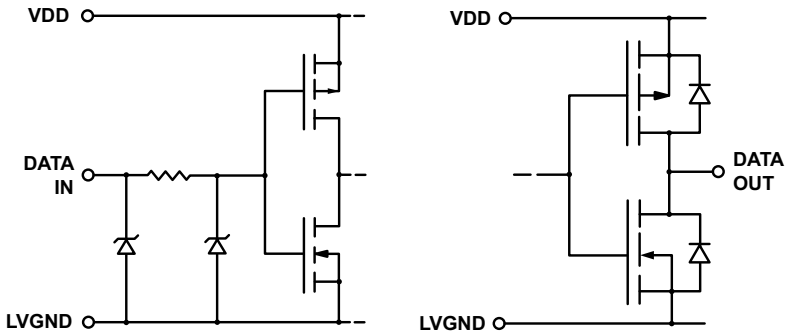


Note:

SC = Shift Clock, LC = Load Count, CC = Count Clock, CSI = Chip Select Input, CSO = Chip Select Output

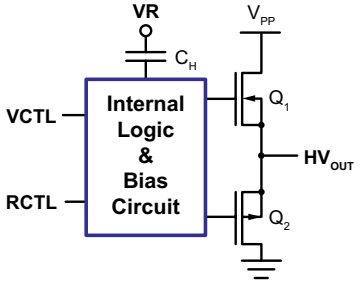
**Data rate = 2x the SC frequency*

Input and Output Equivalent Circuits



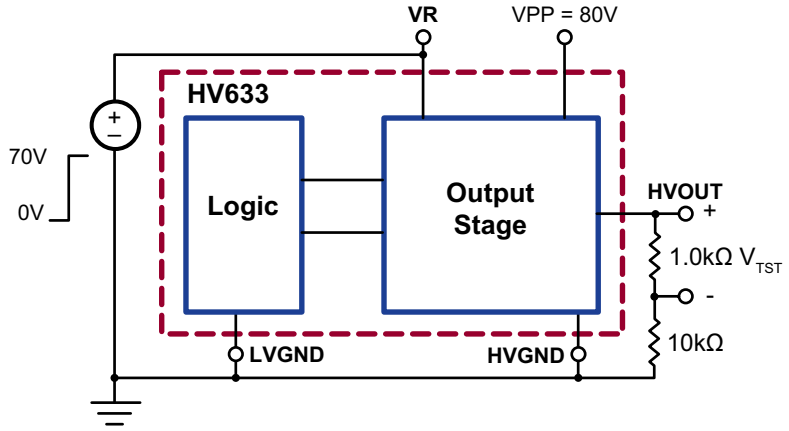
Logic Inputs **Logic Data Output**

Output Stage Detail



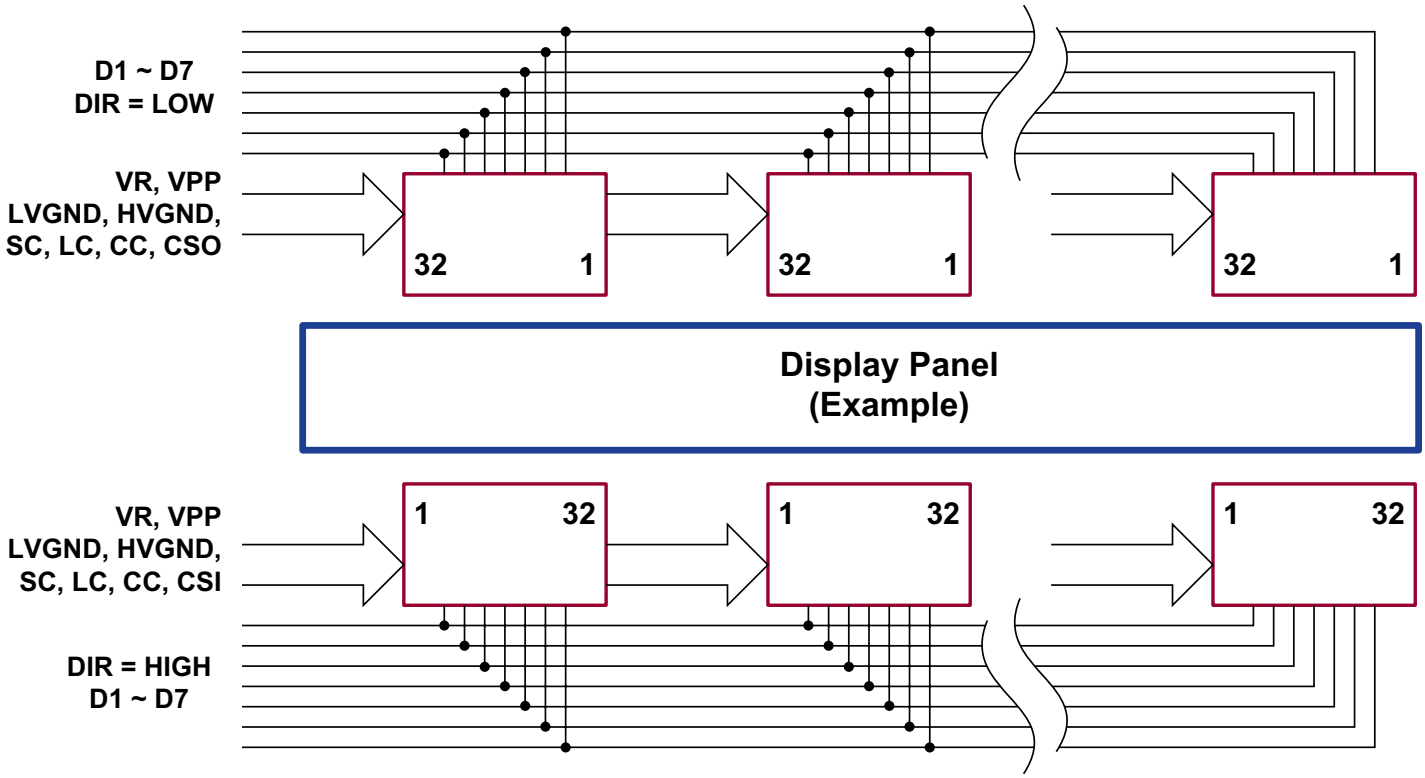
Test Circuit

High-voltage Analog Output Source Current (I_{AOH}). For gray shade #1 (000 0000).



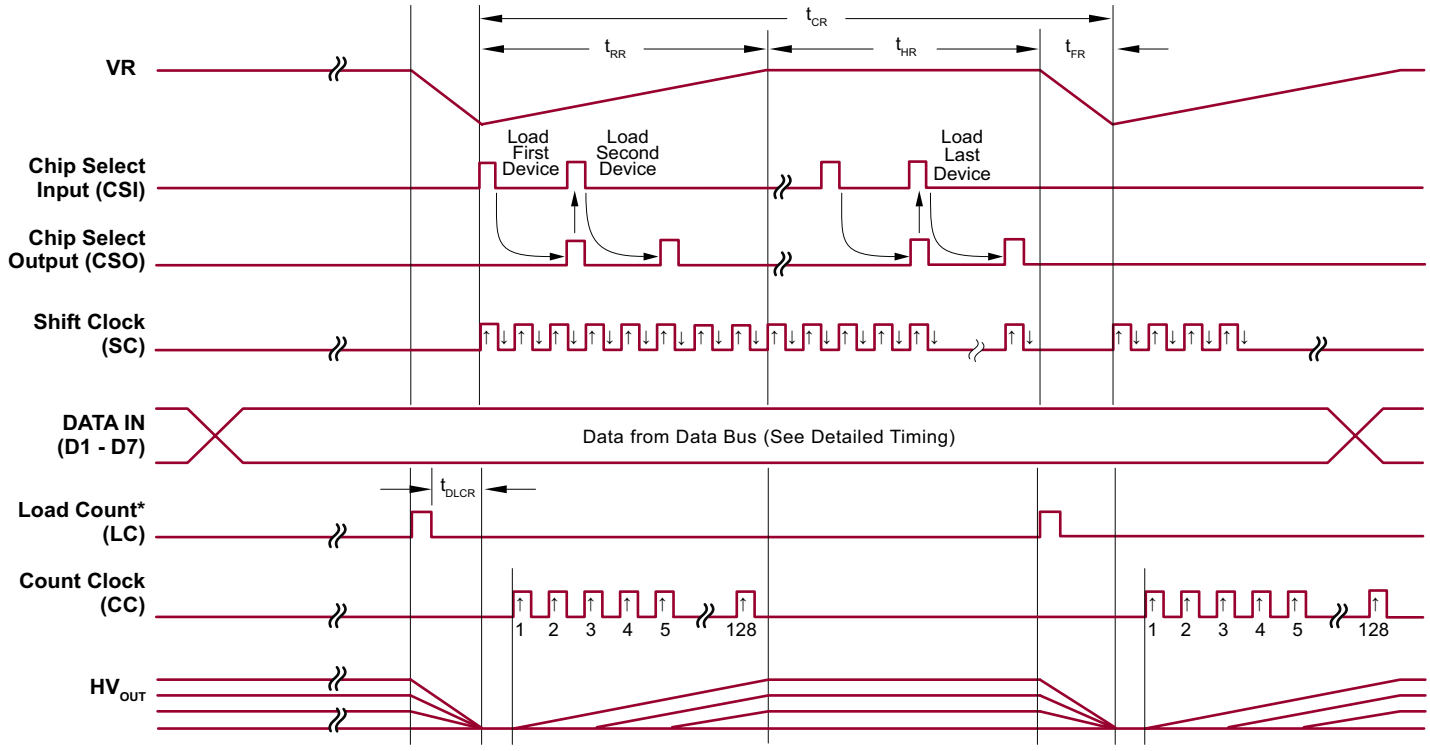
1. *Set HV_{OUT} = Low*
2. *Apply V_{PP} = 80V*
3. *Apply a step voltage of 70V at V_R (slew rate = 4.1V/µs)*
4. *Measure voltage across the 1.0KΩ resistor*
5. *Output source current can be calculated by using V_{TST}/1.0KΩ*

Typical Panel Connections



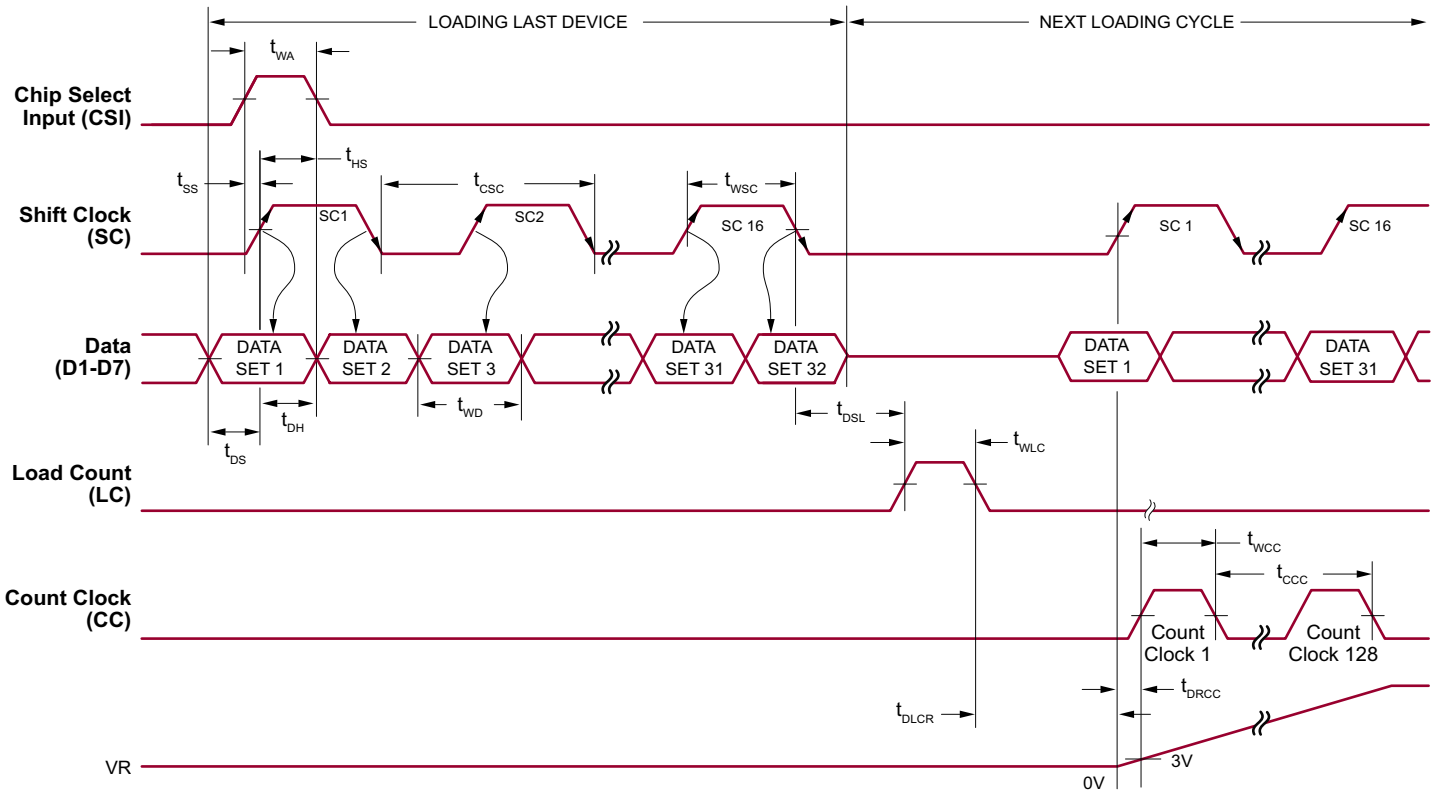
Timing Diagrams

(a) Basic System Timing



HV_{OUT} will clear to zero with load count.

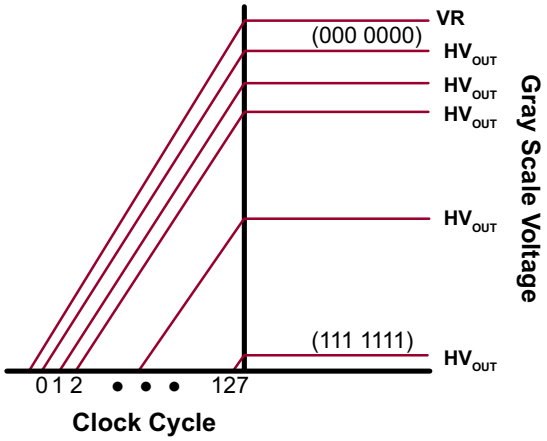
(b) Detailed Device Timing



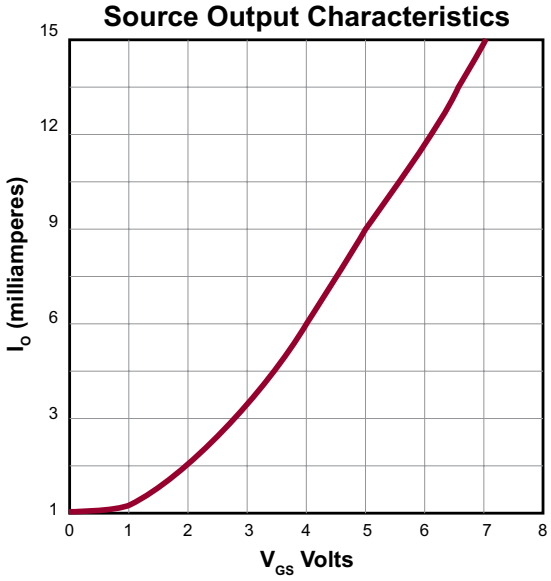
Gray Shade Decoding Scheme

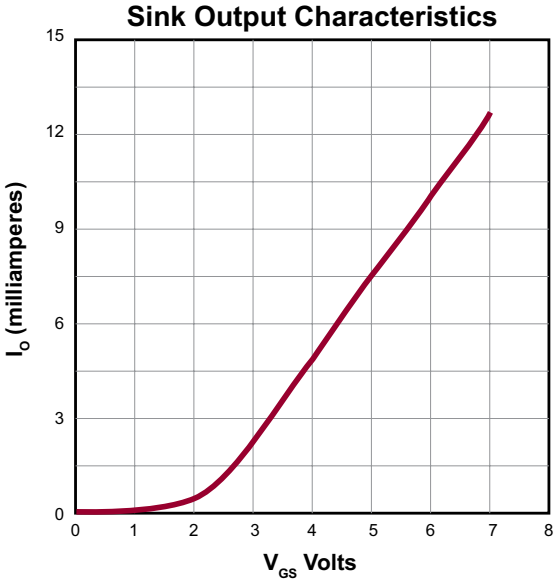
Shade Number	D7	D6	D5	D4	D3	D2	D1
128	1	1	1	1	1	1	1
127	1	1	1	1	1	1	0
126	1	1	1	1	1	0	1
125	1	1	1	1	1	0	0
124	1	1	1	1	0	1	1
123	1	1	1	1	0	1	0
122	1	1	1	1	0	0	1
121	1	1	1	1	0	0	0
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
7	0	0	0	0	1	1	0
6	0	0	0	0	1	0	1
5	0	0	0	0	1	0	0
4	0	0	0	0	0	1	1
3	0	0	0	0	0	1	0
2	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0

Gray Scale Voltage



Typical Performance Curves





Theory of Operation

The HV633 has two primary functions:

1) Loading data from the data bus and,

2) Gray-shade conversion(converting latched data to output voltages).

Since the device was developed initially for flat panel displays, the operation will be described in terms that pertain to that technology. As shown by the Typical Panel Connections, several HV633 packages are mounted at the top and bottom of a display panel. Data exists on a 7-bit bus (adjacent PC board traces) at top and bottom. The D1 through D7 inputs of each chip take data from the bus when either a CSI or CSO pulse is present at the chip. These pulses therefore act as a combination CHIP SELECT and LOCATION STROBE. Because of the way the chip HV_{OUT} pins are sequenced, data on the bus at the bottom of the display panel will be entered into the left-most chip as $HV_{OUT}1$, $HV_{OUT}2$, etc. up to $HV_{OUT}32$. The CSI pulse will accomplish this with DIR = High.

Loading Data from Data Bus

Here is the full data-entry sequence:

1) The micro controller puts data on the bus (7 bits)

2) To enter the data into the 32 sets of 7 latches on the first chip, the shift clock rises. This positive transition is combined with the CSI pulse and is generated only once to strobe the data into the first set of latches. (These latches eventually send data to the $HV_{OUT}1$). The data on the bus then changes, the shift clock falls, and this negative transition is combined with the CSI pulse, which is now propagated internally, to strobe the new data into the next set of 7 latches (which will end up as $HV_{OUT}2$). This internal CSI pulse therefore runs at twice the shift clock rate.

3) When the last set of 7 latches in the first chip has been loaded ($HV_{OUT}32$), the CSI pulse leaves chip 1 and enters chip 2. The exit pin is called CSO and the chip 2 entry pin is CSI. For chips at the top of the panel things are reversed: DIR is low, entry pins are CSO and exit pins are CSI, because the data-into-latches sequence is in descending order, $HV_{OUT}32$ down to $HV_{OUT}1$.

4) The buses may of course be separate, and data can be strobed in on an interleaved basis, etc., but those complications will be left to systems designers.

When data has been loaded into all 32 outputs of all chips (top and bottom of the display panel), the load count pin is pulsed. On its rising transition, all output levels are reset to zero and all the data in the input latches is transferred to a like number of comparator latches, (thus leaving the data latches ready to receive new data during the following operations). After the transfer, the load count pin is brought low. This transition begins the events that convert the binary data into a gray-shade level.

Gray-shade Conversion

1) The COUNT CLOCK is started. An external signal is applied to the COUNT CLOCK pin, causing the counter on each chip to increment from binary 000 0000 to 111 1111 (0 to 127).

2) At the same time, the V_R voltage is applied to all chips, via charging transistors, causing the HOLD CAPACITOR (CH) on each output to experience a rise in voltage.

3) The logic control compares the count in the comparator latch to the count clock. The gate voltage of Q1 and the output voltage HV_{OUT} will ramp up at the same rate as VR.

4) Once V_R has reached the maximum voltage, then all the pixels will be at the final value. (See Gray Scale Voltage.)

Output Voltage Variation

The output voltage of the HV633 is determined by the logic and the ramp voltage V_R. It is possible that the output voltage may be coupled to an unacceptable level due to its adjacent outputs through the panel. In order to solve this problem, internal logic (refer to Output Stage Detail) is integrated in the IC to minimize the effect. Two external pins VCTL and RCTL allow the feasibility to control the current flowing through Q2. The VCTL pin is connected to a voltage source and the RCTL pin is connected to ground through a resistor (2.0V and 56KΩ are used for a particular panel). The internal bias circuit will drive the resistor to a voltage level that is equal to the VCTL voltage at steady state through an operational amplifier. The current flowing through Q1 and Q2 will be limited to VCTL/RCTL. This combination of VCTL and RCTL will reduce the output voltage variation to less than ±0.2V of delta voltage for each gray shade, independent of its adjacent output voltages.

Pin Descriptions

Pin #	Function	Description
1	$HV_{OUT}1$	High-voltage outputs
2	$HV_{OUT}2$	
3	$HV_{OUT}3$	
4	$HV_{OUT}4$	
5	$HV_{OUT}5$	
6	$HV_{OUT}6$	
7	$HV_{OUT}7$	
8	$HV_{OUT}8$	
9	$HV_{OUT}9$	
10	$HV_{OUT}10$	
11	$HV_{OUT}11$	
12	$HV_{OUT}12$	
13	$HV_{OUT}13$	
14	$HV_{OUT}14$	
15	$HV_{OUT}15$	
16	$HV_{OUT}16$	
17	HVGND	This is ground for the high-voltage (output) section. HVGND and LVGND should be connected together externally.
18	VR	High voltage ramp input for charging the output stage hold capacitors (CH). This input can be linear or non-linear as desired.
19	VPP	This input biases the output source followers.
20	NC	No connect.
21	VDD (analog)*	Low-voltage analog supply voltage.
22	CSI	Input pin for the chip select pulse (when DIR is high). Output pin for the chip select pulse (when DIR is low).
23	NC	No connect.
24	VCTL	Voltage supply pin to prevent output voltage from being affected by its adjacent outputs (V_{CTL} = 2.0V for a particular panel). The combination of V_{CTL} and R_{CTL} will reduce the output voltage variation to less than ±0.2V of delta voltage between high voltage outputs of the same level at all gray levels.
25	RCTL	Current sense resistor to ground to prevent output voltage from being affected by its adjacent outputs (R_{CTL} = 56KΩ for a particular panel). See VCTL function above.
26	SC (shift clock)	Triggers data on both rising and falling edges. This implies that the data rate is always twice the clock rate (data rate = 20MHz if clock rate = 10MHz).
27	LVGND	This is ground for the logic section. HVGND and LVGND should be connected together externally.
28	DIR	When this pin is connected to VDD, input data is shifted in ascending order, i.e., corresponding to $HV_{OUT}1$ to $HV_{OUT}32$. When connected to LVGND, input data is shifted in descending order, i.e., corresponding to $HV_{OUT}32$ to $HV_{OUT}1$.
29	VDD (digital)*	Low-voltage digital supply voltage.

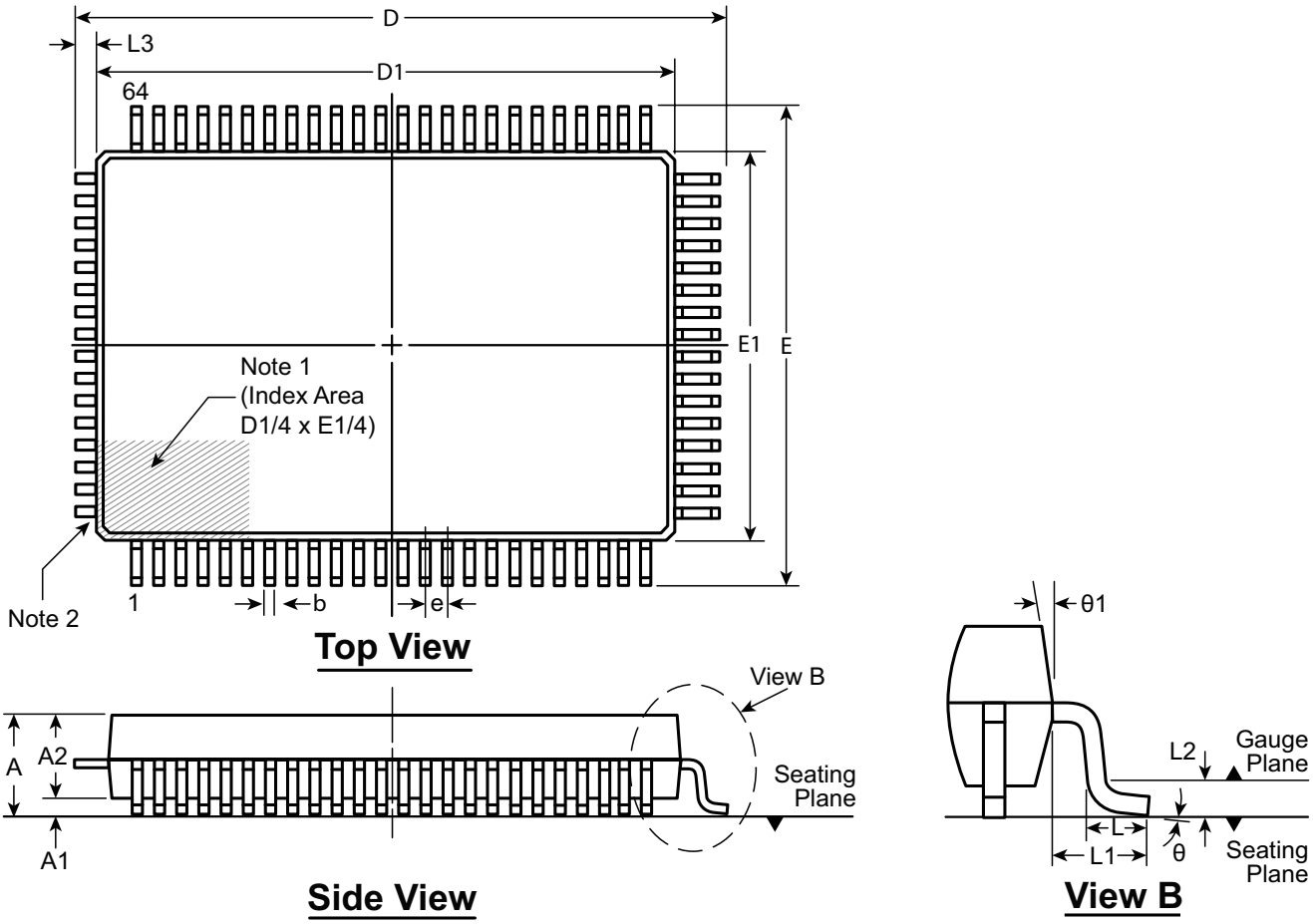
* *Analog VDD and digital VDD may be connected seperately for better noise immunity.*

Pin Descriptions *(cont.)*

Pin #	Function	Description
30	D7	Inputs for binary-format parallel data.
31	D6	
32	D5	
33	D4	
34	D3	
35	D2	
36	D1	
37	NC	No connect.
38	LVGND	This is ground for the logic section. HVGND and LVGND should be connected together externally.
39	NC	No connect.
40	LC (Load Count)	Input for a pulse whose rising edge causes data from the input latches to enter the comparator latches, and whose falling edge initiates the conversion of this binary data to an output level (D-to-A). Also, the HV_{OUT} will clear to zero after the load count is initiated.
41	NC	No connect.
42	CC (Count Clock)	Input to the count clock generator whose increments are compared to the data in the comparator latches.
43	CSO	Input pin for the chip select pulse (when DIR is low). Output pin for the chip select pulse (when DIR is high).
44	NC	No connect.
45	VPP	This input biases the output source followers.
46	NC	No connect.
47	VR	High-voltage ramp input for charging the output stage hold capacitors (CH).This input can be linear or non-linear as desired.
48	HVGND	This is ground for the high-voltage (output) section. HVGND and LVGND should be connected together externally.
49	$HV_{OUT}17$	High-voltage outputs
50	$HV_{OUT}18$	
51	$HV_{OUT}19$	
52	$HV_{OUT}20$	
53	$HV_{OUT}21$	
54	$HV_{OUT}22$	
55	$HV_{OUT}23$	
56	$HV_{OUT}24$	
57	$HV_{OUT}25$	
58	$HV_{OUT}26$	
59	$HV_{OUT}27$	
60	$HV_{OUT}28$	
61	$HV_{OUT}29$	
62	$HV_{OUT}30$	
63	$HV_{OUT}31$	
64	$HV_{OUT}32$	

64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The leads on this side are trimmed.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1
Dimen-sion (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.
Supertex Doc. #: *DSPD-64PQFPPG, Version NR090608.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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