

✓ 54/74199 016749

8-BIT PARALLEL I/O SHIFT REGISTER

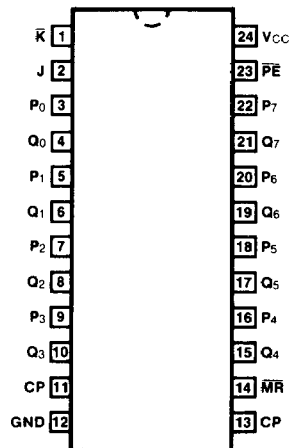
DESCRIPTION — The '199 is a parallel in, parallel out register featuring synchronous parallel load, shift right and hold modes. State changes are initiated by the rising edge of the clock. Serial entry into the first stage is via J and \bar{K} inputs for maximum flexibility. Two clock inputs are provided and it is possible to use one as an inhibit. An asynchronous Master Reset (\overline{MR}) input overrides all other inputs and clears the register.

- PARALLEL IN/PARALLEL OUT
- SYNCHRONOUS PARALLEL LOAD
- ASYNCHRONOUS OVERRIDING CLEAR
- JK ENTRY TO FIRST STAGE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74199PC		9N
Ceramic DIP (D)	A	74199DC	54199DM	6N
Flatpak (F)	A	74199FC	54199FM	4M

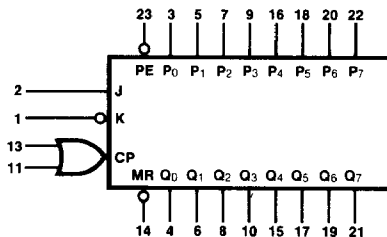
CONNECTION DIAGRAM PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
\bar{K}	Serial Data Input (Active LOW)	1.0/1.0
J	Serial Data Input (Active HIGH)	1.0/1.0
$P_0 - P_7$	Parallel Data Inputs	1.0/1.0
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
\overline{PE}	Parallel Enable Input (Active LOW)	1.0/1.0
$Q_0 - Q_7$	Flip-flop Outputs	20/10

LOGIC SYMBOL







$V_{CC} = \text{Pin } 24$
 $GND = \text{Pin } 12$

FUNCTIONAL DESCRIPTION — The '199 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load and shift right operations. Parallel input data is applied to the $P_0 - P_7$ inputs, while serial entry to Q_0 is via J and \bar{K} . State changes are initiated by the rising edge of the clock. The J, \bar{K} , $P_0 - P_7$ and \overline{PE} inputs can change while the clock is in either state, provided only that the recommended setup and hold times are observed.

Either CP input can be used as the clock; if one is not used it must be tied LOW. One CP input can be used to inhibit the other by applying a HIGH signal, but this should only be done while the other CP is in the HIGH state or else false triggering may result. A LOW signal on \overline{MR} overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
\overline{MR}	\overline{PE}	CP ₁ *	CP ₂ *	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H	X	H	X	Hold
H	X	X	H	
H	L	L		Parallel Load; $P_n \rightarrow Q_n$
H	L		L	
H	H	L		Shift Right, $Q_0 \rightarrow Q_1, Q_1 \rightarrow Q_2, \text{etc.}$
H	H		L	

*See discussion for precautions on CP changes

H = HIGH Voltage Level

L = LOW Voltage Level

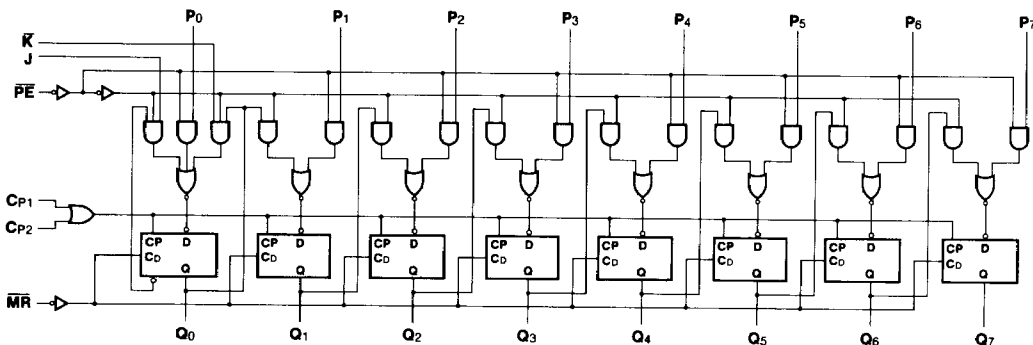
X = Immaterial

SERIAL ENTRY TABLE
($\overline{MR} = \overline{PE} = \text{HIGH}$)


INPUTS		Q_0 at $t_n + 1^*$
J	\bar{K}	
L	L	L
L	H	Q_0 at t_n (No Change)
H	L	$\overline{Q_0}$ at t_n (Toggles)
H	H	H

* $t_n, t_n + 1 =$ time before, after rising CP edge

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		UNITS	CONDITIONS
			Min	Max		
I _{CC}	Power Supply Current	XC	116		mA	V _{CC} = Max; J, \bar{K} , P _n = 4.5 V CP ₁ =  CP ₂ , \bar{MR} , \bar{PE} = Gnd
		XM	104			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74		UNITS	CONDITIONS
			C _L = 15 pF R _L = 400 Ω			
			Min	Max		
f _{max}	Maximum Shift Frequency		25		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP ₁ or CP ₂ to Q _n		26 30		ns	Figs. 3-1, 3-8
t _{PHL}	Propagation Delay \bar{MR} to Q _n		35		ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74		UNITS	CONDITIONS	
			Min	Max			
t _s (H) t _s (L)	Setup Time HIGH or LOW P _n , \bar{K} , J to CP		20 20		ns	Fig. 3-6	
t _h (H) t _h (L)	Hold Time HIGH or LOW P _n , \bar{K} , J to CP		0 0				
t _s (H) t _s (L)	Setup Time HIGH or LOW \bar{PE} to CP		30 30		ns		
t _h (H) t _h (L)	Hold Time HIGH or LOW \bar{PE} to CP		0 0		ns		
t _w (H)	CP Pulse Width HIGH		20		ns		Fig. 3-8
t _w (L)	\bar{MR} Pulse Width LOW		20		ns		Fig. 3-16