

REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED				
A	Drawing updated to reflect current requirements. - lgt										01-11-07				Raymond Monnin				
B	Redrawn. Paragraphs updated to MIL-PRF-38535 requirements. - drw										13-04-11				Charles F. Saffle				
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.																			
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REV STATUS				REV		B	B	B	B	B	B	B	B	B	B	B			
OF SHEETS				SHEET		1	2	3	4	5	6	7	8	9	10				
PMIC N/A				PREPARED BY Rick C. Officer						<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a>									
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A				CHECKED BY Charles E. Besore															
				APPROVED BY Michael A. Frye															
				DRAWING APPROVAL DATE 89-12-04															
				REVISION LEVEL B															
						SIZE A	CAGE CODE <b>67268</b>			<b>5962-89669</b>									
						SHEET 1 OF 10													

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89669	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	SW-06B	Quad SPST JFET analog switch

1.2.2 Case outlines. The case outline) are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V+ supply to V- supply .....	36 V dc
V+ supply to ground .....	36 V dc
Logic input voltage range .....	(-4 V or V- supply) to V+ supply
Analog input voltage range continuous .....	V- supply to V+ supply +20 V dc
Maximum current through any pin including switch.....	30 mA
Storage temperature range .....	-65°C to +150°C
Power dissipation (P <sub>D</sub> ) :	
Case E .....	900 mW
Case 2 .....	500 mW
Lead temperature (soldering, 60 seconds).....	+300°C
Maximum junction temperature range (T <sub>J</sub> ) .....	+150°C
Thermal resistance, junction to case (θ <sub>JC</sub> ).....	See MIL-STD-1835
Thermal resistance, junction to ambient (θ <sub>JA</sub> )	
Cases E .....	91°C/W max
Cases 2 .....	110°C/W max

1.4 Recommended operating conditions.

Positive supply voltage (V+).....	+15 V dc
Negative supply voltage (V-) .....	-15 V dc
Ambient operating temperature range (T <sub>A</sub> ) .....	-55°C to +125°C
High input voltage (V <sub>IH</sub> ) .....	2.0 V dc
Low input voltage (V <sub>IL</sub> ) .....	0.8 V dc

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>±</sub> = ±15 V, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive supply current	I <sub>+</sub>	All switches OFF	1	All		6	mA
			2, 3			9	
Negative supply current	I <sub>-</sub>	All switches OFF	1	All		-5.0	mA
			2, 3			-7.5	
Ground current	I <sub>G</sub>	All switches OFF or ON	1	All		4	mA
			2, 3			6	
Logic "0" input current	I <sub>IL</sub>	V <sub>IN</sub> = 0.8 V	1	All		5	μA
			2, 3			10	
Logic "1" input current <u>1/</u>	I <sub>IH</sub>	V <sub>IN</sub> = 2 V to 15 V	1	All		5	μA
			2, 3			10	
"ON" resistance	R <sub>ON</sub>	V <sub>S</sub> = ±10 V, I <sub>S</sub> = 1 mA	1	All		80	Ω
			2, 3			110	
ΔR <sub>ON</sub> vs V <sub>A</sub>	ΔR <sub>ON</sub>	V <sub>S</sub> = ±10 V, I <sub>S</sub> = 1 mA	1	All		15	%
R <sub>ON</sub> match between switches <u>2/</u>	R <sub>ON</sub> (match)	V <sub>S</sub> = 0 V, I <sub>S</sub> = 100 μA	1	All		10	%
			2, 3			20	
Logic "1" input voltage <u>3/</u>	V <sub>IH</sub>		1, 2, 3	All	2.0		V
Logic "0" input voltage <u>3/</u>	V <sub>IL</sub>		1, 2, 3	All		0.8	V
Analog voltage range <u>3/</u>	V <sub>A</sub>	I <sub>S</sub> = 1 mA	1, 2, 3	All	±10		V
Analog current range <u>4/</u>	I <sub>A</sub>	V <sub>S</sub> = ±10 V <u>5/</u>	1	All	10		mA
			2, 3		7		
Source current switches OFF	I <sub>S(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V	1	All		2	nA
			2, 3			60	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>±</sub> = ±15 V, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Drain current switches OFF	I <sub>D(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V	1	All		2	nA
			2, 3			60	
Source current switch ON	I <sub>S(ON)</sub> + I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±10 V	1	All		2	nA
			2			100	
Turn-on-time	t <sub>ON</sub>	V <sub>S</sub> = -5 V, R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	9	All		500	ns
			10, 11 <u>6/</u>			900	
Turn-off-time	t <sub>OFF</sub>	V <sub>S</sub> = -5 V, R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	9	All		400	ns
			10, 11 <u>6/</u>			500	
Source capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, see 4.3.1c	4	All		7.0	pF
Drain capacitance	C <sub>D(OFF)</sub>	V <sub>S</sub> = 0 V, see 4.3.1c	4	All		5.5	pF
Channel "ON" capacitance	C <sub>D(ON)</sub> and C <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V <u>5/</u>	4	All		15	pF
"OFF" isolation	I <sub>SO(OFF)</sub>	V <sub>S</sub> = 5 V, R <sub>L</sub> = 680Ω, C <sub>L</sub> = 7 pF, f = 500 kHz	4	All	50		dB
Crosstalk	C <sub>T</sub>	V <sub>S</sub> = 5 V, R <sub>L</sub> = 680Ω, C <sub>L</sub> = 7 pF, f = 500 kHz	4	All	60		dB
Functional test		see 4.3.1d	7, 8	All			
Break-before-make time	t <sub>ON</sub> - t <sub>OFF</sub>		9	All	20		ns

1/ Current tested at V<sub>IN</sub> = 2 V (worst case condition).

2/ R<sub>ON</sub> match specified as a percentage of R<sub>average</sub> where :  

$$R_{average} = \frac{(RON1 + RON2 + RON3 + RON4)}{4}$$

3/ V<sub>A</sub>, V<sub>IH</sub>, and V<sub>IL</sub> is verified by leakage and R<sub>ON</sub> tests.

4/ I<sub>A</sub> is defined as follows: For analog currents less than or equal to I<sub>A</sub> min. the switch channel "ON" resistance will not exceed twice the specified R<sub>ON</sub> for that device grade.

5/ This parameter is derived from a calculation of "OFF" isolation test.

6/ If not tested, shall be guaranteed to the limits specified in table I.

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Device type	01	
Case outline	E	2
Terminal number	Terminal symbol	
1	IN <sub>1</sub>	NC
2	D <sub>1</sub>	IN <sub>1</sub>
3	S <sub>1</sub>	D <sub>1</sub>
4	GND	S <sub>1</sub>
5	V-	GND
6	S <sub>2</sub>	NC
7	D <sub>2</sub>	V-
8	IN <sub>2</sub>	S <sub>2</sub>
9	IN <sub>3</sub>	D <sub>2</sub>
10	D <sub>3</sub>	IN <sub>2</sub>
11	S <sub>3</sub>	NC
12	V+	IN <sub>3</sub>
13	DISABLE	D <sub>3</sub>
14	S <sub>4</sub>	S <sub>3</sub>
15	D <sub>4</sub>	V+
16	IN <sub>4</sub>	NC
17	-----	DISABLE
18	-----	S <sub>4</sub>
19	-----	D <sub>4</sub>
20	-----	IN <sub>4</sub>

FIGURE 1. Terminal connections.

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Disable input	Logic input	Switch state	
		Channels 1 and 2	Channels 3 and 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

NC = No connection

FIGURE 2. Truth table.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{S(OFF)}$  and  $C_{D(OFF)}$  measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I herein.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535 . The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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## STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-04-11

Approved sources of supply for SMD 5962-89669 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8966901EA	24355	SW06BQ/883
5962-89669012A	24355	SW06BRC/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

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Vendor name  
and address

Analog Devices, Inc.  
Rt. 1 Industrial Park  
P.O. Box 9106  
Norwood, MA 02062  
Point of Contact:  
804 Woburn Street  
Wilmington, MA 01887-3462

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