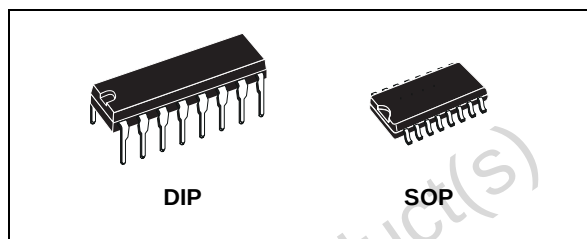




HCF4014B

SYNCHRONOUS PARALLEL OR SERIAL IN/SERIAL OUT 8 - STAGE STATIC SHIFT REGISTER

- MEDIUM SPEED OPERATION :
12 MHz (Typ.) At $V_{DD} = 10V$
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS
OUTPUT BUFFERING AND CONTROL
GATING
- QUIESCENT CURRENT SPECIFIED UP TO
20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC
JESD13B " STANDARD SPECIFICATIONS
FOR DESCRIPTION OF B SERIES CMOS
DEVICES"



ORDER CODES

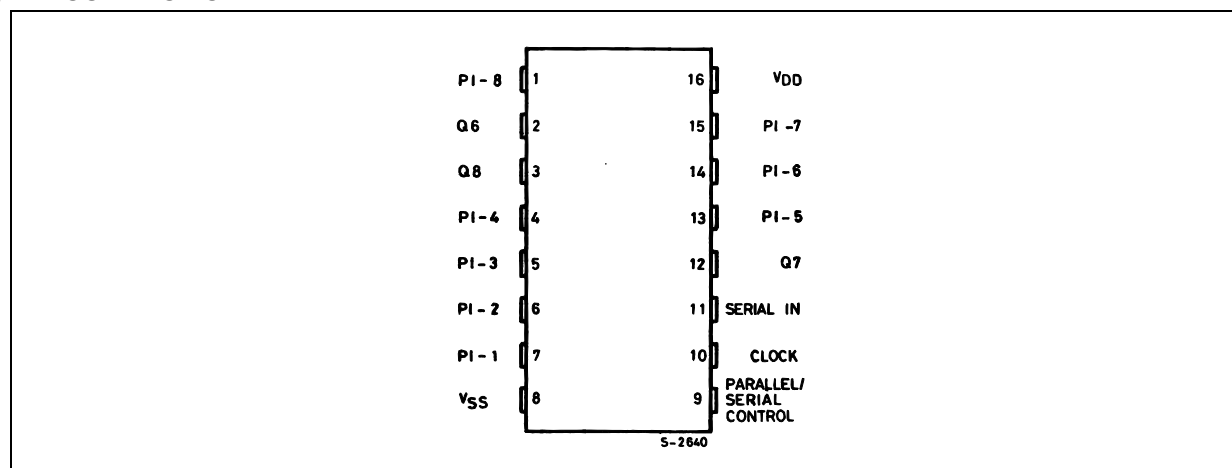
PACKAGE	TUBE	T & R
DIP	HCF4014BEY	
SOP	HCF4014BM1	HCF4014M013TR

DESCRIPTION

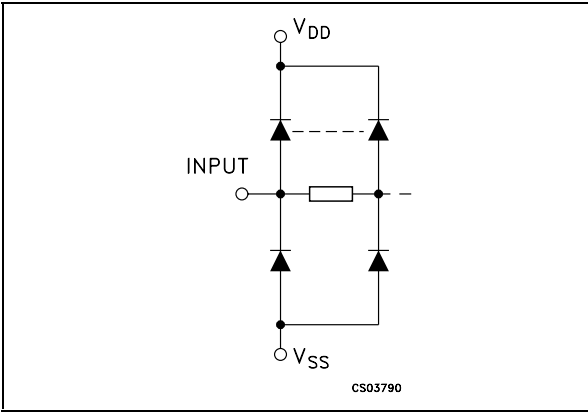
The HCF4014B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. This device is an 8-stage parallel or serial input/serial output register having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop in addition to an output from stage 8, "Q" outputs are also available

from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition. In this device, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

PIN CONNECTION



IINPUT EQUIVALENT CIRCUIT



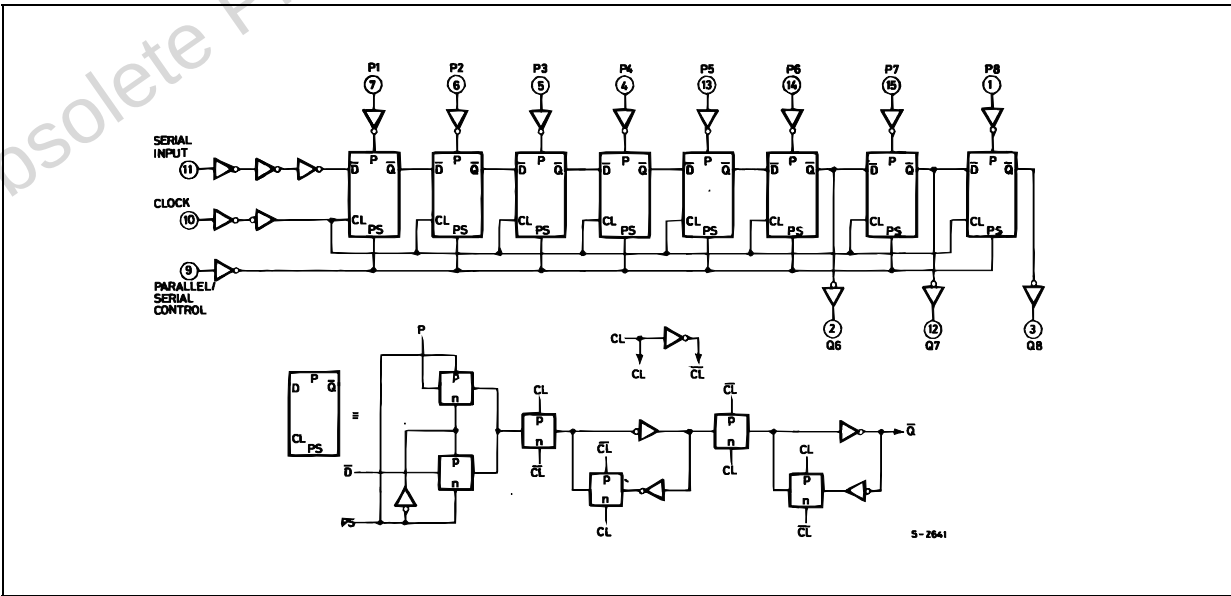
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
7, 6, 5, 4, 13, 14, 15, 1	PI1 to PI8	Parallel Input
11	SERIAL IN	Serial Input
9	PARALLEL/SERIAL CONTROL	Parallel/Serial Input Control
10	CLOCK	Clock Input
2, 3, 12	Q6, Q7, Q8	Buffered Outputs
8	VSS	Negative Supply Voltage
16	VDD	Positive Supply Voltage

TRUTH TABLE

CLOCK	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PI - 1	PI - n	Q ₁ (INTERNAL)	Q _n
	X	1	0	0	0	0
	X	1	1	0	1	0
	X	1	0	1	0	1
	X	1	1	1	1	1
	0	0	X	X	0	Q _n - 1
	1	0	X	X	1	Q _n - 1
	X	X	X	X	Q ₁	Q _n

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		3 to 20	V
V_I	Input Voltage		0 to V_{DD}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time (PI-1 ... PI-8)	$V_{DD} = 5V$	0 to 1000	μs

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

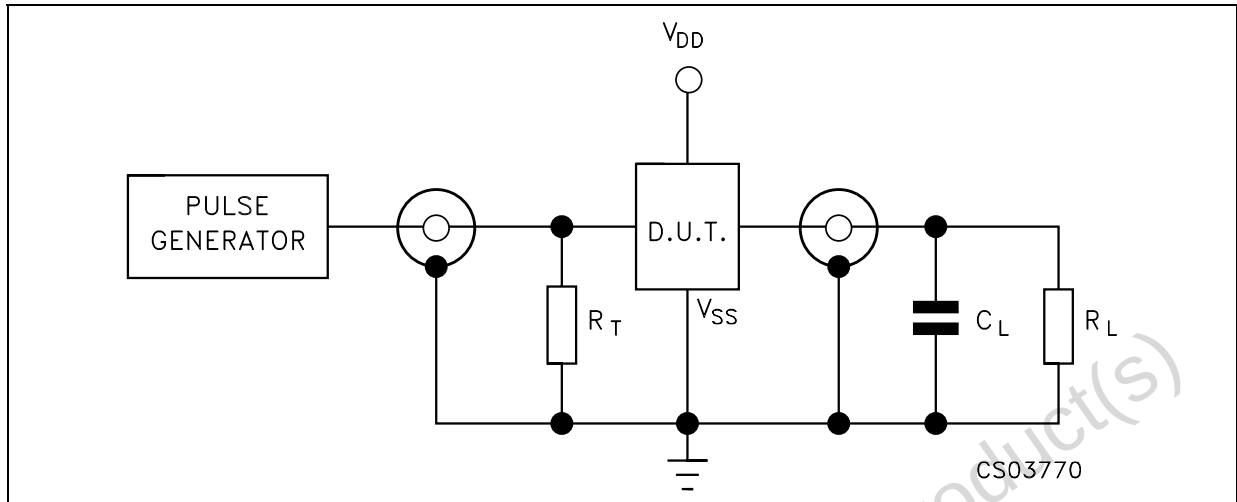
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

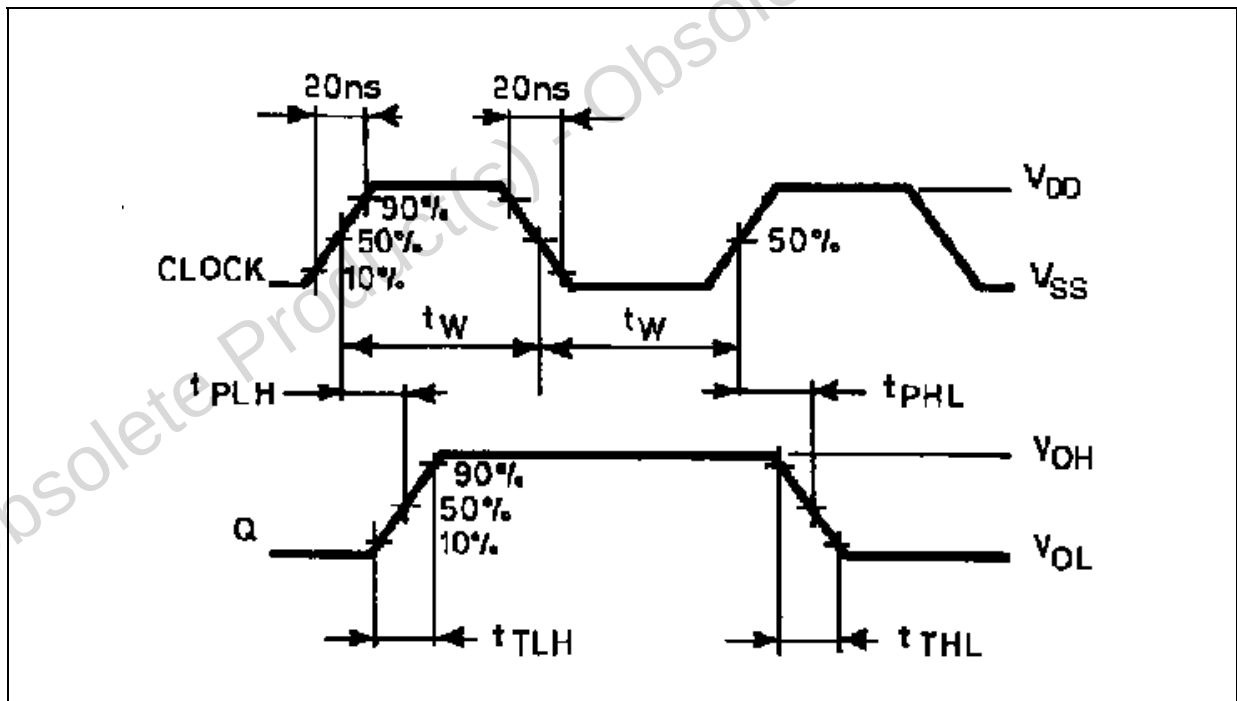
Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t _{PLH} t _{PHL}	Propagation Delay Time	5			160	320	ns
		10			80	160	
		15			60	120	
t _{THL} t _{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f _{CL} ⁽¹⁾	Maximum Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8.5	17		
t _W	Clock Pulse Width	5		180	90		ns
		10		80	40		
		15		50	25		
t _r , t _f	Clock Input Rise or Fall Time	5				15	μs
		10				15	
		15				15	
t _{setup}	Setup Time, serial Input (ref to CL)	5		120	60		ns
		10		80	40		
		15		60	30		
t _{setup}	Setup Time, Parallel Inputs (ref to CL)	5		80	40		ns
		10		50	25		
		15		40	20		
t _{setup}	Setup Time, Parallel/Serial Control (ref to CL)	5		180	90		ns
		10		80	40		
		15		60	30		
t _{hold}	Hold Time, serial in, parallel in, parallel /serial control	5		0			ns
		10		0			
		15		0			

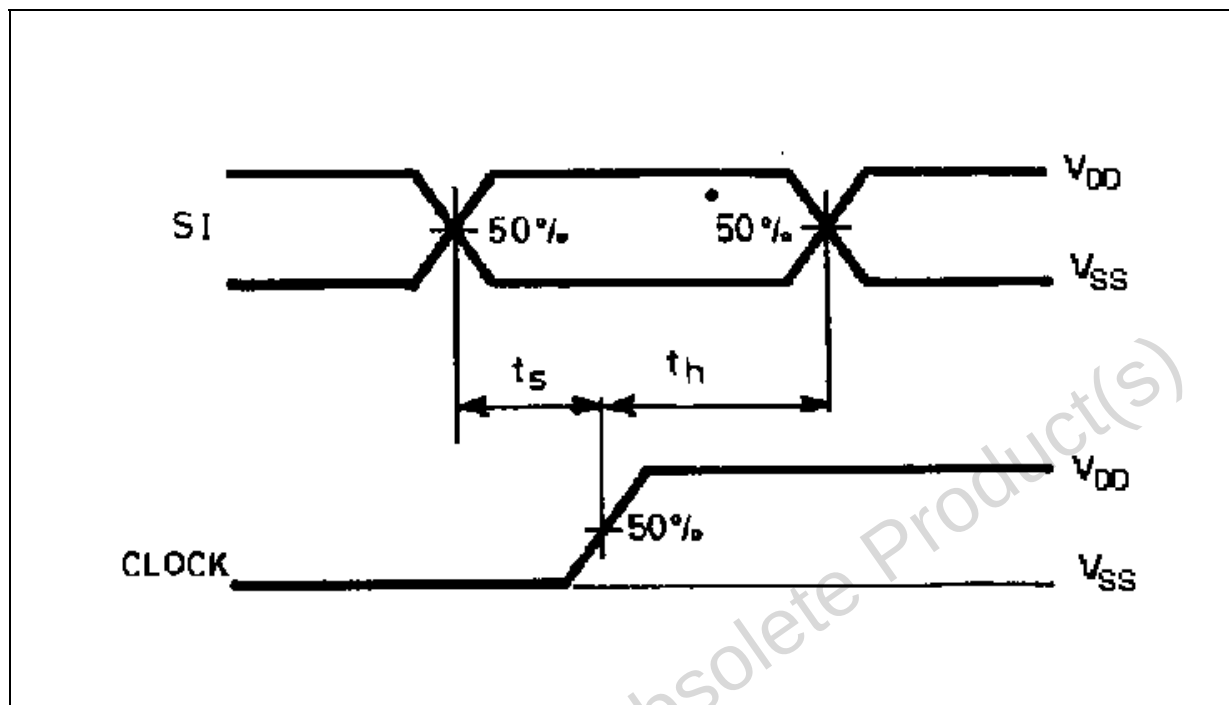
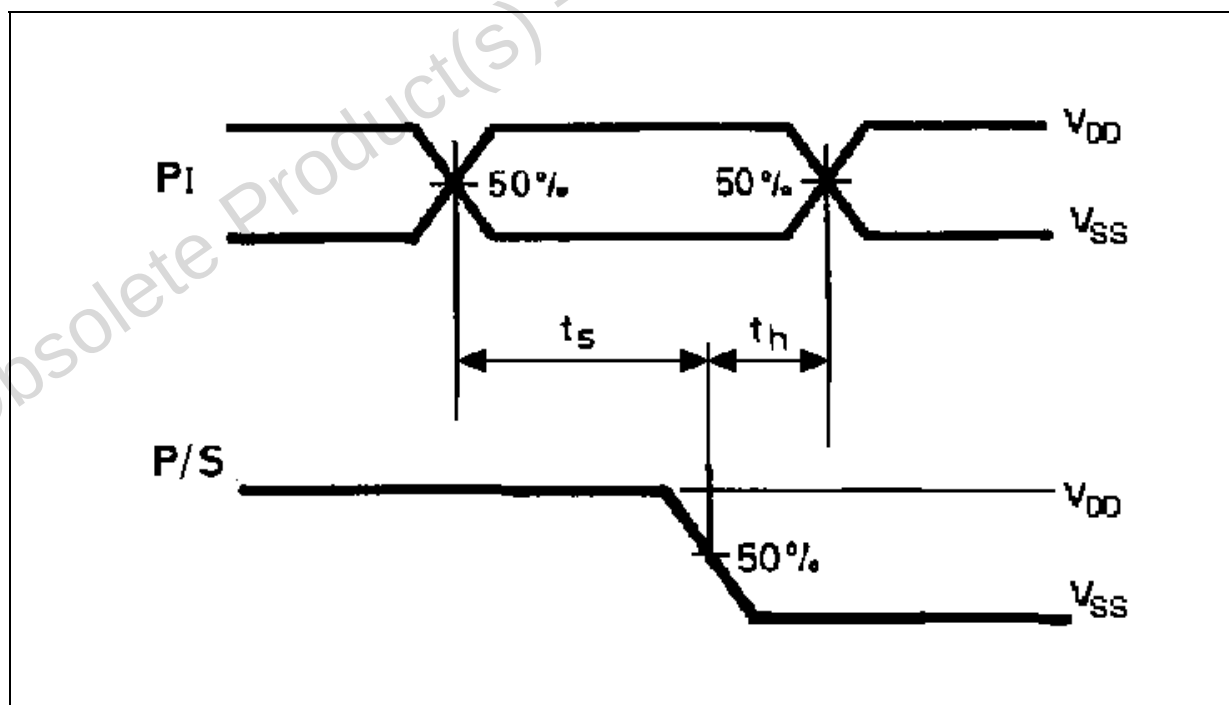
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/ $^{\circ}\text{C}$.(1) If more than one unit is cascaded t_{CL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage of the estimated capacitive load.

TEST CIRCUIT



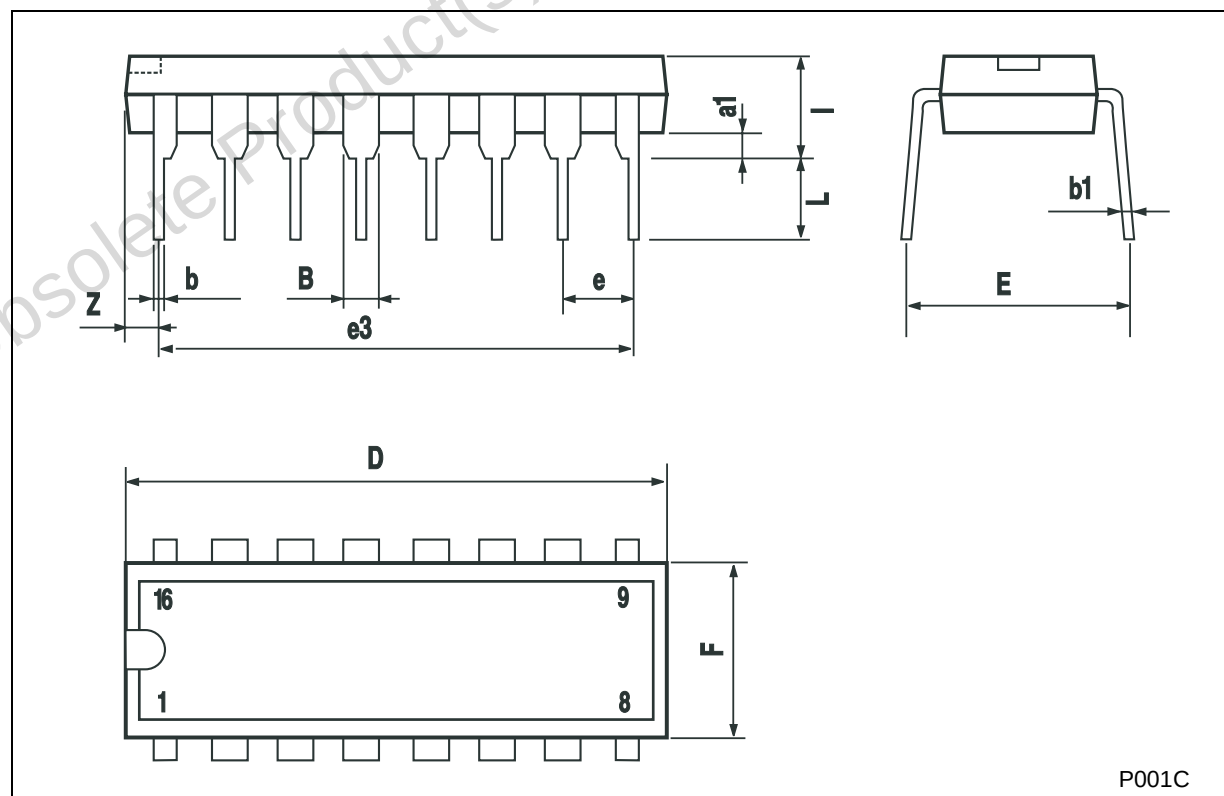
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{k}\Omega$
 $R_T = Z_{\text{OUT}}$ of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAY TIMES, CLOCK PULSE WIDTH ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 2 : SETUP AND HOLD TIMES (SI TO CLOCK) (f=1MHz; 50% duty cycle)**WAVEFORM 3 : SETUP AND HOLD TIME (PI TO P/S) (f=1MHz; 50% duty cycle)**

Plastic DIP-16 (0.25) MECHANICAL DATA

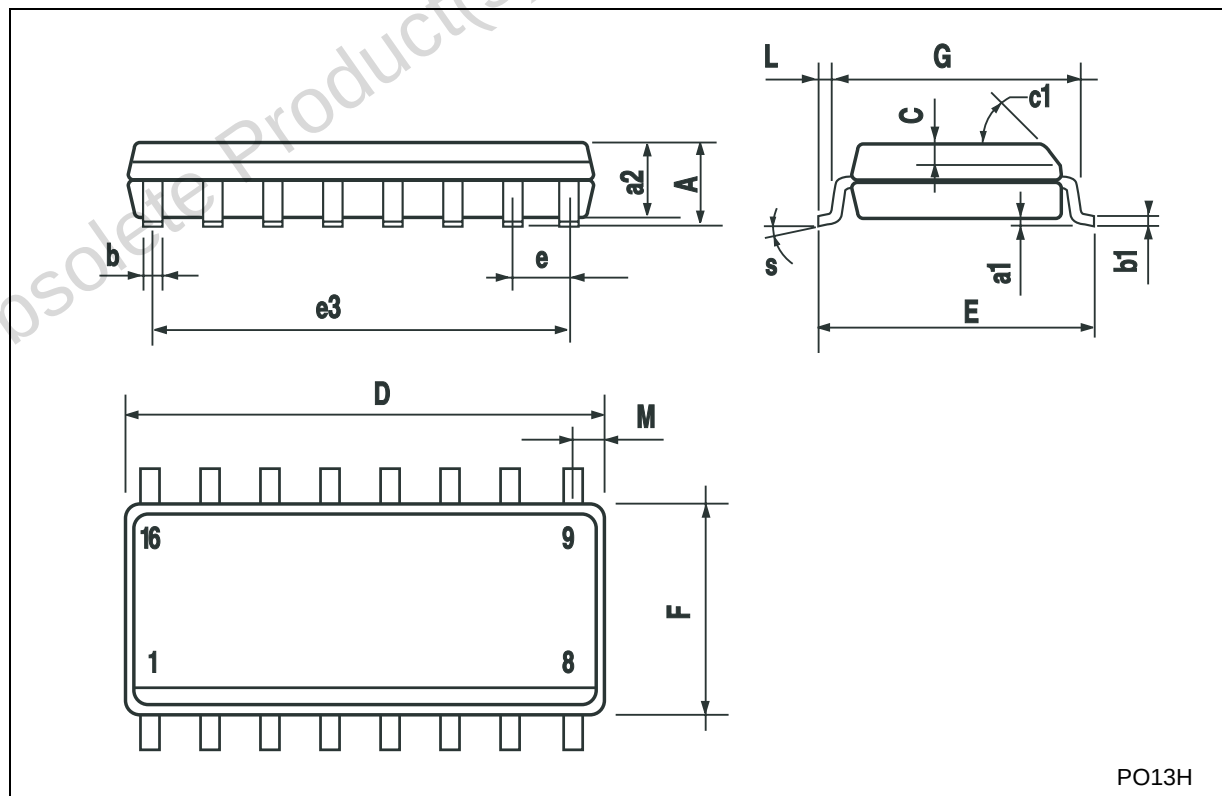
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>