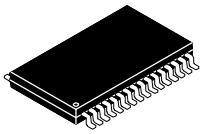
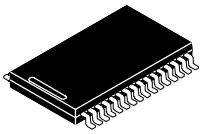




PurePath Digital™ AMPLIFIER
TAS5110A 50-W DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **50 W RMS Power Into 6 Ω at 10% THD**
- **40 W RMS Power Into 6 Ω at 0.1% THD**
- **THD+N < 0.09% Typical (1-kHz Input Signal)**
- **93-dB Dynamic Range (TDAA System)**
- **Power Efficiency > 90% Into 6-Ω and 8-Ω Load**
- **Low Profile, SMD 32-Pin PowerPAD™ Package**
- **Self-Protecting Design**
- **3.3-V Digital Interface**
- **EMI Compliant When Used With Recommended System Design**

APPLICATIONS

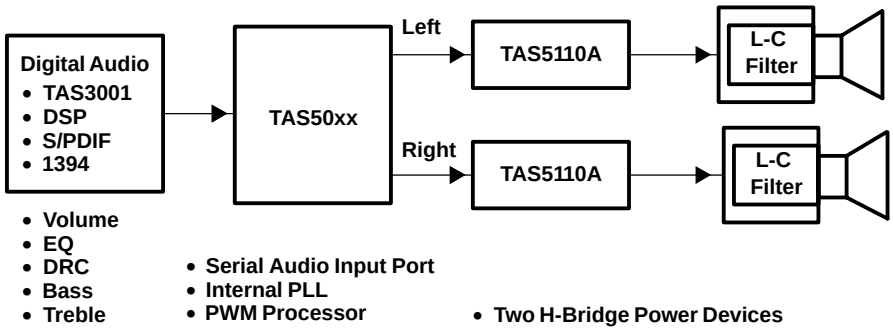
- **DVD Receiver**
- **Home Theater**
- **Mini/Micro Component Systems**
- **Internet Music Appliance**
- **Car Audio Amplifiers and Head Units**

DESCRIPTION

The TAS5110A is a high-performance true-digital audio amplifier (TDAA) power stage, designed to drive 50 W per channel. The TAS5110A incorporates TI's Equibit™ and PurePath Digital technology and is used in conjunction with a digital audio PWM processor (TAS50xx) to deliver high-power, true-digital audio amplification. The efficiency of this digital amplifier can be greater than 90%, reducing the size of both the power supplies and heat sinks needed. The TAS5110A accepts a mono PWM 3.3-V input and controls the switching of an internal CMOS H-bridge.

When used with the TAS50xx PWM processor, system performance of less than 0.09% THD is attainable. Overcurrent protection, overtemperature, and undervoltage protections are built into the TAS5110A, safeguarding the H-bridge and speakers against output shorts, overvoltage conditions, and other fault conditions that could damage the system.

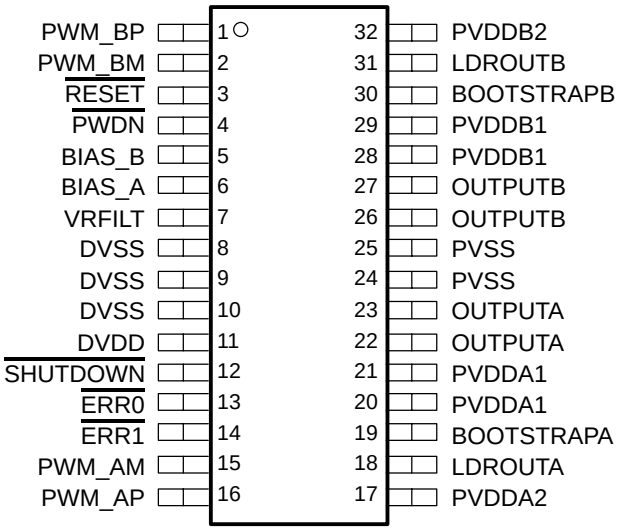
TYPICAL TDAA STEREO AUDIO SYSTEM



TERMINAL ASSIGNMENTS

The TAS5110A is offered in a thermally enhanced 32-pin TSSOP surface-mount package (DAD). The DAD package has the PowerPAD on top.

DAD PACKAGE
(TOP VIEW)



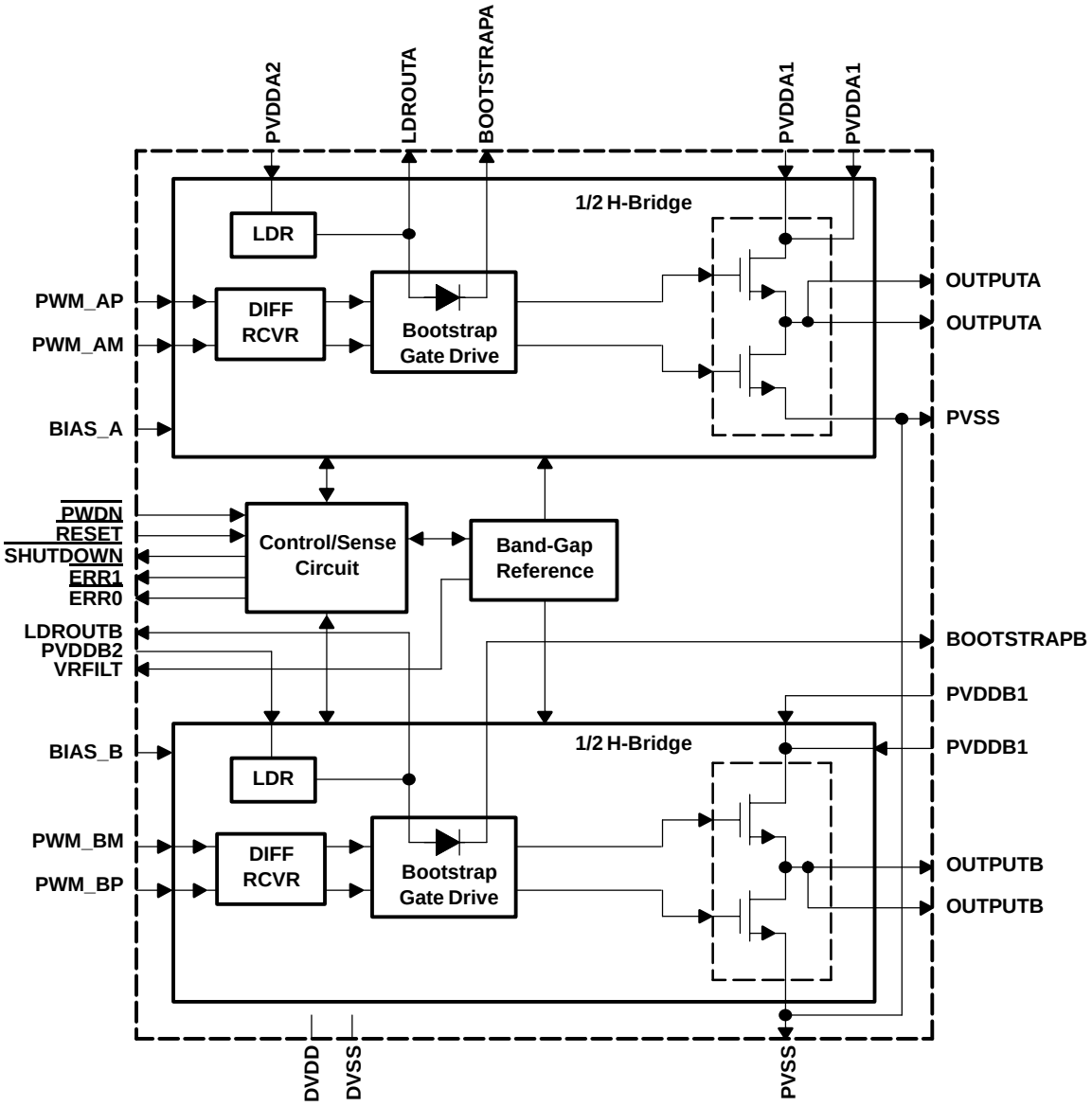
ORDERING INFORMATION

T_C	PACKAGE	TAPE AND REEL
0°C to 70°C	TAS5110ADAD	TAS5110ADADR

REFERENCES

1. *TAS5000 Digital Audio PWM Processor* data manual (SLAS270)
2. *True Digital Audio Amplifier TAS5001 Digital Audio PWM Processor* data sheet (SLES009)
3. *True Digital Audio Amplifier TAS5010 Digital Audio PWM Processor* data sheet (SLAS328)
4. *True Digital Audio Amplifier TAS5012 Digital Audio PWM Processor* data sheet (SLES006)
5. *Digital Audio Measurements* application report (SLAA114)
6. *PowerPAD Thermally Enhanced Package* technical brief (SLMA002)

FUNCTIONAL BLOCK DIAGRAM



SUGGESTED SYSTEM BLOCK DIAGRAMS

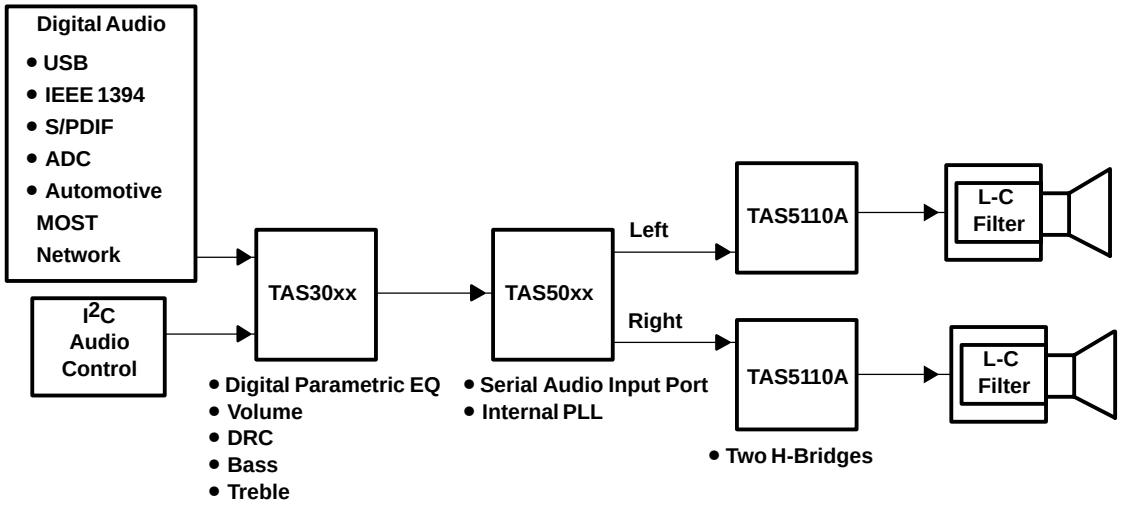


Figure 1. System #1: Stereo Configuration With a TAS3001 Digital Audio Processor

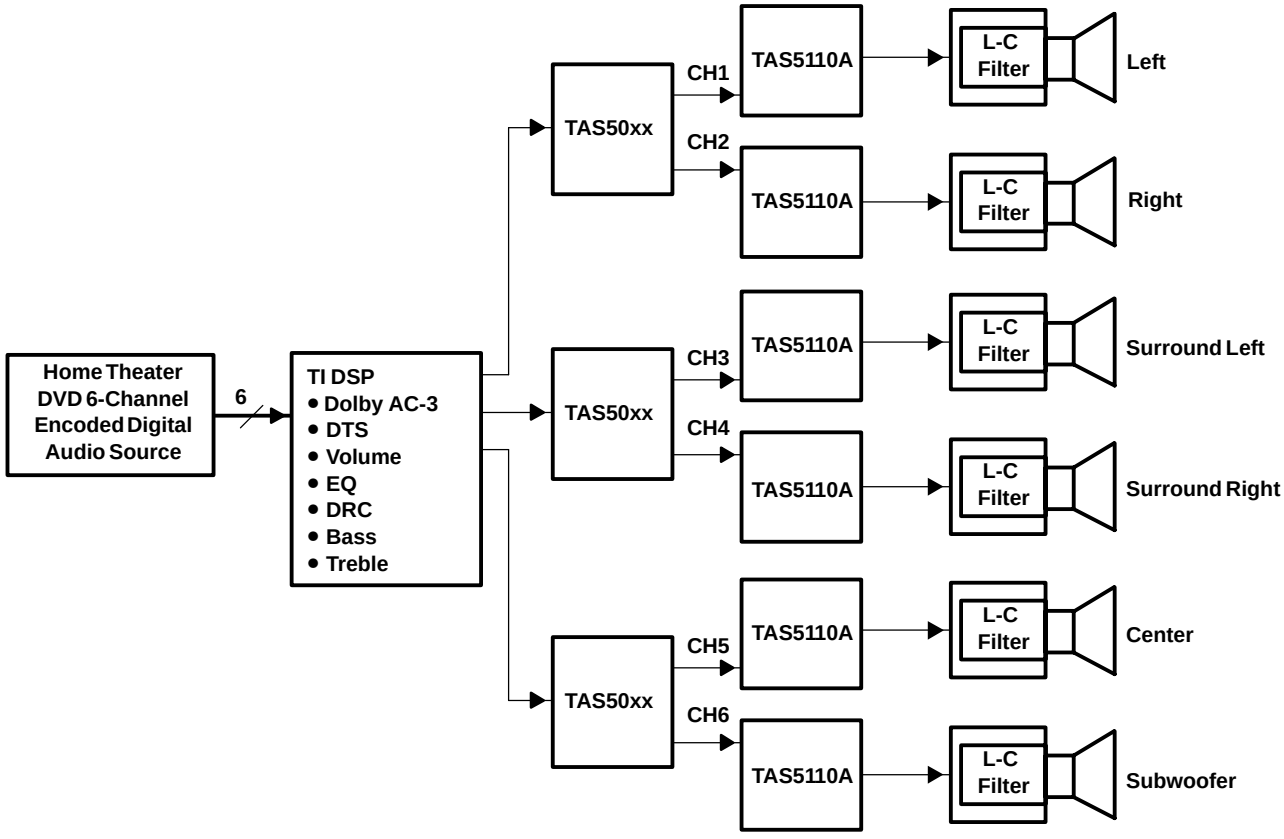


Figure 2. System #2: 6-Channel Audio Playback

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	DAD NO.		
BIAS_A	6	I	Connect external resistor to DVSS.
BIAS_B	5	I	Connect external resistor to DVSS.
BOOTSTRAPA	19	O	Bootstrap capacitor pin for H-bridge A
BOOTSTRAPB	30	O	Bootstrap capacitor pin for H-bridge B
DVDD	11	—	3.3-V digital voltage supply for logic
DVSS	8, 9, 10	—	Digital ground for logic is internally connected to PVSS. All three pins must be tied together but not connected externally to PVSS. See Figure 5.
$\overline{\text{ERR1}}$	14	O	Error/warning report indicator. This output is open drain with internal pullup resistor.
$\overline{\text{ERR0}}$	13	O	Error/warning report indicator. This output is open drain with internal pullup resistor.
LDROUTA	18	O	Low-voltage drop-out regulator output A (not to be used to supply current to external circuitry)
LDROUTB	31	O	Low-voltage drop-out regulator output B (not to be used to supply current to external circuitry)
OUTPUTA	22, 23	O	H-bridge output A
OUTPUTB	26, 27	O	H-bridge output B
PVDDA1	20, 21	—	High-voltage power supply, H-bridge A
PVDDA2	17	—	High-voltage power supply for low-dropout voltage regulator A-side
PVDDB1	28, 29	—	High-voltage power supply, H-bridge B
PVDDB2	32	—	High-voltage power supply for low-dropout voltage regulator B-side
PVSS	24, 25	—	High-voltage power supply ground
$\overline{\text{PWDN}}$	4	I	Power down = 0, normal mode = 1
PWM_AM	15	I	PWM input A(–)
PWM_AP	16	I	PWM input A(+)
PWM_BP	1	I	PWM input B(+)
PWM_BM	2	I	PWM input B(–)
$\overline{\text{RESET}}$	3	I	Reset and mute mode = 0, normal mode = 1; when in reset mode, H-bridge MOSFETs are in low-low output state. Asserting the $\overline{\text{RESET}}$ signal low causes all fault conditions to be cleared.
$\overline{\text{SHUTDOWN}}$	12	O	Device is in shutdown due to fault condition, normal mode = 1, shutdown = 0; when device is in shutdown mode the H-bridge MOSFETs are in low-low output state. The latched output can be cleared by asserting the $\overline{\text{RESET}}$ signal. This output is open drain with internal pullup resistor.
VRFILT	7	O	A filter capacitor must be added between the VRFILT and DVSS pins.

NOTE: The four PWM inputs: PWM_AP, PWM_AM, PWM_BP, and PWM_BM must always be connected to the TAS50xx output pins and never left floating. Floating PWM input pins cause an illegal PWM input state signal to be asserted.

Dual pins: OUTPUTA, OUTPUTB, PVDDA1, and PVDDB1 must have both pins connected externally to the same point on the circuit board, respectively. Both PVSS pins must also be connected together externally. These multiple pins are for the high-current DMOS output devices. Failure to connect all the multiple pins to the same respective node results in excessive current flow in the internal bond wires and can cause the device to fail. All electrical characteristics are specified and measured with all of the multiple pins of each type connected to a single node.

FUNCTIONAL DESCRIPTION

PWM H-Bridge State Control

The digital interface control signals consists of PWM_AP, PWM_AM, PWM_BP, and PWM_BM. These signals are a complementary differential signal format for the A-side half-bridge and the B-side half-bridge.

Bootstrapped Gate Drive

The TAS5110A includes two dedicated bootstrapped power supplies. A bootstrap capacitor is connected between the individual bootstrap pin and the associated output. For example, a capacitor is connected between the BOOTSTRAPA pin and the OUTPUTA pin and another capacitor is connected between the BOOTSTRAPB pin and the OUTPUTB pin. The bootstrap power supply minimizes the number of high voltage power supply levels externally supplied to the system, while providing a low-noise supply level for driving the high-side N-channel DMOS transistors.

Low-Dropout Voltage Regulator

Two on-chip low-dropout voltage regulators (LDO) are provided to minimize the number of external power supplies needed for the system. These voltage regulators are for internal circuits only and cannot be used for external circuitry. Each LDO is dedicated to a half-bridge and its gate driver. An LDO output capacitor is connected between the individual LDO output pin and the associated output return. For example, a capacitor is connected between the LDROUTA pin and the PVSS pin and another capacitor is connected between the LDROUTB pin and the PVSS pin.

High-Current H-bridge Output Stage

The positive outputs of the H-bridge are the two OUTPUTA pins. The negative outputs of the H-bridge are the two OUTPUTB pins. The logic for the input command to H-bridge outputs is described in the *H-bridge output mapping* section immediately following. When the TAS5110A is in the normal mode, as seen in the H-bridge output mapping tables, the outputs are decoded from the inputs. However, the TAS5110A is immediately shut down if any of the following error conditions occur: overcurrent, overtemperature, low regulator output voltage, or an illegal PWM input state is applied. For these conditions, the outputs are set to the appropriate disabled state as specified in the H-bridge output mapping section, and the $\overline{\text{SHUTDOWN}}$ pin is set low.

H-Bridge Output Mapping

The A-side half-bridge output is designed to the following truth table:

INPUTS				OUTPUTS		DESCRIPTION
$\overline{\text{RESET}}$	$\overline{\text{PWDN}}$	PWM_AP	PWM_AM	$\overline{\text{SHUTDOWN}}$	OUTPUTA	
X	X	X	X	0	0 or Hi-Z(1)	Shutdown
X	0	X	X	1	Hi-Z	Power down
0	1	X	X	1	0	Reset
1	1	0	0	0	0	Shutdown
1	1	0	1	1	0	Normal
1	1	1	0	1	1	Normal
1	1	1	1	0	0	Shutdown

(1) Output is 0 for low voltage, overtemperature, and illegal input. Hi-Z is for overcurrent.

The B-side half-bridge output is designed to the following truth table:

INPUTS				OUTPUTS		DESCRIPTION
$\overline{\text{RESET}}$	$\overline{\text{PWDN}}$	PWM_BP	PWM_BM	$\overline{\text{SHUTDOWN}}$	OUTPUTB	
X	X	X	X	0	0 or Hi-Z(1)	Shutdown
X	0	X	X	1	Hi-Z	Power down
0	1	X	X	1	0	Reset
1	1	0	0	0	0	Shutdown
1	1	0	1	1	0	Normal
1	1	1	0	1	1	Normal
1	1	1	1	0	0	Shutdown

(1) Output is 0 for low voltage, overtemperature, or illegal input. Hi-Z is for overcurrent.

Control/Sense Circuitry

The control/sense circuitry consists of the following 3.3-V logic level pins: $\overline{\text{PWDN}}$, $\overline{\text{RESET}}$, $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$. The active-low $\overline{\text{PWDN}}$ input pin powers down all internal circuitry and forces the H-bridge outputs to the Hi-Z state. When the $\overline{\text{PWDN}}$ pin is low, the open drain $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$ pins are also disabled so that their outputs can be pulled high. The active-low $\overline{\text{RESET}}$ input pin forces the H-bridge outputs to the low-low state and resets the overcurrent shutdown latch. The $\overline{\text{PWDN}}$ pin overrides the $\overline{\text{RESET}}$ pin. The $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, and $\overline{\text{SHUTDOWN}}$ outputs indicate the following conditions in the TAS5110A as shown in the following table. These three outputs are open-drain connections with internal pullup resistors so that wire-ORed connections can be made by the user with other external control devices. The short-circuit protect error condition latches the TAS5110A in this shutdown state and forces the H-bridge outputs to the Hi-Z state until the device is reset by means of the $\overline{\text{RESET}}$ pin. The illegal PWM input state, overtemperature, and low regulator voltage error conditions does not latch the device in the shutdown condition. Instead the H-bridge outputs are forced to the low-low state and the TAS5110A returns to normal operation as soon as the error condition ends. Loss of clocking PWM signal is also considered an illegal PWM input state.

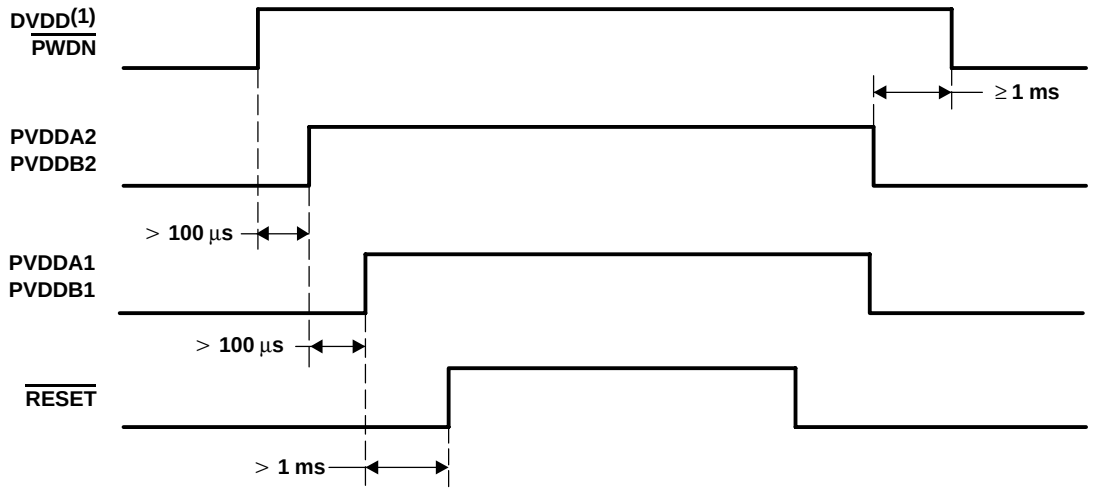
$\overline{\text{SHUTDOWN}}$	$\overline{\text{ERR1}}$	$\overline{\text{ERR0}}$	FUNCTION	OUTPUTA	OUTPUTB
0	0	0	Illegal PWM input state	Low	Low
0	0	1	Short circuit protect (latch)	Hi-Z	Hi-Z
0	1	0	Over temperature protect	Low	Low
0	1	1	Low regulator voltage protect	Low	Low
1	0	0	Reserved	—	—
1	0	1	Reserved	—	—
1	1	0	High temperature – warning	Normal	Normal
1	1	1	Normal operation	Normal	Normal

DEVICE OPERATION

Power Sequences

System Power-up/Power-down Sequencing

The recommended power-up/power-down sequence is shown in Figure 3. For proper operation the $\overline{\text{RESET}}$ signal should be kept low when both DVDD and output power (PVDDA1, PVDDA2, PVDDB1, and PVDDB2) are being applied. The $\overline{\text{RESET}}$ signal should remain low for at least 1 ms after output power is applied.



(1) For most applications, it is recommended that the $\overline{\text{PWDN}}$ pin be connected directly to the DVDD pin.

Figure 3. Power-Up/Power-Down Sequence

$\overline{\text{RESET}}$ Function

The device is put into a reset condition when the (active low) $\overline{\text{RESET}}$ signal is asserted. While in the reset state, the input H-bridge control signals consisting of PWM_AP, PWM_AM, PWM_BP, and PWM_BM are ignored, and the H-bridge MOSFETs are placed in a state where OUTPUTA and OUTPUTB are both low. Asserting the $\overline{\text{RESET}}$ signal low also causes the short circuit protection latch to be reset. The $\overline{\text{RESET}}$ signal is normally connected to the VALID signal from the TAS50xx.

Reinitialization Sequence

Proper initial conditions for this device include asserting the $\overline{\text{RESET}}$ signal until the reset operation has completed (1 ms). Additionally, when using this device with the TAS50xx controller, this function can be accomplished by asserting the reset pin on the TAS50xx during the reset sequence (see Figure 3).

Audio Application Considerations

Optimal Power Transfer For H-Bridge

The TAS5110A is a power H-bridge that is designed to deliver a maximum of 50 W RMS into a 6-Ω load. In order to achieve 50 W into 6 Ω, the system designer must provide an adequate thermal design. See the *Thermal Methodology for the 32-Pin DAD Package 50 W, 6-Ω Test* section for a discussion of possible thermal solutions. Careful attention must be given to the value of the high-voltage power supply level for a given load resistance. See recommended operating conditions. See the *Maximum Available Power at Common Load Impedances for DAD Packages* section.

reconstruction output filter

An output reconstruction filter is required between the H-bridge outputs and the loudspeaker load. This second-order low-pass filter passes the audio information to the loudspeaker, while filtering out the high-frequency out-of-band information contained in the H-bridge output PWM pulses. The values of the L and C components selected are dependent on the loudspeaker load impedance.

Fault Indicator Usage

The TAS5110A is a self-protecting device that provides device fault reporting, including overtemperature protect, undervoltage lockout (low regulator voltage), and short-circuit protection. The short circuit protection protects against short circuits that may occur at the loudspeaker load when configured. The TAS5110A is not recommended for driving loads less than 6 Ω, because the internal current limit protection might be activated.

An undervoltage lockout signal occurs when an insufficient voltage level is present on the LDROUTA or LDROUTB pins. During this condition, gate drive levels are not sufficient for driving the power MOSFETs. Normal operation is resumed when the minimum proper LDROUTA or LDROUTB level is obtained and the low regulator voltage protect signal is de-asserted. See the *control/sense circuitry* section for error and warning conditions.

A high-temperature warning signal is asserted on pin $\overline{\text{ERR0}}$ when the device temperature exceeds 125°C typical.

If the internal device temperature exceeds 150°C typical, the overtemperature protect signal is asserted and the TAS5110A is shut down. The device re-enables once the temperature drops to 125°C typical. See the *control/sense circuitry* section for error and warning conditions.

Detection of an illegal PWM input state or the loss of a clocking PWM input signal causes an illegal PWM input state signal to be asserted on the $\overline{\text{ERR1}}$and $\overline{\text{ERR0}}$ pins and sets the $\overline{\text{SHUTDOWN}}$ pin to the low state.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
DC supply voltage range	DVDD to DVSS	–0.3 V to 4.2 V
	PWM_AP, PWM_AM, PWM_BP, PWM_BM	–0.3 V to DVDD + 0.3 V
	$\overline{\text{RESET}}$, $\overline{\text{PWDN}}$	–0.3 V to DVDD + 0.3 V
	PVDDA1 to PVSS, PVDDB1 to PVSS	–0.3 V to 28 V
	PVDDA2 to PVSS, PVDDB2 to PVSS	0.3 V to 27 V
Output DMOS drain-to-source breakdown voltage		28 V
Operating junction temperature range, T_J		–40°C to 150°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(maximum output power = 50 W (RMS), T_J = 25°C)

Thermal Data(1)

			MIN	NOM	MAX	UNIT
$T_{J(SD)}$	Shutdown junction temperature			150		°C
$T_{J(W)}$	Warning junction temperature			125		°C
T_C	Operating temperature	Commercial	0	25	70	°C
$R_{\theta JC}$(2)	Thermal resistance junction-to-case	2 oz. trace and copper pad without solder		1.6		°C/W
$R_{\theta JA}$(2)	Thermal resistance junction-to-ambient			44.3		°C/W

(1) One of the most influential components on the thermal performance of a package is board design. In order to take full advantage of the heat dissipating abilities of the PowerPAD packages, a board must be used that acts similar to a heat sink and allows for the use of the exposed (and solderable), deep downset pad. See Appendix A of the *PowerPAD Thermally Enhanced Package* technical brief, TI literature number SLMA002.
(2) For the DAD package.

R_L = 6 Ω to 8 Ω

			MIN	NOM	MAX	UNIT
Supply voltage	Digital	DVDD to DVSS	3	3.3	3.6	V
	Regulator	PVDDA2 to PVSS	16.5	22	26.5	V
		PVDDB2 to PVSS	16.5	22	26.5	
		PVDDA2 to PVSS(1)	10.5		16.5	
		PVDDB2 to PVSS(1)	10.5		16.5	

(1) Connect LDROUTA to PVDDA2 and connect LDROUTB to PVDDB2. Under this condition, the H-bridge forward on-state resistance is increased. This increases internal power dissipation. Maximum output power may need to be reduced to meet thermal conditions.

Maximum Available Power at Common Load Impedances for the DAD Package Unclipped (0 dB) Level(1)

LOAD IMPEDANCE (Ω)	PVDAA1/PVDDB1 (VDC)	APPROXIMATE MAXIMUM OUTPUT POWER (W)	THD+N AT MAXIMUM POWER AND 1-kHz INPUT(2)
6	27	50	< 10%
6	27	43	< 0.09%
8	27	34	< 0.09%

(1) Dependent on board design and component selection
(2) Test conditions are described in the *Thermal Methodology for the 32-Pin DAD Package 50 W, 6-Ω Test*.

STATIC DIGITAL SPECIFICATIONS

$\overline{\text{RESET}}$, $\overline{\text{PWDN}}$, PWM_AP, PWM_AM, PWM_BP, PWM_BM, T_J = 25°C, DVDD = 3.3 V

PARAMETERS		MIN	MAX	UNIT
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
	Input leakage current	–10	10	μA

$\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$, $\overline{\text{SHUTDOWN}}$, (Open Drain With Internal Pullup Resistor) T_J = 25°C, DVDD = 3.3 V)

PARAMETERS		MIN	MAX	UNIT
	Internal pullup resistors from $\overline{\text{SHUTDOWN}}$, $\overline{\text{ERR0}}$, $\overline{\text{ERR1}}$ to DVDD	15		kΩ
V_{OL}	Low-level output voltage (I_O = 4 mA)		0.4	V

ELECTRICAL CHARACTERISTICS

Supply, T_J = 25°C (F_S = 384 kHz, OUTPUTA and OUTPUTB not connected, DVDD = 3.3 V, PVDDA1 = 25 V, PVDDB1 = 25 V, PVDDA2 = 22 V, PVDDB2 = 22 V, 50% input duty cycle)

PARAMETER			TYP	MAX	UNIT
Supply current	DVDD	Operating	2		mA
		$\overline{PWDN}$ = 0		500	µA
	PVDDA1, PVDDB1	Operating(1)	6.3		mA
		$\overline{PWDN}$ = 0		25	µA
	PVDDA2, PVDDB2	Operating	6.5		mA
		$\overline{PWDN}$ = 0		250	µA

(1) 13-kΩ resistor from BIAS_A (pin 11) to DVSS and 13-kΩ resistor from BIAS_B (pin 12) to DVSS.

H-Bridge Transistors, PVDDA2 = PVDDB2 = 22 V, DVDD = 3.3 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-to-source breakdown voltage	I_D = 1 mA, $\overline{PWDN}$ = 0, Hi-Z state	28			V
Forward on-state resistance, low-side drivers OUTPUTA and OUTPUTB to PVSS	I_{SINK} = 2.5 A, See Notes 1, 2, and 3, PWM_AP = PWM_BP = 0, PWM_AM = PWM_BM = 1		0.2	0.24	Ω
Forward on-state resistance, high-side drivers PVDDA1 to OUTPUTA, PVDDB1 to OUTPUTB	I_{SOURCE} = 2.5 A, See Notes 1, 2, and 4, PWM_AP = PWM_BP = 1, PWM_AM = PWM_BM = 0		0.2	0.24	Ω
On-state resistance matching, low-side drivers			98%		
On-state resistance matching, high-side drivers			98%		

(1) Test time should be < 1 ms to minimize temperature change
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(3) Connect PVDDA2 and PVDDB2 to a 22-V power supply with respect to PVSS. LDROUTA, LDROUTB, BOOTSTRAPA, and BOOTSTRAPB pins open.
(4) Connect PVDDA2 to 22-V power supply with respect to PVSS. LDROUTA, LDROUTB, BOOTSTRAPA, and BOOTSTRAPB capacitors are connected, respectively. Clock PWM inputs to allow bootstrap capacitors to charge. 93–99% modulation must be used on PWM_AP, PWM_AM, PWM_BP, and PWM_BM inputs to prevent the activity detector from shutting down the device during this measurement. Note that F_S = 384 kHz.

Electrical Characteristics, Voltage Regulator, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (LDROUTA, LDROUTB)	I_O = 5 mA, See Note 1, PVDDA2 = PVDDB2 = 18 V to 27 V, DVDD = 3.3 V	14.5	15.3	16	V

(1) These voltage regulators are for internal gate drive circuits only and are not to be used under any circumstances to supply current to external circuity.

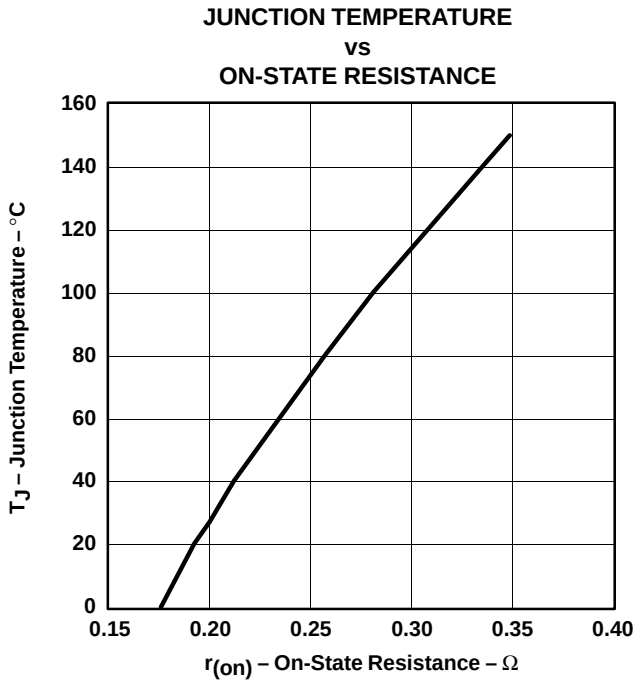


Figure 4. Temperature vs On-State Resistance

APPLICATION INFORMATION

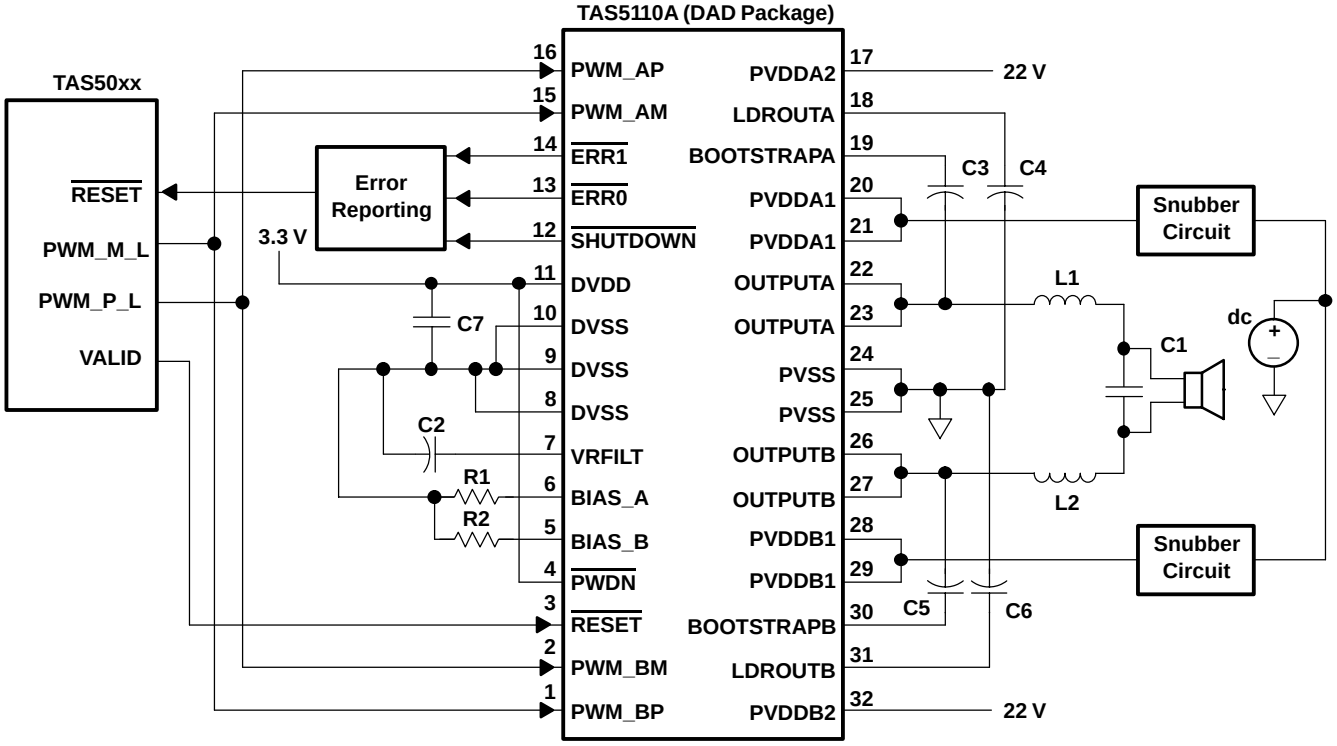


Figure 5. Typical TAS5110A Application (One Channel Shown)

THERMAL INFORMATION

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have two shortcomings: they do not address the low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal count that is high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced HTSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PCB. Because of the very small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipater, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved. See the dissipation derating table.

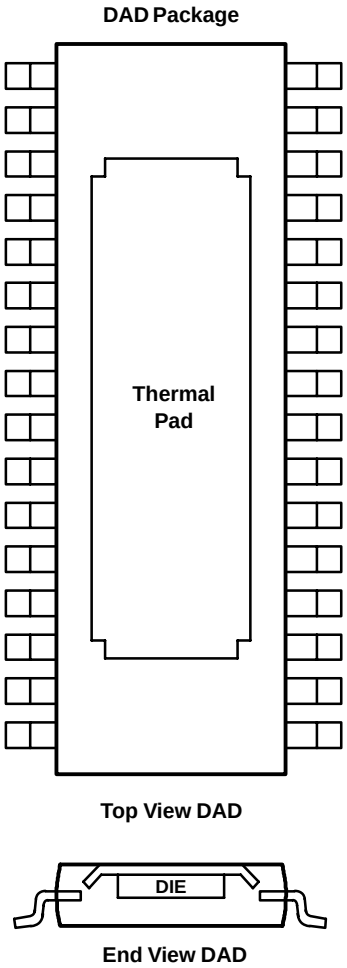


Figure 6. View of Thermally Enhanced DAD Package

Thermal Methodology for the 32-Pin DAD Package 50 W, 6-Ω Test

The thermal test for the DAD part (e.g., thermal pad oriented away from the board) was conducted as shown in Figure 7 and Figure 8. The cooling approach was to attach a heat sink to the thermal pad and conduct the heat to ambient air.

Since the approach was to use a chassis below the board, it was inverted and a spacer bar used to connect the pads thermally to the heat sink. The bar was made high enough that the components on the board were clear of the chassis.

The pad-to-spacer thermal resistance was about 3.2°C/W with the thermal compound indicated.

The chassis provided the only heat sink to air and was chosen as representative of a possible cooling approach. A closed plastic top and insulating front and back panels ensured that only the bottom and sides of the U shaped chassis contributed to cooling. The chassis was spaced 0.25 inch from the table to simulate a normal chassis configuration. The thermal pad does not need to be isolated from ground. (Any heat sink with a thermal resistance to air of 3.9°C/W or lower also works.) In this test, the exposed chassis reached long-term equilibrium temperatures above 50°C, so the approach would have to be modified for touch temperature consideration. The chassis temperature after 10 minutes of 50 W into 6 Ω was below 50°C.

The test ran for three hours with 2 × 50 W RMS at 1 kHz into a 6-Ω resistive load at an ambient lab temperature of 23°C. No audio or thermal problems were encountered during that time.

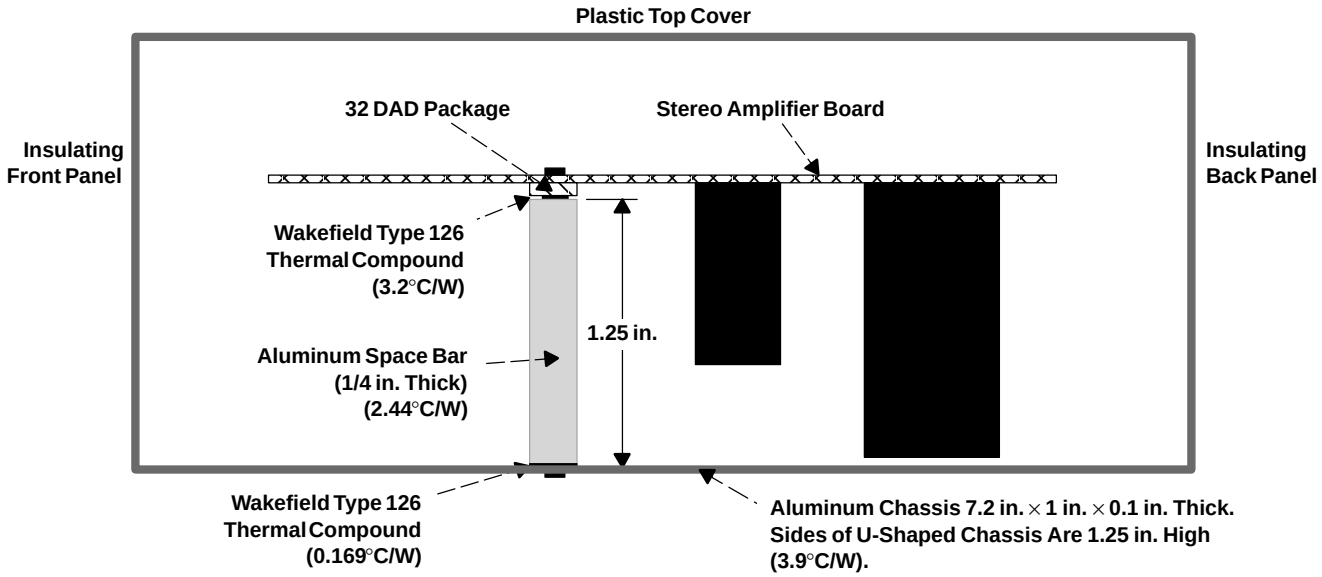


Figure 7. 32-Pin DAD Package Cross-Sectional View (Side)

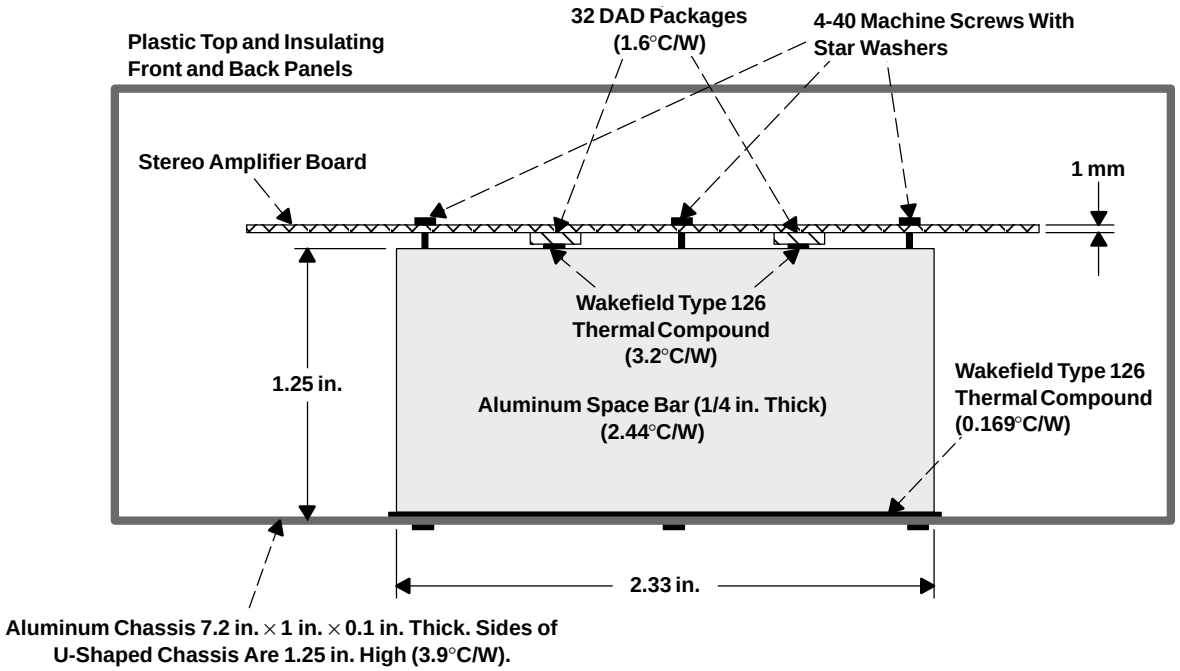


Figure 8. 32-Pin DAD Package Cross-Sectional View (Front)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TAS5110ADAD	NRND	HTSSOP	DAD	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TAS5110ADADG4	NRND	HTSSOP	DAD	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TAS5110ADADR	NRND	HTSSOP	DAD	32		TBD	Call TI	Call TI	
TAS5110ADADRG4	NRND	HTSSOP	DAD	32		TBD	Call TI	Call TI	

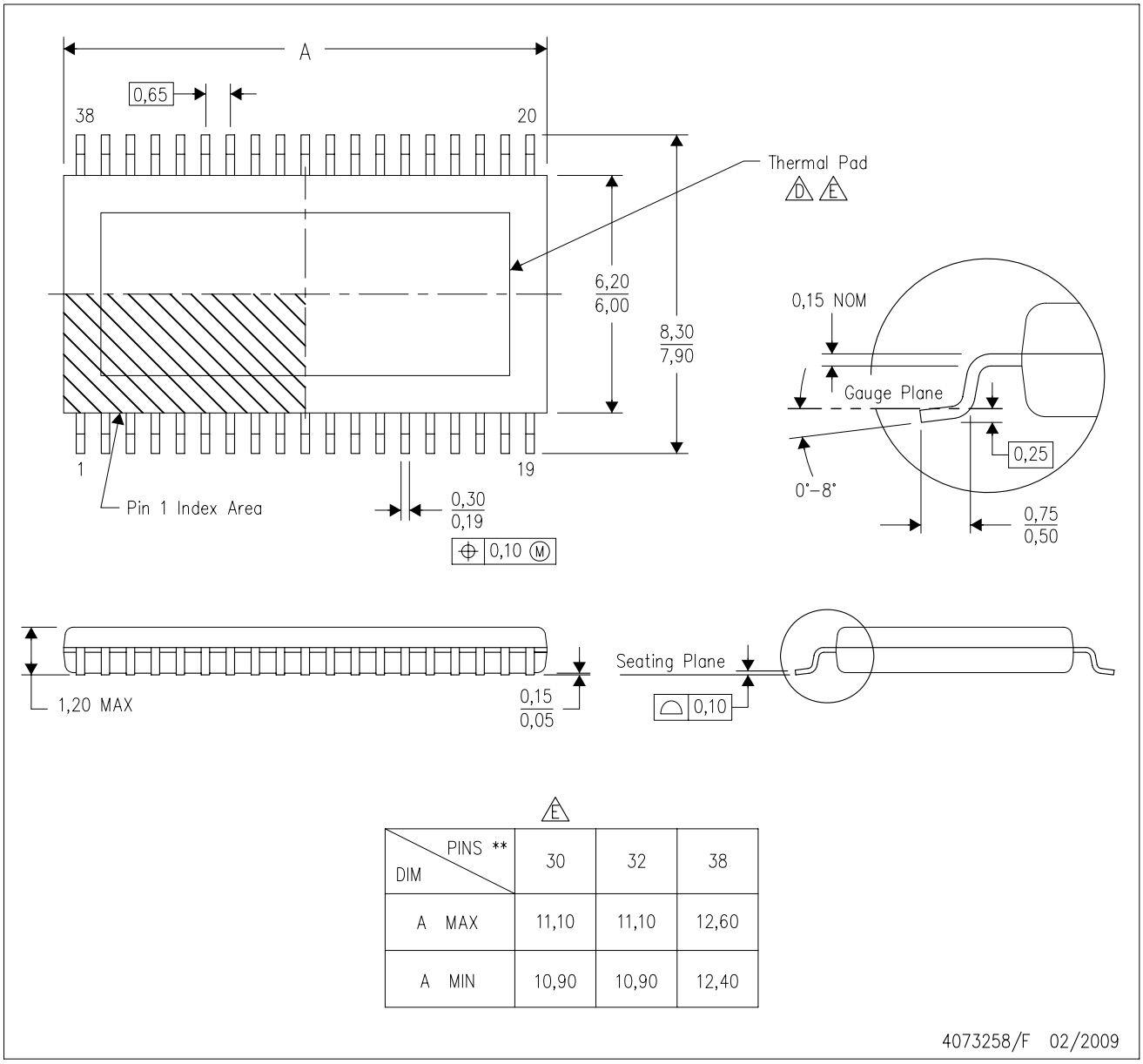
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DAD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE (DIE DOWN)

38 PIN SHOWN



E

DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4073258/F 02/2009

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153, except 30 pin body length and JEDEC variations for top side thermal pad.

PowerPAD is a trademark of Texas Instruments.

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