

FEATURES

- **Ultralow Voltage Noise**
 - **30nV_{p-p} Noise: 0.1Hz to 10Hz**
 - **1.2nV/ $\sqrt{\text{Hz}}$ Typical at 1kHz**
- **Maximum Offset Voltage: 50 μ V**
- **Maximum Offset Voltage Drift: 0.5 μ V/ $^{\circ}$ C**
- **CMRR: 124dB (Minimum)**
- **A_{VOL}: 132dB (Minimum)**
- **Slew Rate: 30V/ μ s**
- **Gain-Bandwidth Product: 15MHz**
- **Wide Supply Range: 8V to 33V**
- **Ultralow THD: -115dB at 1kHz**
- **Unity Gain Stable**
- **Low Power Shutdown: 6.2 μ A**
- **SO-8E and 4mm $\times$ 3mm 12-Lead DFN Packages**
- **4.5kV HBM and 2kV CDM Tolerant**

APPLICATIONS

- ADC Driver Applications
- Low Noise Precision Signal Processing
- Multiplexed Applications
- DAC Buffer
- Precision Data Acquisition
- Active Filters
- Professional Audio

DESCRIPTION

The **LT[®]6018** is a 33V precision operational amplifier with excellent noise performance. With 0.1Hz to 10Hz noise of only 30nV_{p-p}, the LT6018 is an outstanding choice for applications where 1/f noise impacts system performance. The LT6018 has excellent DC performance with a maximum offset voltage of 50 μ V and a maximum offset voltage drift of 0.5 μ V/ $^{\circ}$ C. The input offset voltage remains low over the entire common mode input range, providing a minimum CMRR of 124dB. Open loop gain is typically 142dB enabling the part to achieve linearity better than 1ppm. The proprietary circuit topology of the LT6018 provides excellent slew rate and settling time without compromising noise or DC precision.

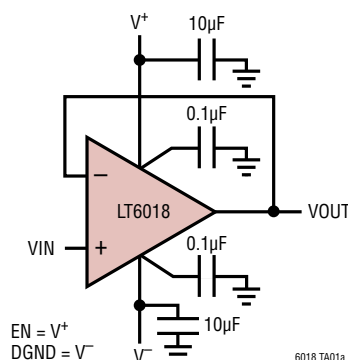
An enable pin allows the LT6018 to be put in a low power shutdown mode, reducing the typical supply current to only 6.2 μ A. A reference pin for the enable pin is also provided, which simplifies the interface between external circuitry and the LT6018.

The LT6018 is available in 8-lead SO and 12-lead 4mm $\times$ 3mm DFN packages, both of which include an exposed pad to reduce thermal resistance. The LT6018 is specified over the -40 $^{\circ}$ C to 85 $^{\circ}$ C and -40 $^{\circ}$ C to 125 $^{\circ}$ C temperature ranges.

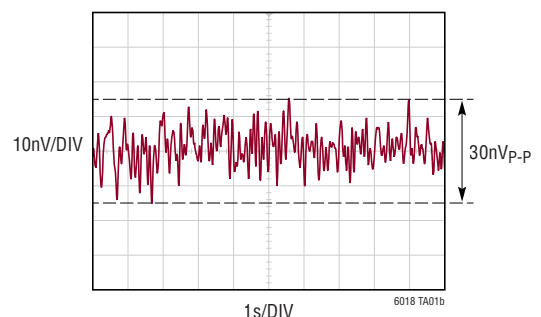
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TYPICAL APPLICATION

Precision Low Noise Buffer



0.1Hz to 10Hz Voltage Noise



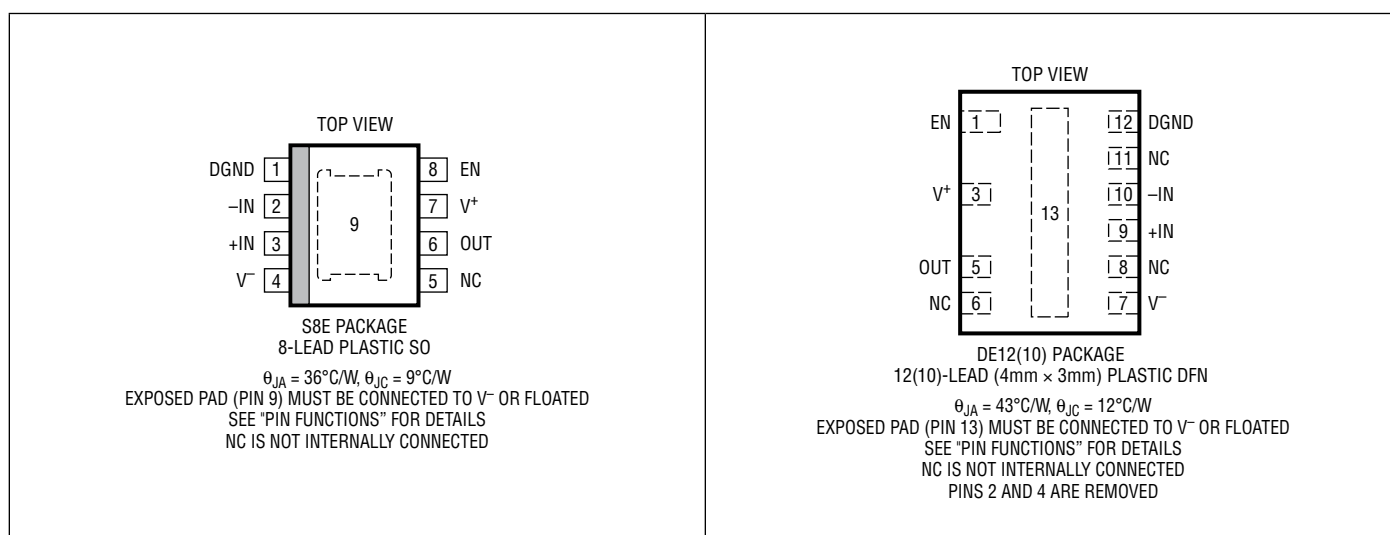
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ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)36V
 Input Voltage
 (+IN, -IN, DGND, EN) ($V^- - 0.3V$) to ($V^+ + 0.3V$)
 Input Current (+IN, -IN, DGND, EN) $\pm 10mA$
 Differential Input Current (+IN, -IN) $\pm 25mA$
 Output Current (Note 2) $50mA_{RMS}$
 Output Short-Circuit Duration Thermally Limited

Operating and Specified Temperature Range
 I-Grade $-40^{\circ}C$ to $85^{\circ}C$
 H-Grade $-40^{\circ}C$ to $125^{\circ}C$
 Maximum Junction Temperature $150^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 S8E Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PIN CONFIGURATION



ORDER INFORMATION <http://www.linear.com/product/LT6018#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6018IS8E#PBF	LT6018IS8E#TRPBF	6018	8-Lead Plastic S8E Exposed Pad	$-40^{\circ}C$ to $85^{\circ}C$
LT6018IDE#PBF	LT6018IDE#TRPBF	6018	12-Lead (4mm x 3mm) Plastic DFN	$-40^{\circ}C$ to $85^{\circ}C$
LT6018HS8E#PBF	LT6018HS8E#TRPBF	6018	8-Lead Plastic S8E Exposed Pad	$-40^{\circ}C$ to $125^{\circ}C$
LT6018HDE#PBF	LT6018HDE#TRPBF	6018	12-Lead (4mm x 3mm) Plastic DFN	$-40^{\circ}C$ to $125^{\circ}C$

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at $T_A = 25^\circ\text{C}$. $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$, $V_{\text{EN}} = 1.7\text{V}$, $V_{\text{DGND}} = 0\text{V}$ unless otherwise noted. V_S is defined as $(V^+ - V^-)$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8E Package	●	± 7	± 50 ± 75	μV μV
		DFN Package	●	± 8	± 70 ± 95	μV μV
$\Delta V_{\text{OS}}/\Delta\text{Time}$	Long Term Input Offset Voltage Stability (Note 3)			0.45		$\mu\text{V}/\text{Mo}$
$\Delta V_{\text{OS}}/\Delta\text{Temp}$	Input Offset Voltage Drift (Note 4)	S8E Package	●	± 0.2	± 0.5	$\mu\text{V}/^\circ\text{C}$
		DFN Package	●	± 0.2	± 0.5	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●	-50 -60	50 60	nA nA
			●			
I_{B}	Input Bias Current	$T_A = -40^\circ\text{C}$ to 85°C	●	-150 -400	-60 400	nA nA
		$T_A = -40^\circ\text{C}$ to 125°C	●	-900	900	nA
	Input Noise Voltage	0.1Hz to 10Hz		30		nV _{p-p}
e_n	Input Noise Voltage Density	$f = 10\text{Hz}$		1.2		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		1.2		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$, Unbalanced Source		3		pA/ $\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$, Balanced Source		0.75		pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	Common Mode		7		pF
		Differential Mode		32		pF
R_{IN}	Input Resistance	Common Mode		50		M Ω
		Differential Mode		30		k Ω
V_{ICM}	Common-Mode Input Range (Note 5)	Guaranteed by CMRR	●	$V^- + 3$	$V^+ - 3$	V
CMRR	Common-Mode Rejection Ratio	$V_{\text{ICM}} = -12\text{V}$ to 12V	●	124 120	133	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 8\text{V}$ to 33V	●	130 128	140	dB dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 500\Omega$, $V_{\text{OUT}} = -10\text{V}$ to 10V	●	132 128	142	dB dB
V_{OL}	Output Swing Low ($V_{\text{OUT}} - V^-$)	No Load		80		mV
		$I_{\text{SINK}} = 1\text{mA}$	●	100	200	mV
			●		700	mV
		$I_{\text{SINK}} = 20\text{mA}$	●	750	1400 1800	mV mV
V_{OH}	Output Swing High ($V^+ - V_{\text{OUT}}$)	No Load		425		mV
		$I_{\text{SOURCE}} = 1\text{mA}$	●	730	800	mV
			●		900	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●	1150	1400 1600	mV mV
I_{SC}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, Sourcing	●	40	90	mA
		$V_{\text{OUT}} = 0\text{V}$, Sinking	●	65	100	mA
SR	Slew Rate	$A_V = 1$, 10V Step	●	20 15	30	V/ μs V/ μs
		$A_V = 1$, 5V Step			20	V/ μs
GBW	Gain-Bandwidth Product	$f = 50\text{kHz}$		12	15	MHz
		$T_A = -40^\circ\text{C}$ to 85°C	●	11		MHz
		$T_A = -40^\circ\text{C}$ to 125°C	●	9		MHz
V_S	Supply Voltage Range	Guaranteed by PSRR	●	8	33	V

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at $T_A = 25^\circ\text{C}$. $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$, $V_{\text{EN}} = 1.7\text{V}$, $V_{\text{DGND}} = 0\text{V}$ unless otherwise noted. V_S is defined as $(V^+ - V^-)$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_S	Supply Current	In Active Mode		7.2	7.65	mA
		$T_A = -40^\circ\text{C}$ to 85°C	●		9	mA
		$T_A = -40^\circ\text{C}$ to 125°C	●		10	mA
		In Shutdown Mode, $V_{\text{EN}} = 0.8\text{V}$	●	6.2	20	μA
THD	Total Harmonic Distortion	$R_L = 600\Omega$, $f = 1\text{kHz}$, $V_{\text{OUT}} = 3V_{\text{RMS}}$, $A_V = 1$		-115		dB
		$R_L = 600\Omega$, $f = 10\text{kHz}$, $V_{\text{OUT}} = 3V_{\text{RMS}}$, $A_V = 1$		-104		dB
		$R_L = 600\Omega$, $f = 1\text{kHz}$, $V_{\text{OUT}} = 20V_{\text{P-P}}$, $A_V = 1$		-106		dB
		$R_L = 600\Omega$, $f = 10\text{kHz}$, $V_{\text{OUT}} = 20V_{\text{P-P}}$, $A_V = 1$		-92		dB
t_S	Settling Time	5V Step 0.0015% (16-Bit), $A_V = 1$, $R_L = 2\text{k}$, $C_L = 100\text{pF}$		1.2		μs
		10V Step 0.0015% (16-Bit), $A_V = 1$, $R_L = 2\text{k}$, $C_L = 100\text{pF}$		1.2		μs
t_{ON}	Enable Time	$A_V = 1$, Settled to 1%		25		μs
V_{DGND}	DGND Pin Voltage Range		●	V^-	$V^+ - 3$	V
I_{DGND}	DGND Pin Current		●	-700	-1400	nA
I_{EN}	EN Pin Current		●	-700	-1400	nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND	●		0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND	●	1.7		V

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$, $V_{\text{EN}} = 1.7\text{V}$, $V_{\text{DGND}} = 0\text{V}$ unless otherwise noted. V_S is defined as $(V^+ - V^-)$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8E Package	●	± 7	± 50	μV
		DFN Package	●	± 8	± 70	μV
$\Delta V_{\text{OS}}/\Delta\text{Temp}$	Input Offset Voltage Drift (Note 4)	S8E Package	●	± 0.2	± 0.5	$\mu\text{V}/^\circ\text{C}$
		DFN Package	●	± 0.2	± 0.5	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●	± 6	50	nA
			●	-60	60	nA
I_B	Input Bias Current	$T_A = -40^\circ\text{C}$ to 85°C	●	-150	-40	150
		$T_A = -40^\circ\text{C}$ to 125°C	●	-400	400	nA
			●	-900	900	nA
	Input Noise Voltage	0.1Hz to 10Hz		30		$\text{nV}_{\text{P-P}}$
e_n	Input Noise Voltage Density	$f = 10\text{Hz}$		1.2		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		1.2		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$, Unbalanced Source		3		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$, Balanced Source		0.75		$\text{pA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	Common Mode		8.3		pF
		Differential Mode		39		pF
R_{IN}	Input Resistance	Common Mode		50		$\text{M}\Omega$
		Differential Mode		30		$\text{k}\Omega$
V_{ICM}	Common-Mode Input Range (Note 5)	Guaranteed by CMRR	●	$V^- + 3$	$V^+ - 3$	V
CMRR	Common-Mode Rejection Ratio	$V_{\text{ICM}} = -2\text{V}$ to 2V	●	122	130	dB
			●	118		dB

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$, $V_{\text{EN}} = 1.7\text{V}$, $V_{\text{DGND}} = 0\text{V}$ unless otherwise noted. V_S is defined as $(V^+ - V^-)$.

PSRR	Power Supply Rejection Ratio	$V_S = 8\text{V to } 33\text{V}$	●	130 128	140	dB dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 500\Omega$, $V_{\text{OUT}} = -2\text{V to } 2\text{V}$	●	130 126	142	dB dB
V_{OL}	Output Swing Low ($V_{\text{OUT}} - V^-$)	No Load $I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SINK}} = 20\text{mA}$	● ● ●		80 100 200 700 900 1400 1800	mV mV mV mV mV mV mV
V_{OH}	Output Swing High ($V^+ - V_{\text{OUT}}$)	No Load $I_{\text{SOURCE}} = 1\text{mA}$ $I_{\text{SOURCE}} = 20\text{mA}$	● ● ●		425 700 800 900 1160 1400 1600	mV mV mV mV mV mV mV
I_{SC}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, Sourcing $V_{\text{OUT}} = 0\text{V}$, Sinking	● ●	40 40	85 60	mA mA
SR	Slew Rate	$A_V = 1$, 4V Step $A_V = 1$, 2V Step			13 10	V/ μs V/ μs
GBW	Gain-Bandwidth Product	$f = 50\text{kHz}$ $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$	● ● ●	11.5 10.5 8.5	14.5	MHz MHz MHz
V_S	Supply Voltage Range	Guaranteed by PSRR	●	8	33	V
I_S	Supply Current	In Active Mode $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ In Shutdown Mode, $V_{\text{EN}} = 0.8\text{V}$	● ● ● ●		6.6 7 8.5 9.5 6 20 50	mA mA mA mA μA μA
THD	Total Harmonic Distortion	$R_L = 100\Omega$, $f = 1\text{kHz}$, $V_{\text{OUT}} = 1.41V_{\text{RMS}}$, $A_V = 1$ $R_L = 100\Omega$, $f = 10\text{kHz}$, $V_{\text{OUT}} = 1.41V_{\text{RMS}}$, $A_V = 1$			-107 -86	dB dB
t_{ON}	Enable Time	$A_V = 1$, Settled to 1%			35	μs
V_{DGND}	DGND Pin Voltage Range		●	V^-	$V^+ - 3$	V
I_{DGND}	DGND Pin Current		●		-700 -1400	nA
I_{EN}	EN Pin Current		●		-700 -1400	nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND	●		0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND	●	1.7		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT6018 is capable of producing peak output currents in excess of 50mA. Current density limitations within the IC require the continuous RMS current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 50mA (Absolute Maximum). Proper heat sinking may be required to keep the junction temperature below the absolute maximum rating. Refer to Figure 9, and the Safe Operating Area section of the data sheet for more information.

Note 3: Long term input offset voltage stability refers to the average trend line of offset voltage vs time over extended periods after the first 30 days of operation.

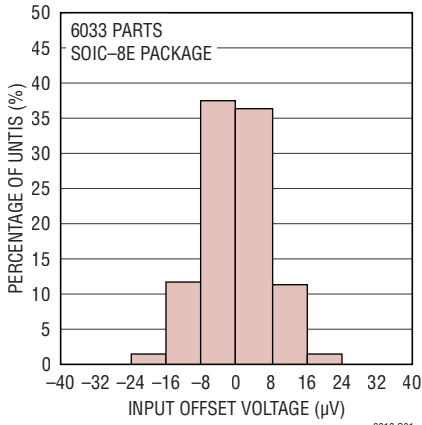
Note 4: Guaranteed by design.

Note 5: The LT6018 input stage is limited to operating between $V^- + 3\text{V}$ and $V^+ - 3\text{V}$. Exceeding this input common mode range will cause a significant increase in input bias current, reduction of open loop gain and degraded stability.

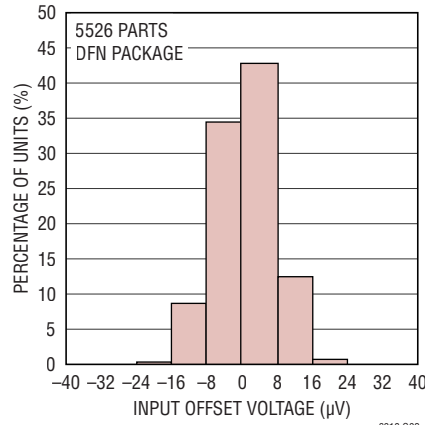
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{EN} = 1.7\text{V}$, $V_{DGND} = 0\text{V}$, $R_L = 500\Omega$ unless otherwise noted.

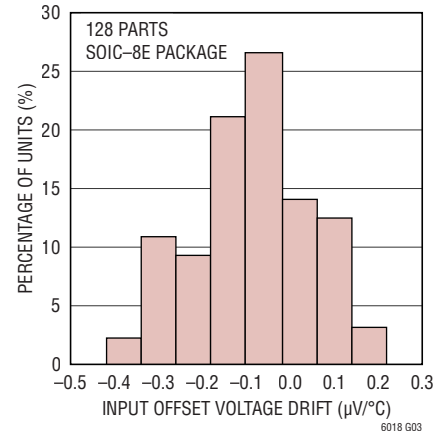
Typical Distribution of Input Offset Voltage



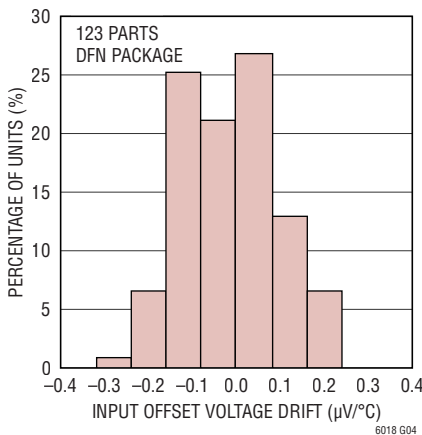
Typical Distribution of Input Offset Voltage



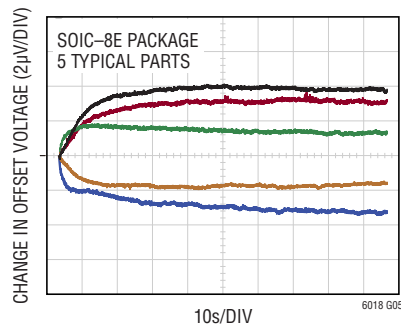
Typical Distribution of Input Offset Voltage Drift



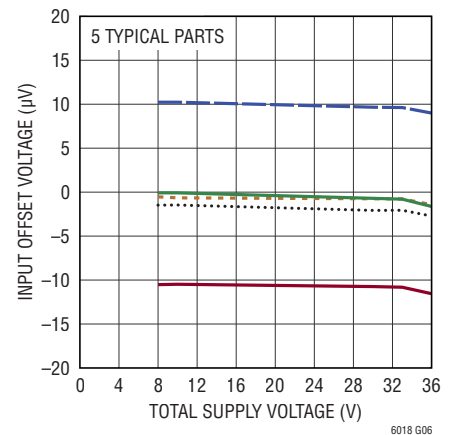
Typical Distribution of Input Offset Voltage Drift



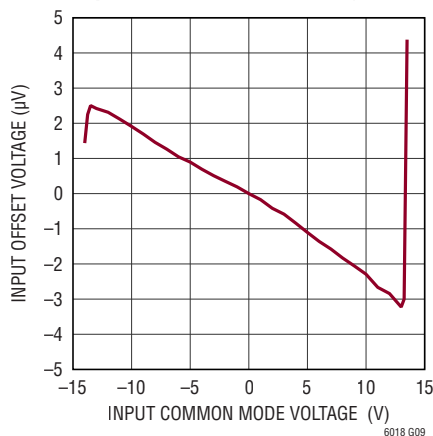
Input Offset Voltage Warm-Up Drift



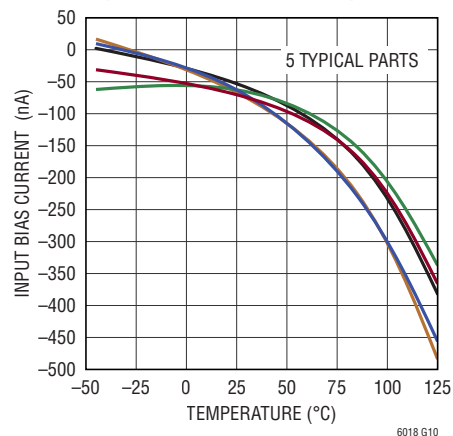
Input Offset Voltage vs Supply Voltage



Input Offset Voltage vs Input Common Mode Voltage



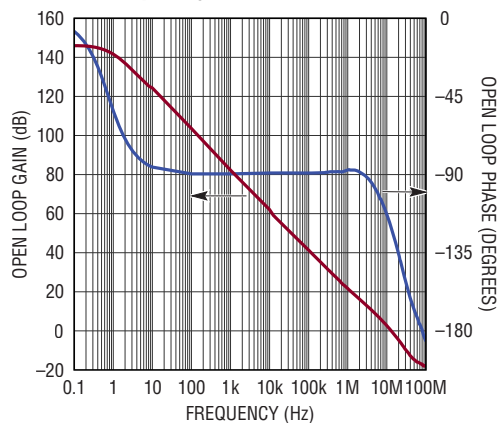
Input Bias Current vs Temperature



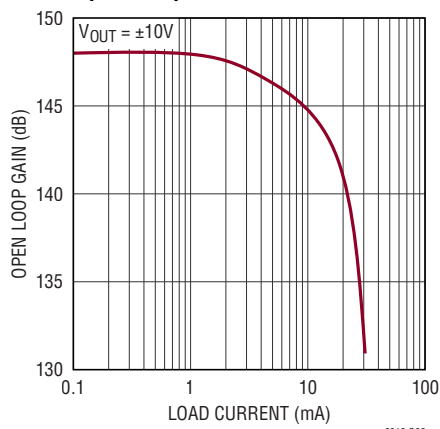
TYPICAL PERFORMANCE CHARACTERISTICS

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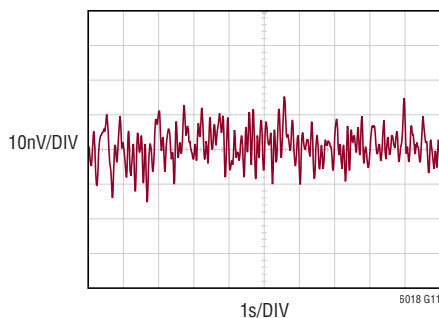
Open-Loop Gain and Phase vs Frequency



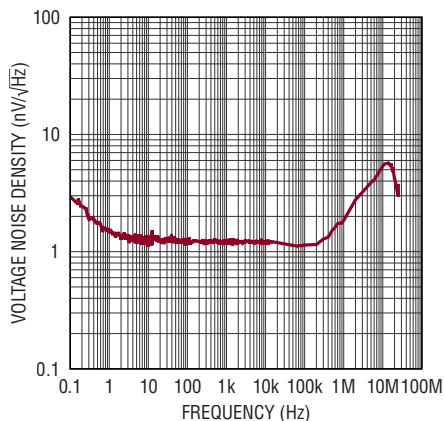
Open-Loop Gain vs Load



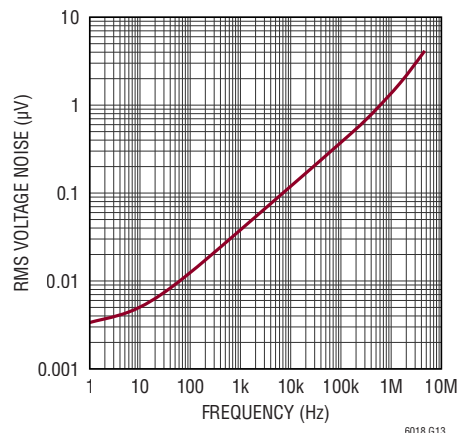
0.1Hz to 10Hz Voltage Noise



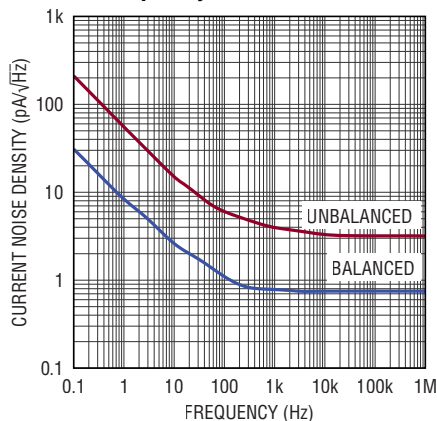
Voltage Noise Density vs Frequency



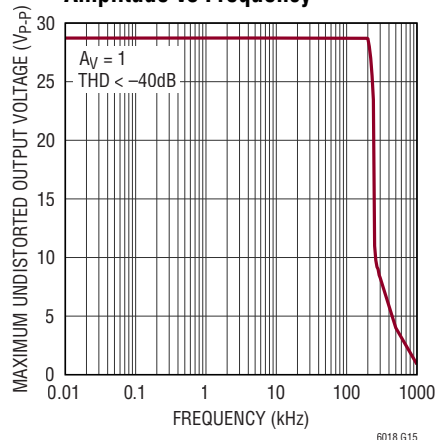
Integrated Voltage Noise (0.1Hz to Frequency Indicated)



Current Noise Density vs Frequency



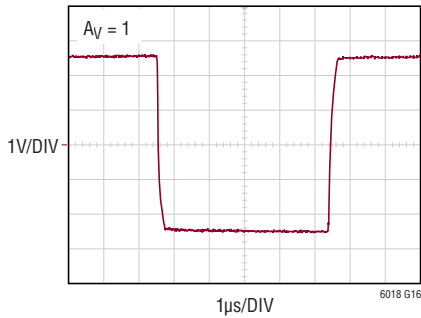
Maximum Undistorted Output Amplitude vs Frequency



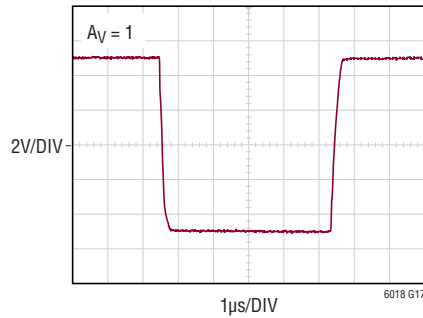
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{EN} = 1.7\text{V}$, $V_{DGND} = 0\text{V}$, $R_L = 500\Omega$ unless otherwise noted.

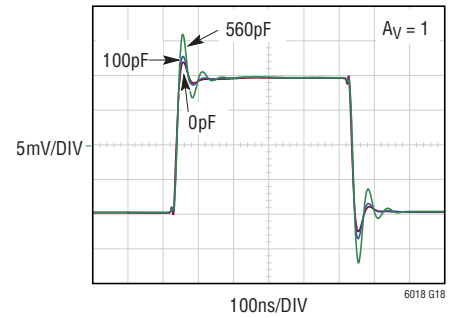
**Large-Signal Transient Response
(5V Step)**



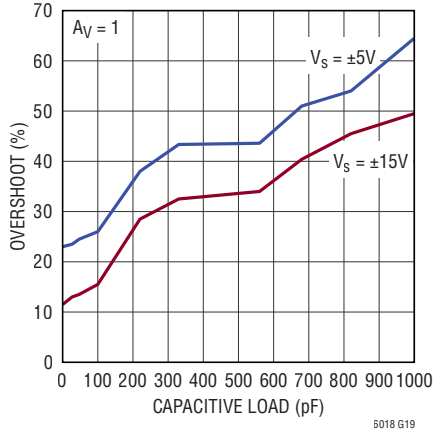
**Large-Signal Transient Response
(10V Step)**



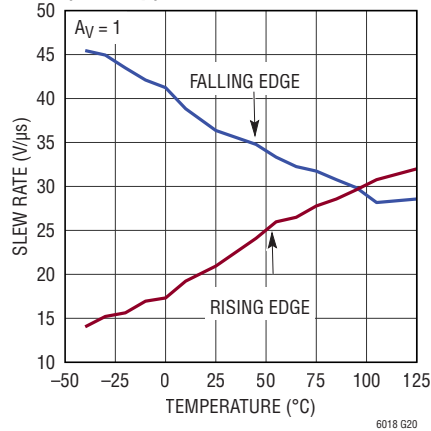
Small-Signal Transient Response



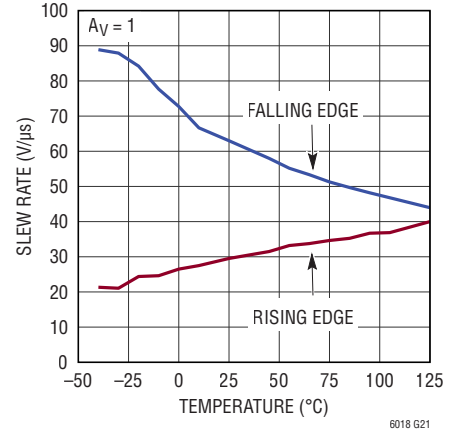
Overshoot vs Capacitive Load



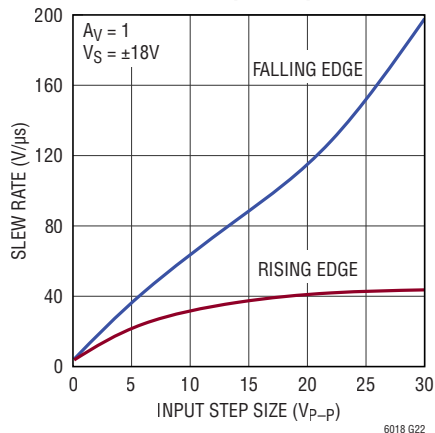
**Slew Rate vs Temperature
(5V Step)**



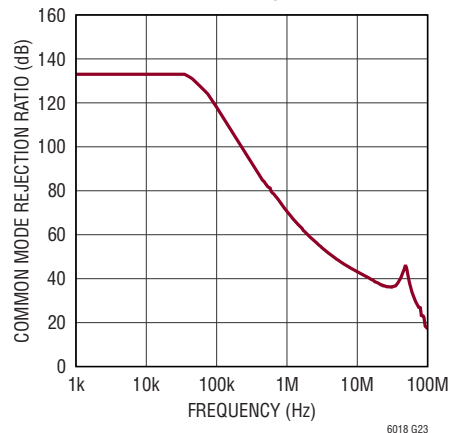
**Slew Rate vs Temperature
(10V Step)**



Slew Rate vs Input Step

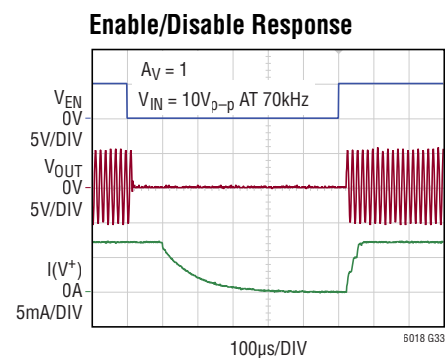
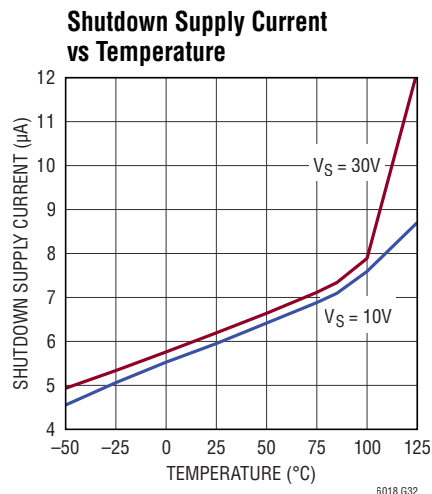
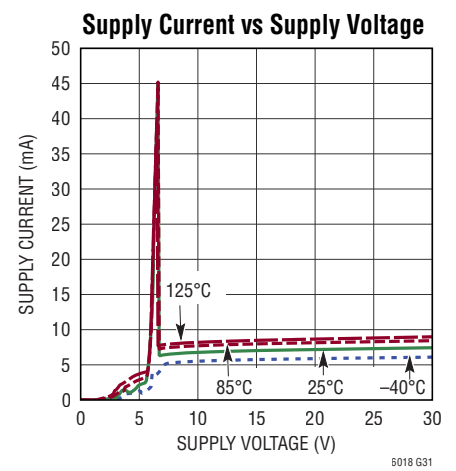
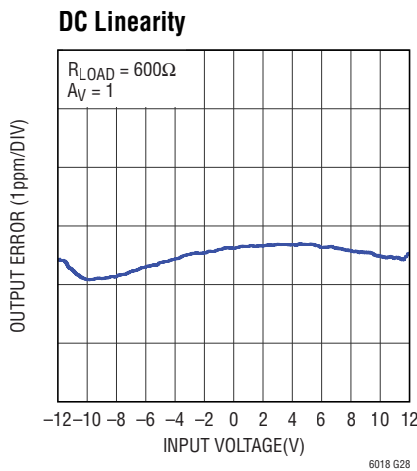
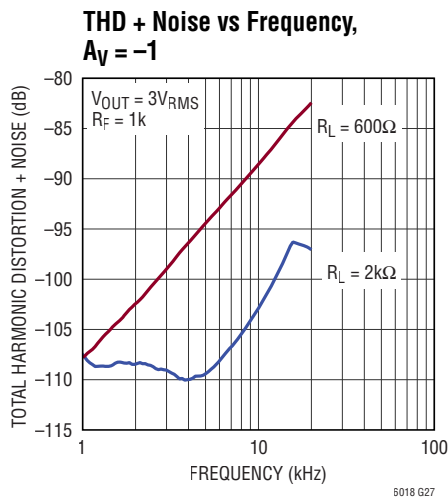
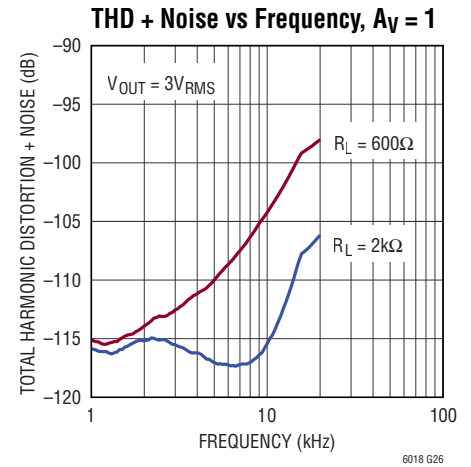
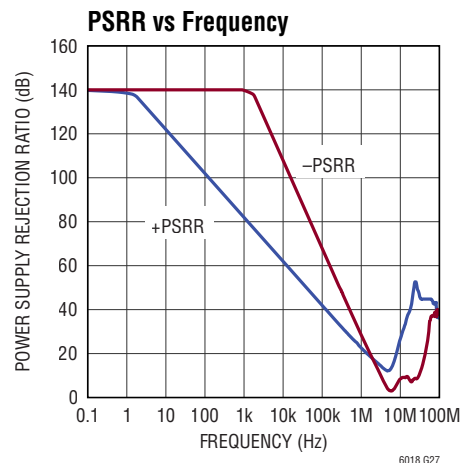
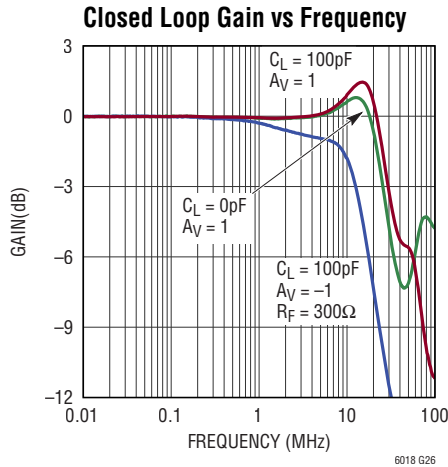


CMRR vs Frequency



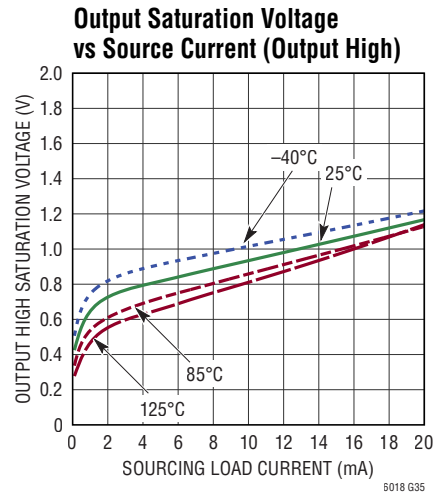
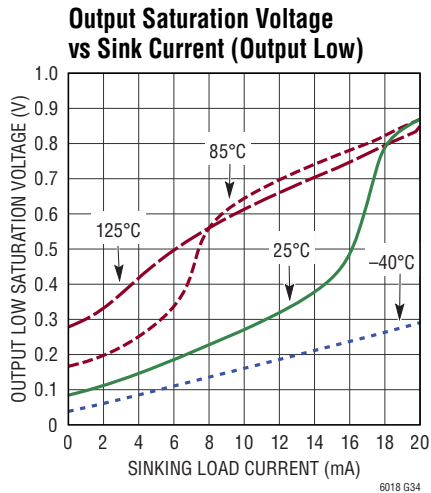
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{EN} = 1.7\text{V}$, $V_{DGND} = 0\text{V}$, $R_L = 500\Omega$ unless otherwise noted.

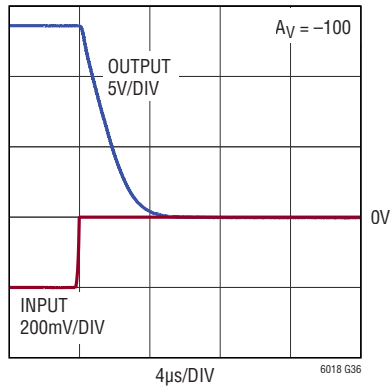


TYPICAL PERFORMANCE CHARACTERISTICS

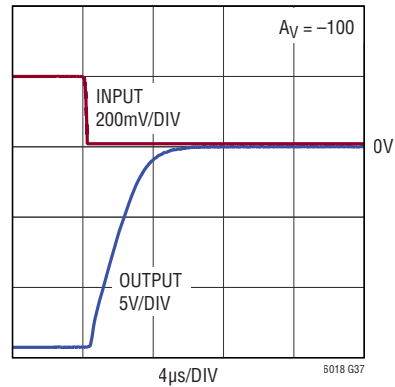
$T_A = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = -15\text{V}$, $V_{EN} = 1.7\text{V}$, $V_{DGND} = 0\text{V}$, $R_L = 500\Omega$ unless otherwise noted.



Positive Output Overdrive Recovery



Negative Output Overdrive Recovery



PIN FUNCTIONS (SOIC-8E/DFN)

DGND (Pin 1/Pins 12): Reference for EN Pin. It is normally tied to ground. DGND must be in the range from V^- to $V^+ - 3V$. If grounded, V^+ must be $\geq 3V$. The EN pin threshold is specified with respect to the DGND pin. DGND cannot be floated.

-IN (Pin 2/Pin 10): Inverting Input of the Amplifier.

+IN (Pin 3/Pin 9): Noninverting Input of the Amplifier.

V^- (Pin 4/Pin 7): Negative Power Supply. Bypass capacitors should be placed as close as possible between the LT6018 supply pins and ground to ensure proper bypassing. Additional bypass capacitance may be used between the power supply pins.

OUT (Pin 6/Pin 5): Amplifier Output. In shutdown mode, the amplifier's output is not high impedance (see Applications section).

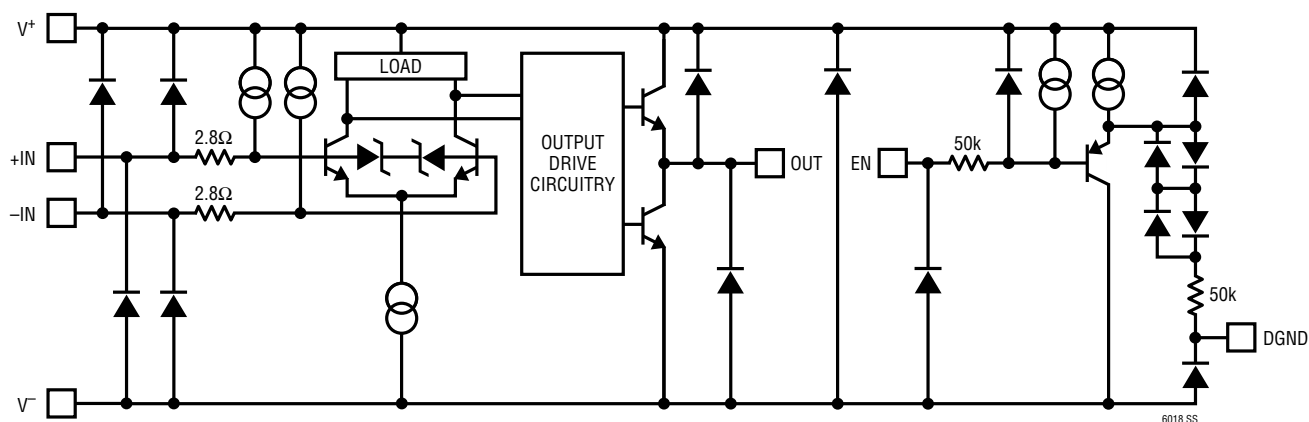
V^+ (Pin 7/Pin 3): Positive Power Supply. Bypass capacitors should be placed as close as possible between the LT6018 supply pins and ground to ensure proper bypassing. Additional bypass capacitance may be used between the power supply pins.

EN (Pin 8/Pin 1): Enable Input. This pin must be connected high, normally to V^+ , for the amplifier to be functional. EN is active high with the threshold approximately two diodes above DGND. EN cannot be floated. The shutdown threshold voltage is specified with respect to the voltage on the DGND pin.

NC (Pin 5/Pins 6, 8, 11): Not internally connected.

Exposed Pad (Pin 9/Pin 13): The exposed pad is electrically connected to V^- , but should not be used to provide power to the part. Use the V^- pin to provide power. The exposed pad can be connected to V^- or floated. Connecting the exposed pad to the V^- plane will improve thermal performance (see Safe Operating Area section).

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

Overview

The proprietary circuitry used in the LT6018 provides a unique combination of precision specifications including ultralow 1/f noise, low broadband noise, low offset and enhanced slew rate without degrading CMRR. The combination of DC specifications and fast settling time allows the LT6018 to solve demanding signal chain requirements. Attention to board layout, supply bypassing and heat sinking must be observed to ensure that the full performance of the LT6018 is realized.

The supply current of the LT6018 increases with large differential input voltages. Normally, this does not impact the LT6018 because the amplifier is forcing the two inputs to be at the same potential. Conditions which cause continuous differential input voltage to appear should be avoided in order to avoid excessive die heating of the LT6018. This includes but is not limited to: operation as a comparator, excessive loading on the output and overdriving the input.

Preserving Input Precision

Preserving the input accuracy of the LT6018 requires that the application circuit and PC board layout do not introduce errors comparable to or greater than the 7μV typical offset of the amplifier. Temperature differentials across the input connections can generate thermocouple voltages of tens of microvolts so the connections of the input leads should be short, close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

In precision applications it is also important to consider amplifier loading when selecting feedback resistor values as well as the loads on the device as these will appear in parallel and affect input offset. See the Feedback Components section for more details.

Noise

The amplifier voltage noise (e_n), positive input current noise (i_{np}), negative input current noise (i_{nn}), source resistance (R_S), and feedback resistors (R_1) and (R_2) are individual voltage noise contributors. The total noise (e_{not}) appearing at the output of the LT6018 will be the root sum square of all the individual voltage noise contributors (Figure 1).

$$e_{not} = \sqrt{e_{no}^2 + e_{rso}^2 + e_{inpo}^2 + e_{r1o}^2 + e_{r2o}^2 + e_{inno}^2}$$

$$G_V = \left(1 + \frac{R_2}{R_1}\right)$$

$$e_{no} = e_n \cdot G_V$$

$$e_{rso} = e_{nrs} \cdot G_V = \sqrt{4kTR_S} \cdot G_V$$

$$e_{inpo} = i_{np} \cdot R_S \cdot G_V$$

$$e_{r1o} = e_{nr1} \cdot \frac{R_2}{R_1} = \sqrt{4kTR_1} \cdot \frac{R_2}{R_1}$$

$$e_{r2o} = e_{nr2} = \sqrt{4kTR_2}$$

$$e_{inno} = i_{nn} \cdot R_2$$

The total input referred voltage noise (e_{nit}) is calculated by dividing the total output referred voltage noise (e_{not}) by the amplifier gain.

$$e_{nit} = \frac{e_{not}}{G_V}$$

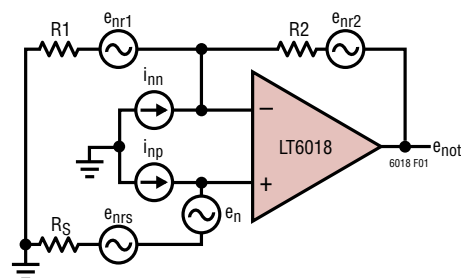


Figure 1. LT6018 Noise Contributors

APPLICATIONS INFORMATION

High Dynamic Input Impedance

Op amps often have protection diodes clamping the two inputs within a diode voltage of each other as seen in Figure 2. During large voltage transitions on the input, these diodes can conduct, since the output cannot respond instantaneously. This can cause circuitry in front of the amplifier as well as the amplifier's own output stage to get overloaded. Often there may be series input resistors (either integrated or discrete) to limit this current, but on extremely low noise parts such as the LT6018, that is not desirable.

The unique input circuitry of the LT6018 does not have this typical diode configuration, but rather a series Zener diode configuration as shown in Figure 3. For 5V input steps, the LT6018 has much higher impedance during transients and allows the user to reduce or eliminate the current limiting resistors, preserving low noise. Figure 4 shows how input bias current increases with differential input voltage for the traditional protection scheme and the LT6018 protection scheme.

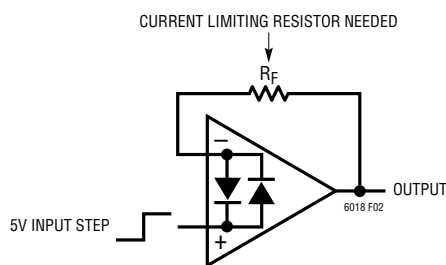


Figure 2. Typical Op Amp Diode Input Protection

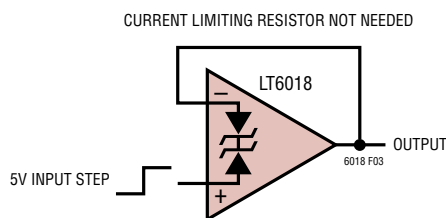


Figure 3. LT6018 Series Zener Diode Input Protection

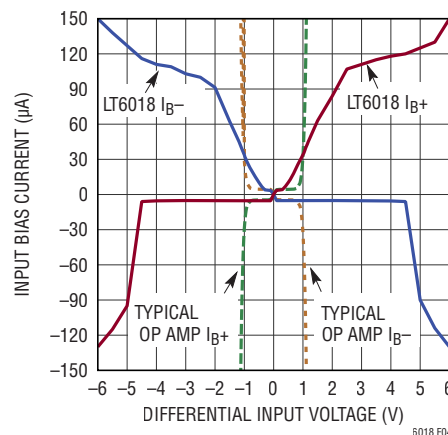


Figure 4. Typical Op Amp vs LT6018 Input Protection

Shutdown Operation

The LT6018 shutdown function has been designed to be easily controlled from single supply logic or micro-controllers. To enable the LT6018 when $V_{DGND} = 0V$ the enable pin must be driven above 1.7V. Conversely, to enter the low power shutdown mode the enable pin must be driven below 0.8V. In a $\pm 15V$ dual supply application where $V_{DGND} = -15V$, the enable pin must be driven above $-13.3V$ to enable the LT6018. If the enable pin is driven below $-14.2V$ the LT6018 enters the low power shutdown mode. Note that to enable the LT6018 the enable pin voltage can range from $-13.3V$ to $15V$ whereas to disable the LT6018 the enable pin can range from $-15V$ to $-14.2V$. Figure 5 shows examples of enable pin control. While in shutdown, the output of the LT6018 is not high impedance. The LT6018 is typically capable of coming out of shutdown within $25\mu s$. This is useful in power sensitive applications where duty cycled operation is employed. In these applications the system is in low power mode the majority of the time, but then needs to wake up quickly and settle for an acquisition before being powered back down to save power.

APPLICATIONS INFORMATION

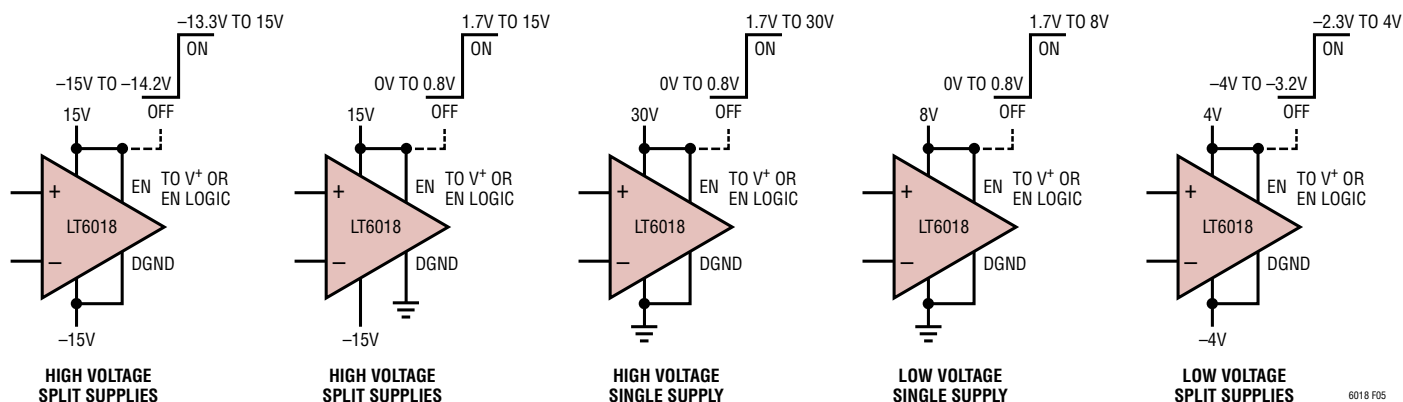


Figure 5. LT6018 Enable Pin Control Examples

Output Leakage in Shutdown Mode

In shutdown mode, the LT6018's output is not high impedance and may conduct a small amount of current due to on-chip leakages. This current can interact with the input protection diodes or any other circuitry connected to the output. Consider the case of a unity gain buffer shown in Figure 6. When the LT6018 is placed in shutdown mode, leakage current flows from the V_{OUT} pin through the input protection diodes causing V_{OUT} to be around 6V. If the output pin is loaded to ground in the same example, the output would be $I_{LEAKAGE} \cdot R_{LOAD}$ above ground. Figure 7 shows the resulting current as the V_{OUT} is swept. In addition, transient voltage applied to the LT6018 output while in shutdown mode may cause the output devices to momentarily conduct.

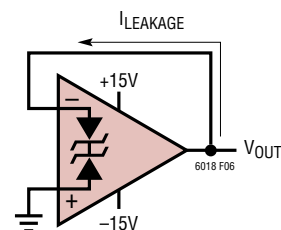


Figure 6. Output Leakage in Shutdown Mode

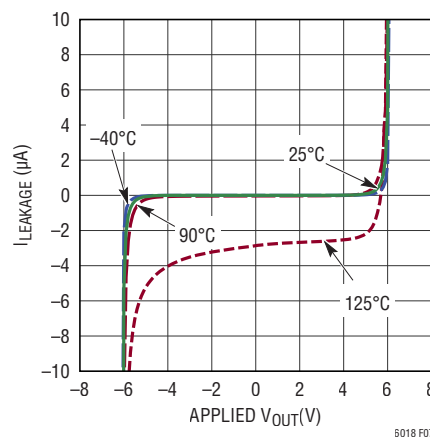


Figure 7. Output Impedance in Shutdown Mode Configured as a Buffer

Feedback Components

To optimize the stability and noise performance of the LT6018, care must be taken when selecting feedback components. For higher resistance values, the pole formed by the inverting parasitic input capacitance and feedback resistors will tend to degrade stability; a lead compensation capacitor across the feedback resistor may be used to eliminate ringing or oscillation. Larger value feedback

APPLICATIONS INFORMATION

GAIN	R _G	R _F	C _F	RTI NOISE, f = 1kHz (nV/√Hz)
2	500Ω	500Ω		2.48
2	1k	1k	5pF	3.46
2	2k	2k	5pF	5.20
5	200Ω	800Ω		2.08
10	100Ω	900Ω		1.73
101	10Ω	1k		1.27
201	5Ω	1k		1.23
201	50Ω	10k		1.51

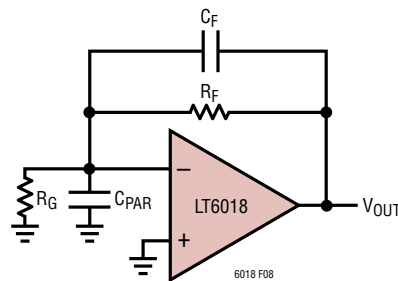


Figure 8. Suggested Feedback Components for Low Noise Stable Operation

resistors will also contribute more thermal noise and further degrade performance (see Applications Information, Noise section). Lower value resistances will tend to improve on these conditions, however, excessive amplifier loading may occur as the feedback network will appear in parallel with the load resistance the LT6018 is required to drive. Figure 8 shows suggested feedback components for maintaining good loop stability and noise performance.

Capacitive Loads

The LT6018 can easily drive capacitive loads up to 100pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance that the amplifier can drive.

Safe Operating Area

The safe operating area, or SOA shown in Figure 9, illustrates the voltage, current and temperature conditions where the LT6018 can be reliably operated. The SOA takes into account the ambient temperature and the power dissipated by the device. This includes the product of the load current and the difference between the supply and output voltage, and the quiescent current and supply voltage.

The LT6018 is safe when operated within the boundaries shown in Figure 9. Thermal resistance junction to case, θ_{JC} , is rated at a constant 9°C/W. Thermal resistance junction to ambient θ_{JA} , is dependent on board layout and any additional heat sinking. Connecting the exposed pad to V^- will reduce θ_{JA} and improve thermal performance. The curves in Figure 9 show the direct effect of θ_{JA} on SOA.

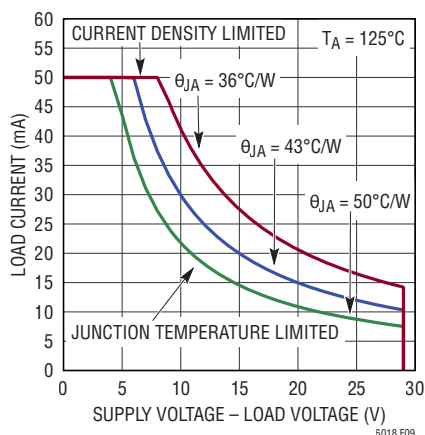


Figure 9. Safe Operating Area

6018 TA02

EN = V⁺
DGND = V⁻

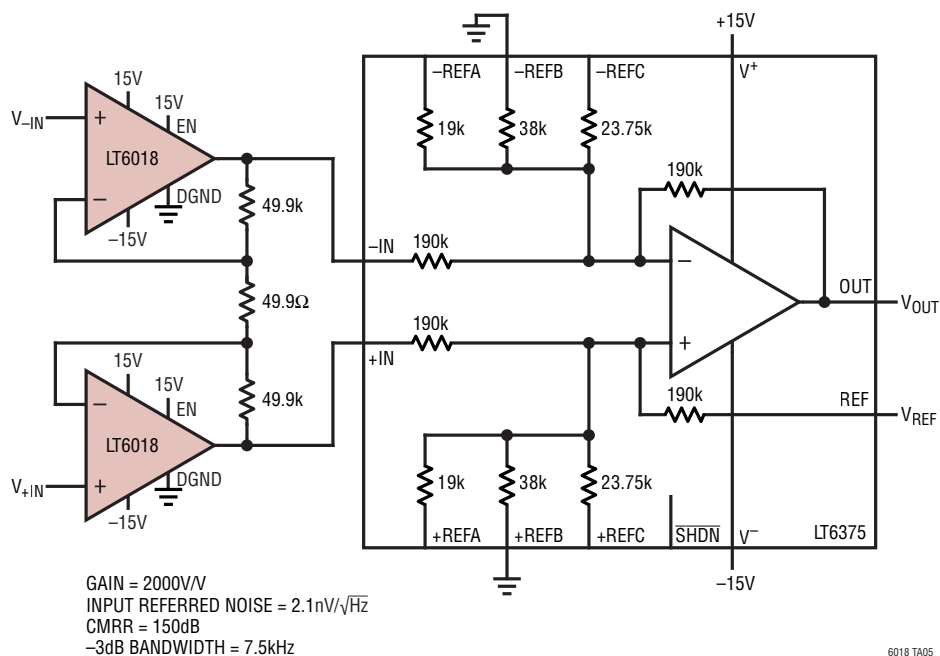
6018 TA03

[illegible]

6018 TA04

TYPICAL APPLICATIONS

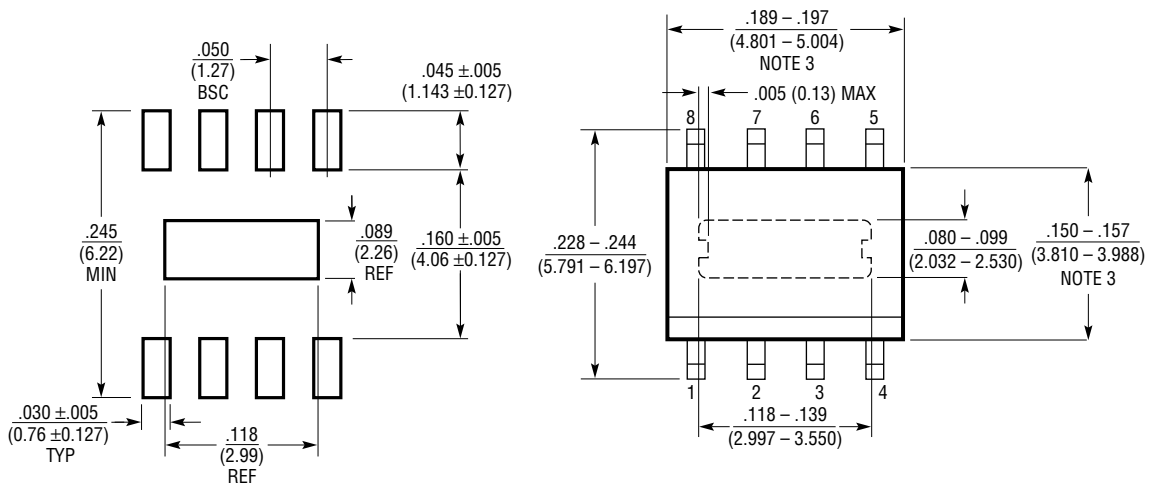
Low Noise, High CMRR Instrumentation Amplifier



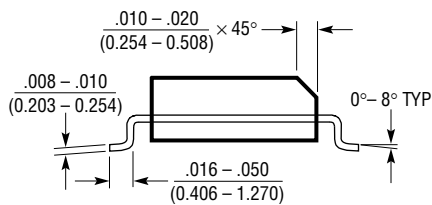
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LT6018#packaging> for the most recent package drawings.

S8E Package 8-Lead Plastic SOIC (Narrow .150 Inch) Exposed Pad (Reference LTC DWG # 05-08-1857 Rev C)

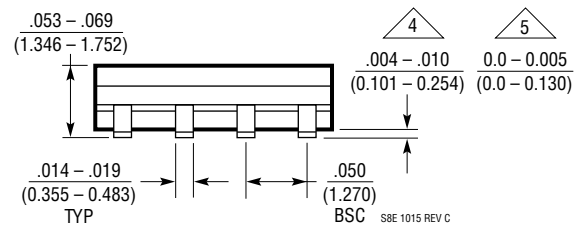


RECOMMENDED SOLDER PAD LAYOUT



- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.010"$ (0.254mm)

4. STANDARD LEAD STANDOFF IS 4mils TO 10mils (DATE CODE BEFORE 542)
5. LOWER LEAD STANDOFF IS 0mils TO 5mils (DATE CODE AFTER 542)



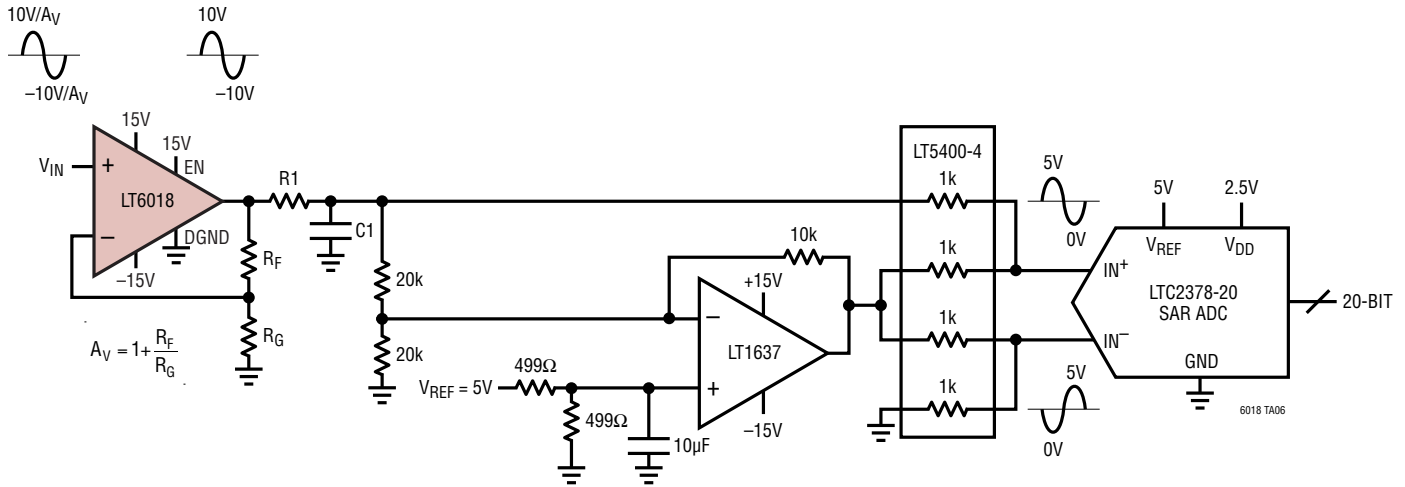
S8E 1015 REV C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/17	Product description changed from 36V to 33V	1
		Package name description changed from SOIC to SO	1
		Long Term Input Offset Voltage Stability added	3
		Note 3 added for Long Term Input Offset Voltage Stability. Note 3 and Note 4 renamed Note 4 and Note 5, respectively	5

TYPICAL APPLICATIONS

Driving LTC2378-20 with $\pm 10\text{V}$ Input Signal ($f_{\text{IN}} = 100\text{Hz}$, -1dBFS , 800ksps)



A_V (V/V)	COMPONENT VALUES	SNR (dB)	THD (dB)	SFDR (dB)
1	$R_F = 0\Omega$, $R_G = \text{OPEN}$, $R_1 = 0\Omega$, $C_1 = \text{OPEN}$	102.5	-121.6	123.0
10	$R_F = 900\Omega$, $R_G = 100\Omega$, $R_1 = 10\Omega$, $C_1 = 0.01\mu\text{F}$	100.6	-99.8	100.0

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Ultralow Noise, Precision High Speed Op Amp, $A_V \geq 2$ Stable	0.1Hz to 10Hz Noise = $35\text{nV}_{\text{P-P}}$, $e_n = 0.85\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 40\mu\text{V}$, $\text{SR} = 15\text{V}/\mu\text{s}$, $\text{GBW} = 75\text{MHz}$, $I_S = 7.4\text{mA}$
LT1128	Ultralow Noise, Precision High Speed Op Amp, $A_V = +1$ Stable	0.1Hz to 10Hz Noise = $35\text{nV}_{\text{P-P}}$, $e_n = 0.85\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 40\mu\text{V}$, $\text{SR} = 6\text{V}/\mu\text{s}$, $\text{GBW} = 20\text{MHz}$, $I_S = 7.4\text{mA}$
LT1115	Ultralow Noise, Low Distortion, Audio Op Amp	DC to 20kHz Noise = $0.5\mu\text{V}_{\text{P-P}}$, $e_n = 0.9\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 200\mu\text{V}$, $\text{SR} = 15\text{V}/\mu\text{s}$, $\text{GBW} = 70\text{MHz}$, $I_S = 8.5\text{mA}$
LT1037	Low Noise, High Speed Precision Op Amp, $A_V \geq 5$ Stable	0.1Hz to 10Hz Noise = $60\text{nV}_{\text{P-P}}$, $e_n = 2.5\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 25\mu\text{V}$, $\text{SR} = 15\text{V}/\mu\text{s}$, $\text{GBW} = 60\text{MHz}$, $I_S = 2.7\text{mA}$
LT1007	Low Noise, High Speed Precision Op Amp, $A_V = +1$ Stable	0.1Hz to 10Hz Noise = $60\text{nV}_{\text{P-P}}$, $e_n = 2.5\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 25\mu\text{V}$, $\text{SR} = 2.5\text{V}/\mu\text{s}$, $\text{GBW} = 8\text{MHz}$, $I_S = 2.7\text{mA}$
LT1468	Low Noise, 16-Bit Op Amp	0.1Hz to 10Hz Noise = $0.3\mu\text{V}_{\text{P-P}}$, $e_n = 5\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 75\mu\text{V}$, $\text{SR} = 22\text{V}/\mu\text{s}$, $\text{GBW} = 90\text{MHz}$, $I_S = 3.9\text{mA}$
LT6020	Low Power, Enhanced Slew Op Amp	0.1Hz to 10Hz Noise = $1.1\mu\text{V}_{\text{P-P}}$, $e_n = 46\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 30\mu\text{V}$, $\text{SR} = 5\text{V}/\mu\text{s}$, $\text{GBW} = 400\text{kHz}$, $I_S = 100\mu\text{A}$
LT6023	Micropower, Enhanced Slew Op Amp	0.1Hz to 10Hz Noise = $3.0\mu\text{V}_{\text{P-P}}$, $e_n = 132\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 30\mu\text{V}$, $\text{SR} = 1.4\text{V}/\mu\text{s}$, $\text{GBW} = 40\text{kHz}$, $I_S = 20\mu\text{A}$
LTC2057	High Voltage, Low Noise, Zero Drift Amplifier	DC to 10Hz Noise = $200\text{nV}_{\text{P-P}}$, $e_n = 11\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 4\mu\text{V}$, $\text{SR} = 0.45\text{V}/\mu\text{s}$, $\text{GBW} = 1.5\text{MHz}$, $I_S = 0.8\text{mA}$
LTC6240	Low Noise, CMOS Amplifier	0.1Hz to 10Hz Noise = $550\text{nV}_{\text{P-P}}$, $e_n = 7\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 125\mu\text{V}$, $\text{SR} = 10\text{V}/\mu\text{s}$, $\text{GBW} = 18\text{MHz}$, $I_S = 1.8\text{mA}$
LT6230	Low Noise, Rail-to-Rail Output Amplifier	0.1Hz to 10Hz Noise = $180\text{nV}_{\text{P-P}}$, $e_n = 1.1\text{nV}/\sqrt{\text{Hz}}$, $V_{\text{OS}} = 500\mu\text{V}$, $\text{SR} = 60\text{V}/\mu\text{s}$, $\text{GBW} = 215\text{MHz}$, $I_S = 3.15\text{mA}$