

54/74170 011734
54LS/74LS170 011735
4 X 4 REGISTER FILE
 (With Open-Collector Outputs)

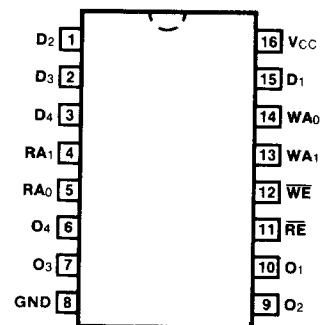
DESCRIPTION — The '170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 X 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features 3-state outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**

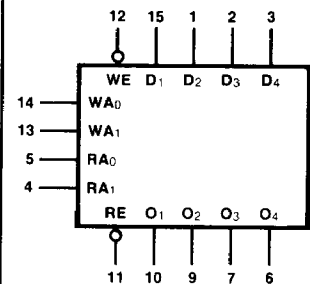
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74170PC, 74LS170PC		9B
Ceramic DIP (D)	A	74170DC, 74LS170DC	54170DM, 54LS170DM	7B
Flatpak (F)	A	74170FC, 74LS170FC	54170FM, 54LS170DM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



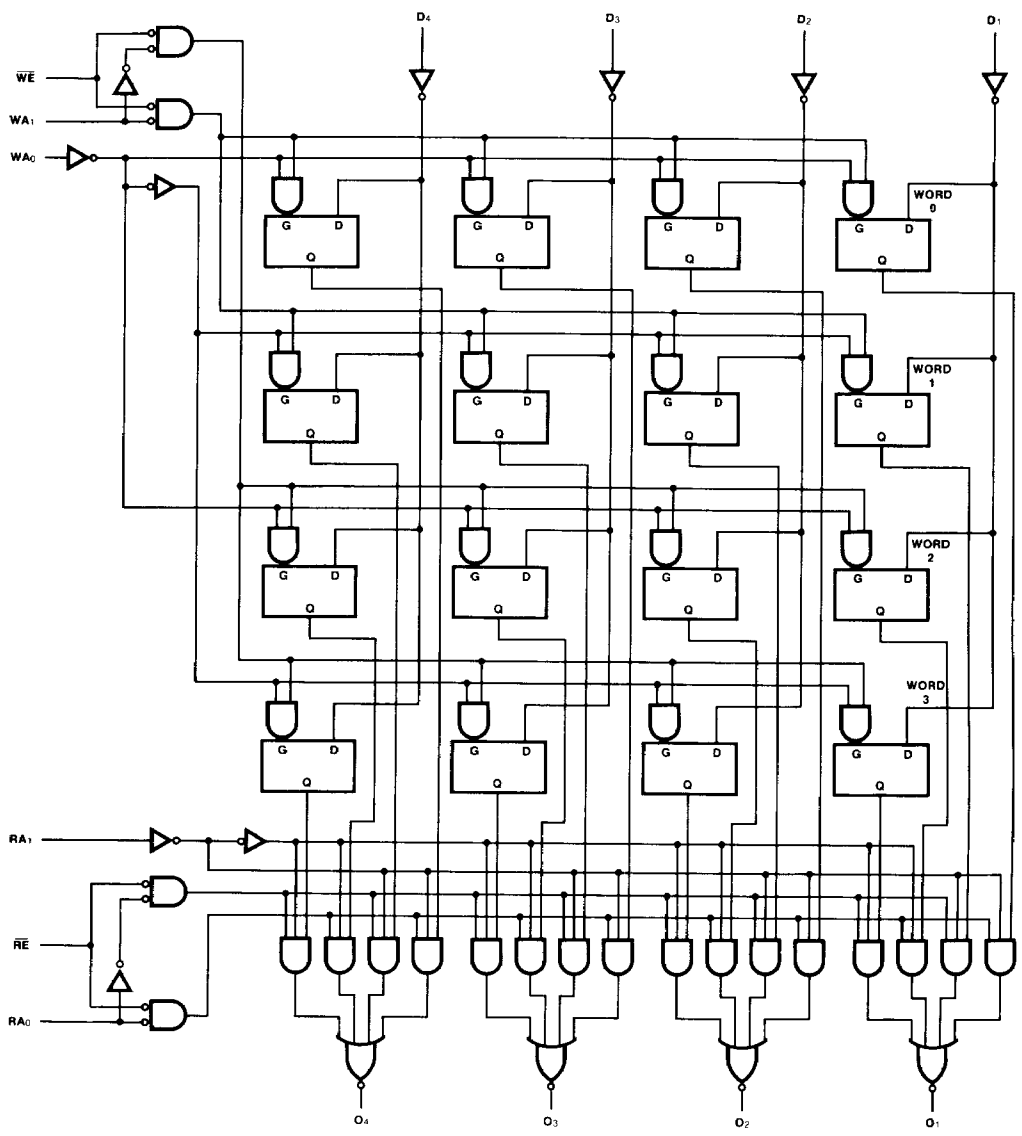
V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D ₁ — D ₄	Data Inputs	1.0/1.0	0.5/0.25
WA ₀ , WA ₁	Write Address Inputs	1.0/1.0	0.5/0.25
WE	Write Enable Input (Active LOW)	1.0/1.0	1.0/0.5
RA ₀ , RA ₁	Read Address Inputs	1.0/1.0	0.5/0.25
RE	Read Enable Input (Active LOW)	1.0/1.0	1.0/0.5
O ₁ — O ₄	Data Outputs	OC*/10	OC*/5.0 (2.5)

*OC — Open Collector

LOGIC DIAGRAM



WRITE FUNCTION TABLE

WRITE INPUTS			D INPUTS TO
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

READ FUNCTION TABLE

READ INPUTS			OUTPUTS FROM
$\overline{RE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I _{OH}	Output HIGH Current		30		20		μA	V _{CC} = Min, V _{OH} = 5.5 V
I _{CC}	Power Supply Current	XC	150		40		mA	V _{CC} = Max; D _n , $\overline{WE}$, $\overline{RE}$ = 4.5 V; WA _n , RA _n = Gnd
		XM	140		40			

AC CHARACTERISTICS: $V_{CC} = +5.0 V$, $T_A = +25^\circ C$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay* RA ₀ or RA ₁ to O _n	35 40		35 35		ns	Figs. 3-1, 3-20
t _{PLH} t _{PHL}	Propagation Delay RE to O _n	15 30		30 30		ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay WE to O _n	40 45		35 35		ns	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	30 45		35 35		ns	Figs. 3-1, 3-5

*Measured at least 25 ns after entry of new data at selected location.

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 V$, $T_A = +25^\circ C$

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s	Setup Time HIGH or LOW D_n to rising $\overline{WE}$	10		10		ns	Fig. a
t_h	Hold Time HIGH or LOW D_n to rising $\overline{WE}$	15		5.0		ns	
t_s	Setup Time HIGH or LOW WA_n to falling $\overline{WE}$	15		10		ns	
t_h	Hold Time HIGH or LOW WA_n to rising $\overline{WE}$	5.0		5.0		ns	
$t_w (L)$	$\overline{WE}$ or $\overline{RE}$ Pulse Width LOW	25		25		ns	

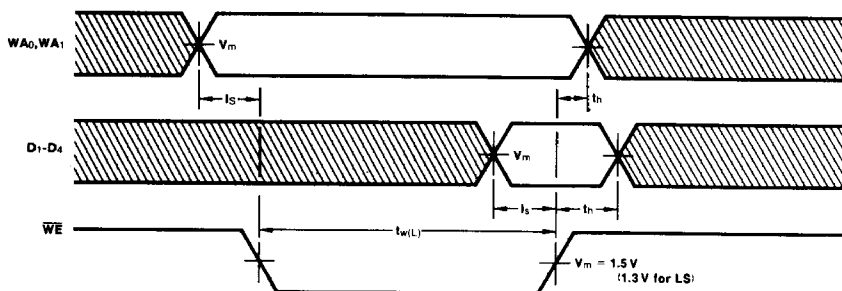


Fig. a