



MP174A

700V Non-Isolated Off-Line Regulator, Up to 400mA Output Current with Improved EMI Performance

DESCRIPTION

The MP174A is a primary-side regulator that provides accurate constant voltage (CV) regulation without an opto-coupler. It supports buck, buck-boost, boost, and flyback topologies. It has an integrated 700V MOSFET to simplify the structure and reduce costs. These features make it an ideal regulator for off-line low power applications, such as home appliances and standby power.

The MP174A is a green-mode-operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load and improves the overall average efficiency.

The MP174A has various protection features, including thermal shutdown (OTP), VCC under-voltage lockout (UVLO), over-load protection (OLP), short-circuit protection (SCP), and open-loop detection.

The MP174A is available in a small TSOT23-5 package and SOIC8 package.

FEATURES

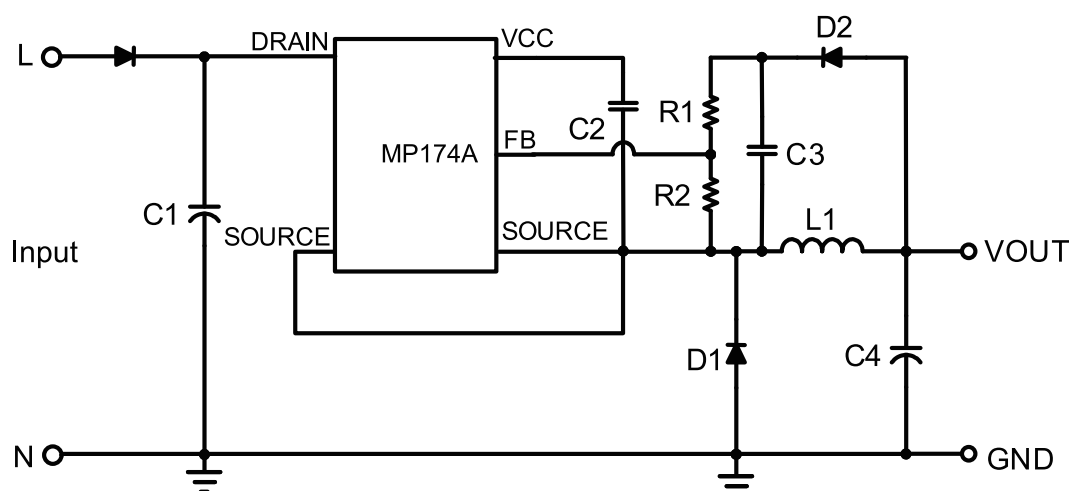
- Primary-Side CV Control, supporting Buck, Buck-Boost, Boost, and Flyback Topologies
- Integrated 700V/13.5Ω MOSFET and Current Source
- <30mW No-Load Power Consumption
- Up to 5W Output Power
- Maximum DCM Output Current Less than 250mA
- Maximum CCM Output Current Less than 400mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- OTP, UVLO, OLP, SCP, Open-Loop Detection

APPLICATIONS

- Home Appliances, White Goods and Consumer Electronics
- Industrial Controls
- Standby Power

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MP174AGJ*	TSOT23-5	<i>See Below</i>
MP174AGS**	SOIC-8	<i>See Below</i>

* For Tape & Reel, add suffix -Z (e.g. MP174AGJ-Z).

** For Tape & Reel, add suffix -Z (e.g. MP174AGS-Z).

TOP MARKING (MP174AGJ)

| BJKY

BJK: Product code of MP174AGJ

Y: Year code

TOP MARKING (MP174AGS)

MP174A
LLLLLLLL
MPSYWW

MP174A: Part number

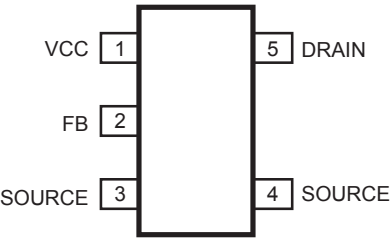
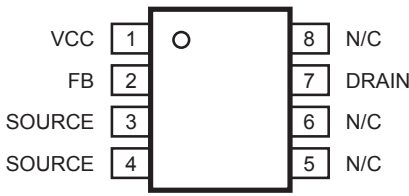
LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
 VCC 1 5 DRAIN FB 2 SOURCE 3 4 SOURCE	 VCC 1 8 N/C FB 2 7 DRAIN SOURCE 3 6 N/C SOURCE 4 5 N/C
TSOT23-5	SOIC-8

PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Control circuit power supply.
2	2	FB	Regulator feedback.
3,4	3,4	SOURCE	Internal power MOSFET source. Ground reference for VCC and FB pins.
5	7	DRAIN	Internal power MOSFET drain. High-voltage current source input.
	5,6,8	N/C	Not connected.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Drain to source.....	-0.3V to 700V
All other pins	-0.3V to 6.5V
Continuous Power Dissipation.... (T _A = +25°C) ⁽²⁾	
TSOT23-5	1W
SOIC8.....	1W
Junction Temperature.....	150°C
Lead Temperature	260°C
Storage Temperature.....	-60°C to +150°C
ESD Capability Human Body Mode	2.0kV
ESD Charged Device Model	
TSOT23-5	1.5kV
SOIC8.....	2.0kV

Recommended Operating Conditions ⁽³⁾

Operating Junction Temp. (T _J).	-40°C to +125°C
Operating VCC range	5.3V to 5.6V

Thermal Resistance ⁽⁴⁾

	θ_{JA}	θ_{JC}
TSOT23-5	100	55
SOIC-8	96	45

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowance continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowance power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

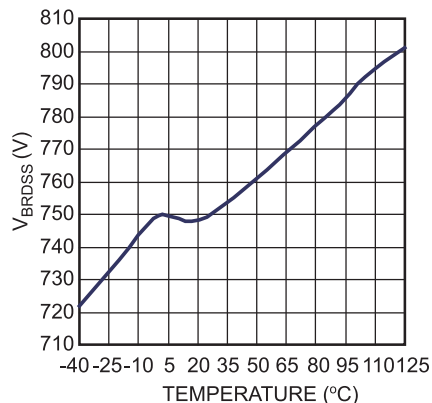
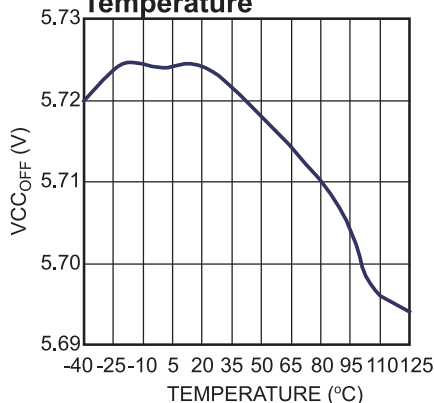
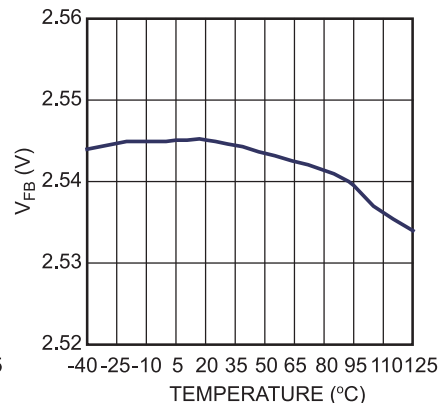
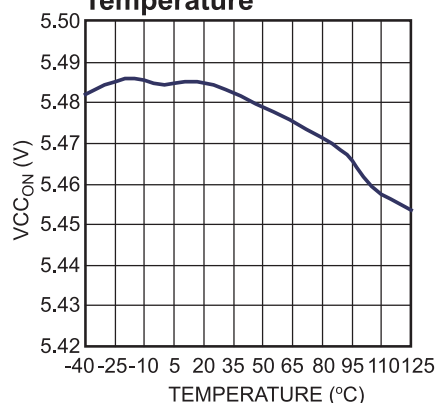
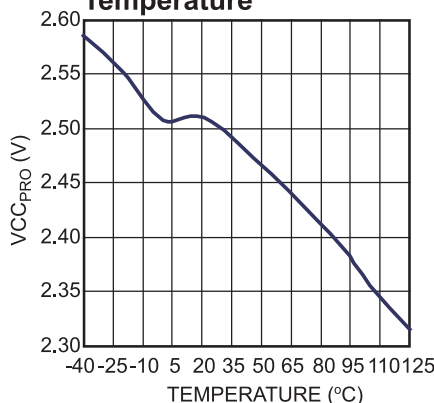
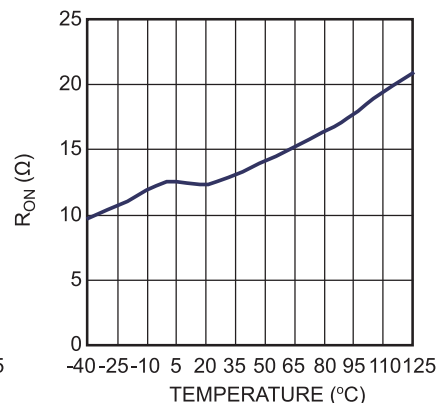
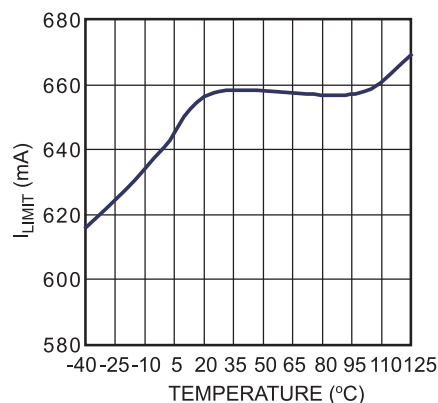
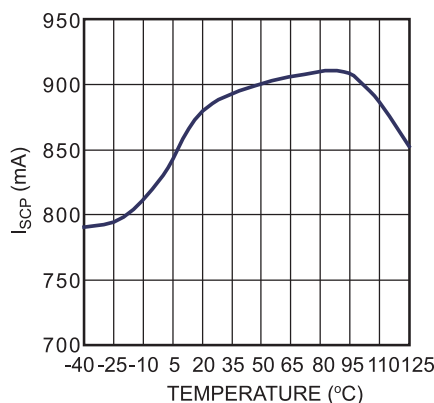
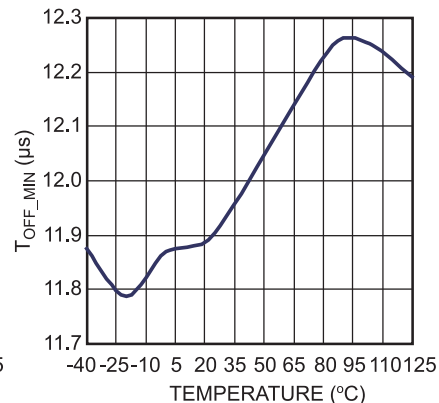
VCC = 5.5V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source and Internal MOSFET (Drain Pin)						
Internal regulator supply current	I _{Regulator}	V _{CC} =4V; V _{Drain} =100V	2.2	4.1	6	mA
Drain pin leakage current	I _{Leak}	V _{CC} =5.8V; V _{Drain} =500V		10	17	μA
Breakdown voltage	V _{(BR)DSS}	T _J =25°C	700			V
ON resistance	R _{ON}	T _J =25°C		13.5	17	Ω
		T _J =125°C		21	25	Ω
Supply Voltage Management (VCC Pin)						
VCC level (increasing) where the internal regulator stops	V _{CCOFF}		5.4	5.6	6	V
VCC level (decreasing) where the internal regulator turns on	V _{CCON}		5.1	5.3	5.7	V
VCC regulator on and off hysteresis			130	250		mV
VCC level (decreasing) where the IC stops	V _{CCStop}		3	3.4	3.6	V
VCC level (decreasing) where the protection phase ends	V _{CCPro}			2.4	2.8	V
Internal IC consumption	I _{CC}	f _s =28kHz, D=66.7%			720	μA
		No switching			200	μA
		V _{CC} =5.3V, latch-off phase		16	24	μA
Internal Current Sense						
Peak current limit	I _{Limit}	T _J =25°C	600	660	720	mA
Leading-edge blanking	τ _{LEB1}			350		ns
SCP threshold	I _{SCP}	T _J =25°C	750	900		mA
Leading-edge blanking for SCP ⁽¹⁾	τ _{LEB2}			180		ns
Feedback Input (FB Pin)						
Minimum off time	τ _{Min_off}		9.5	12	15	μs
Maximum on time	τ _{Max_on}		19	24	31	μs
Primary MOSFET feedback turn-on threshold	V _{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	V _{FB_OLP}		1.6	1.7	1.8	V
OLP delay time	τ _{OLP}	f _s =28kHz		220		ms
Open-loop detection	V _{OLD}		0.4	0.5	0.6	V
Thermal Shutdown						
Thermal shutdown threshold ⁽¹⁾				150		°C
Thermal shutdown recovery hysteresis ⁽¹⁾				30		°C

Notes:

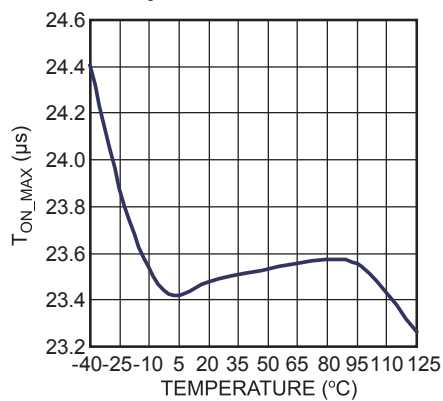
1) This parameter is guaranteed by design.

TYPICAL CHARACTERISTICS

Breakdown Voltage vs. Temperature

VCC Increasing Level at which the Internal Regulator Stops vs. Temperature

Feedback Voltage vs. Temperature

VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature

VCC Decreasing Level at which the Protection Phase Ends vs. Temperature

On State Resistance vs. Temperature

Peak Current Limit vs. Temperature

SCP Point vs. Temperature

Minimum Off Time vs. Temperature


TYPICAL CHARACTERISTICS *(continued)*

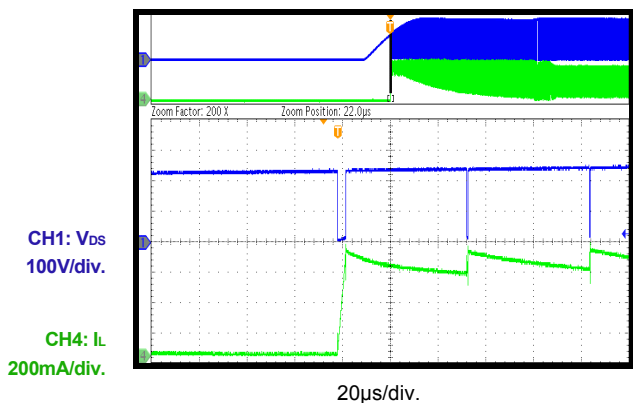
Maximum On Time vs. Temperature



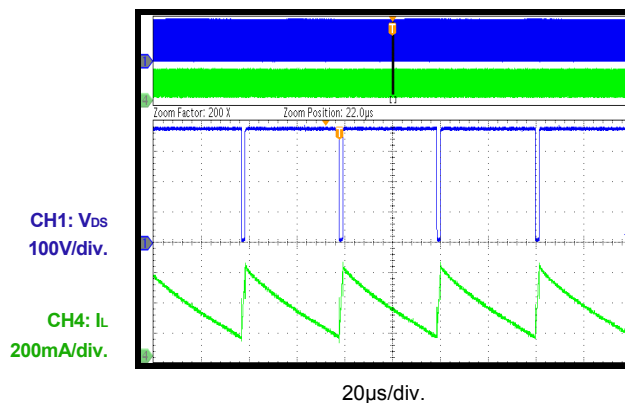
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 265VAC$, $V_{OUT} = 12V$, $I_{OUT} = 300mA$, $L = 1.2mH$, $C_{OUT} = 100\mu F$, $T_A = +25^{\circ}C$, unless otherwise noted.

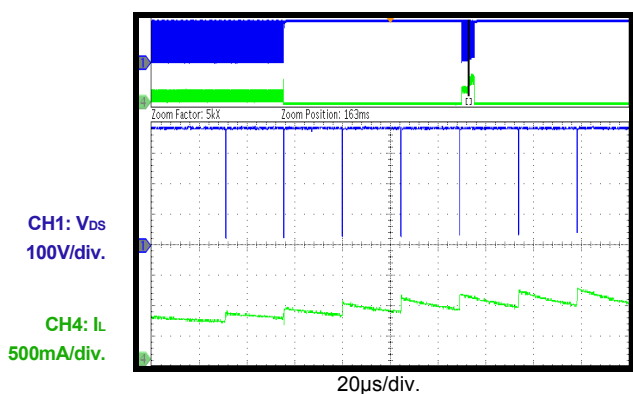
Start-Up



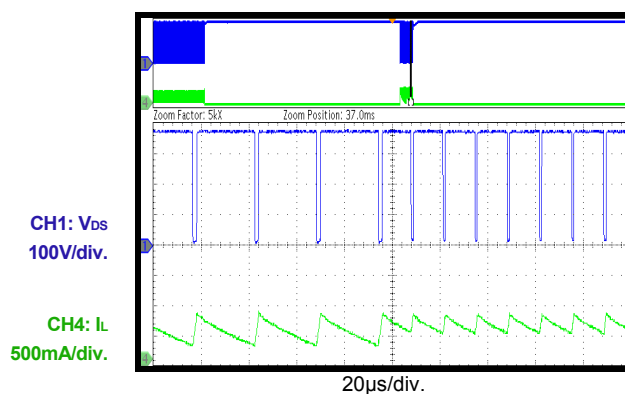
Normal Operation



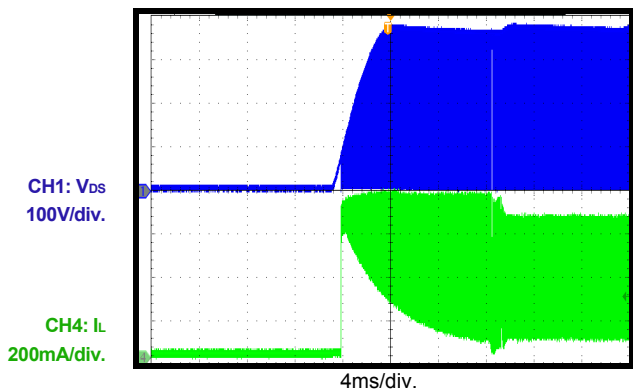
SCP



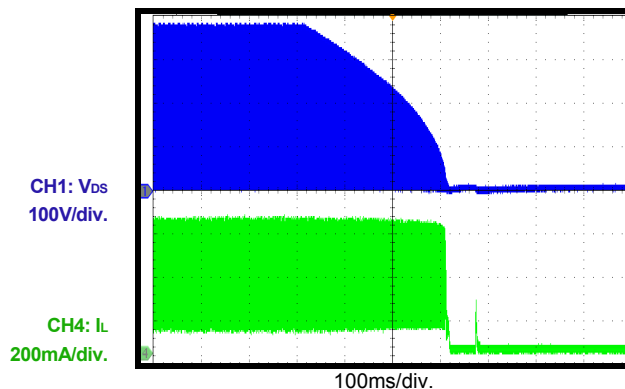
Open Loop Detection



Input Power Start-Up



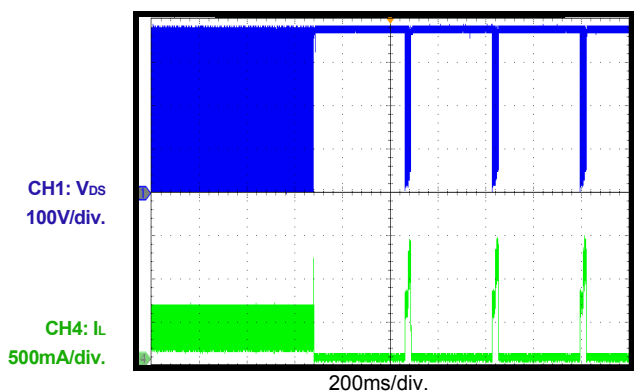
Input Power Shutdown



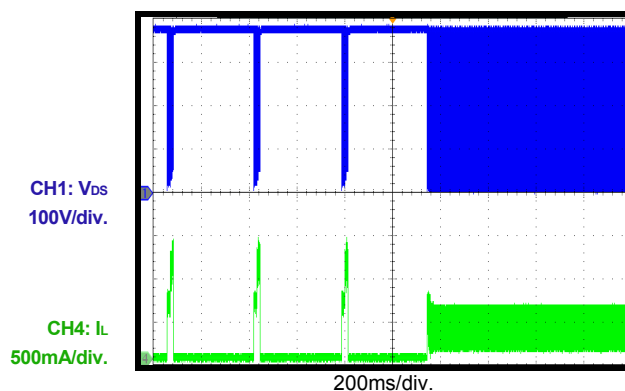
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 265VAC$, $V_{OUT} = 12V$, $I_{OUT} = 300mA$, $L = 1.2mH$, $C_{OUT} = 100\mu F$, $T_A = +25^{\circ}C$, unless otherwise noted.

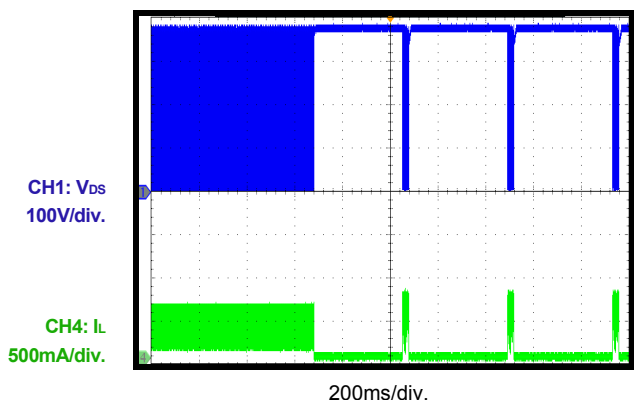
SCP Entry



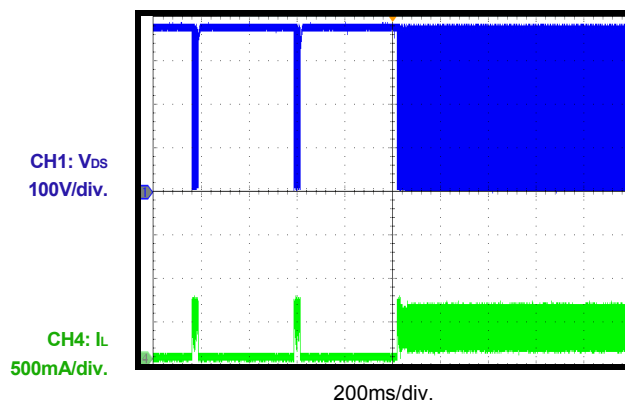
SCP Recovery



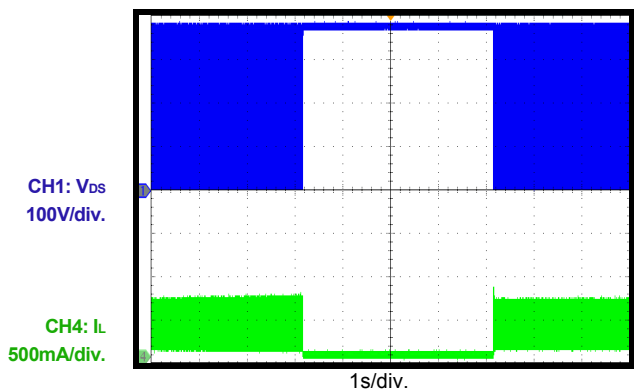
Open Loop Detection Entry



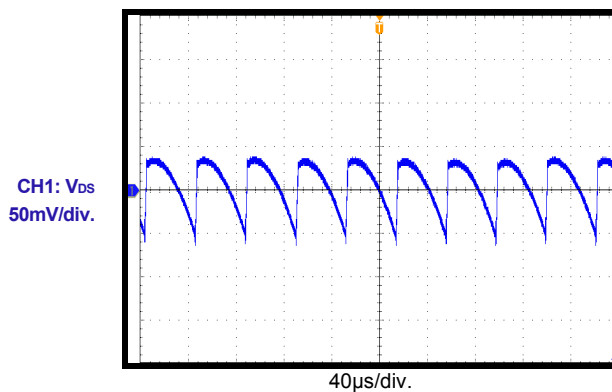
Open Loop Detection Recovery



OTP



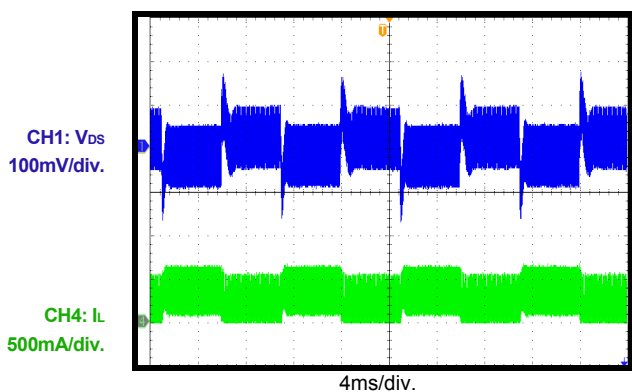
Output Ripple



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

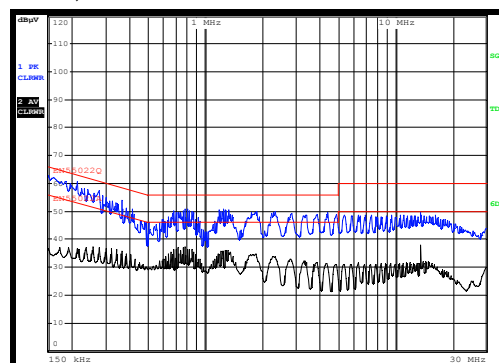
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Load Transient



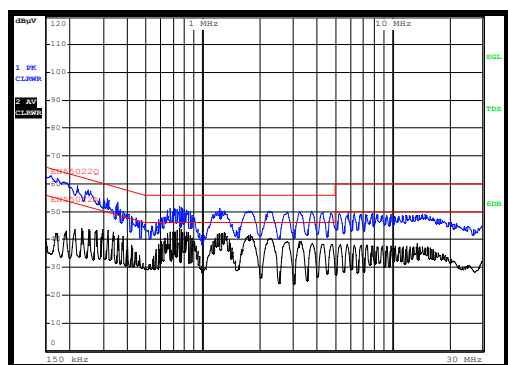
EMI Performance

L Line, $V_{IN}=230VAC$



EMI Performance

N Line, $V_{IN}=230VAC$



FUNCTIONAL BLOCK DIAGRAM

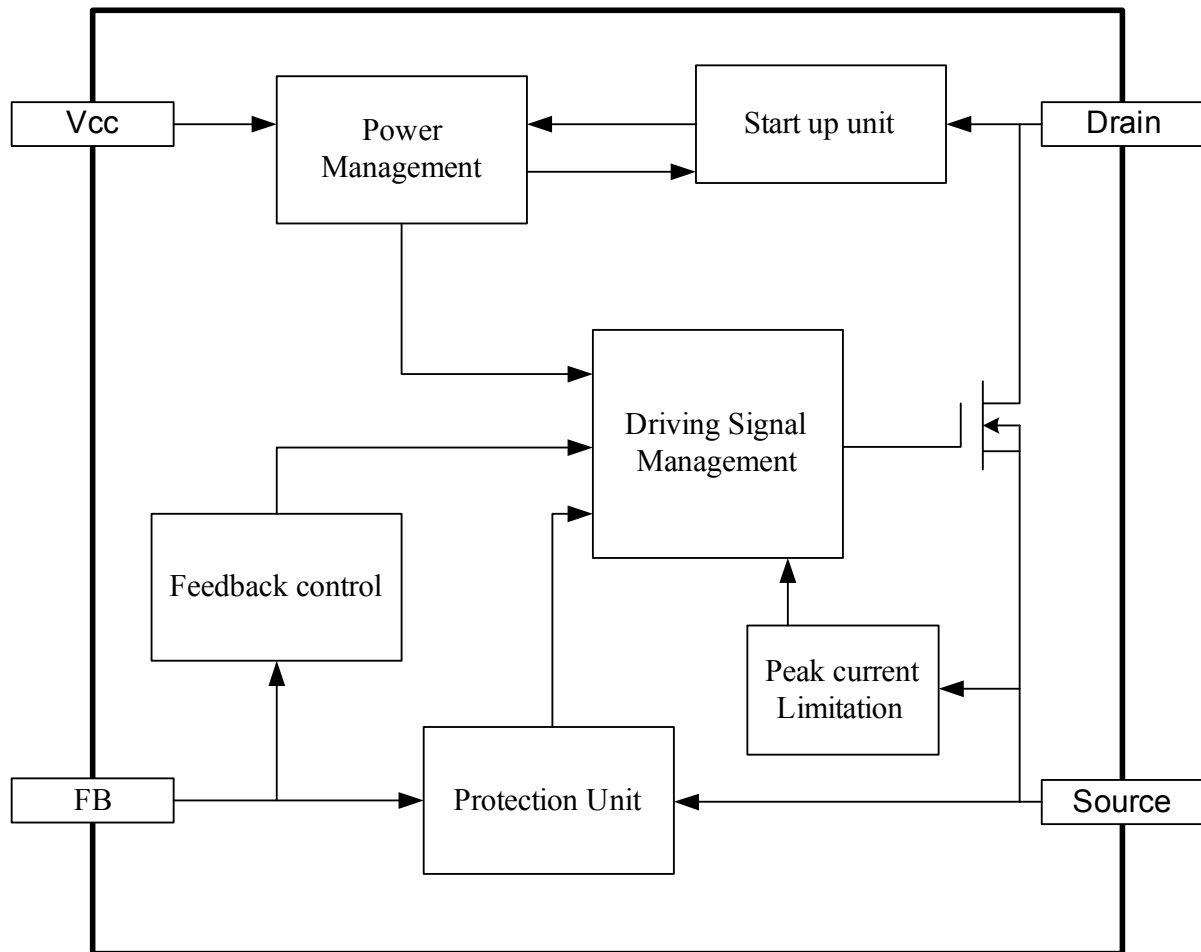


Figure 1: Functional Block Diagram

OPERATION

The MP174A is a green-mode-operation regulator: the peak current and the switching frequency both decrease with a decreasing load. As a result, it offers excellent light-load efficiency and improves average efficiency. The typical application diagram shows the regulator operates with a minimum number of external components.

Start-Up and Under-Voltage Lockout

The internal high-voltage regulator self-supplies the IC from the Drain pin. When VCC voltage reaches 5.6V, the IC starts switching, and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below 5.3V. A small capacitor (in the low μF range) can maintain the VCC voltage and lower the capacitor cost.

The IC stops switching when the VCC voltage drops below 3.4V.

Under fault conditions—such as OLP, SCP, and OTP—the IC stops switching and an internal current source ($\sim 16\mu\text{A}$) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until the VCC voltage drops below 2.4V. The restart time can be estimated using Equation (1):

$$\tau_{\text{restart}} = C_{\text{VCC}} \times \frac{V_{\text{CC}} - 2.4\text{V}}{16\mu\text{A}} + C_{\text{VCC}} \times \frac{5.6\text{V} - 2.4\text{V}}{4.1\text{mA}} \quad (1)$$

Soft Start

The IC stops operation when the VCC voltage drops below 3.4V, and it starts operation when VCC is charged to 5.6V. Every time the chip starts operation there is a soft-start period. The soft start prevents the inductor current from overshooting by limiting the minimum off time.

The MP174A adopts a 2 phase minimum off time limit soft start. Each soft-start phase retains 256 switching cycles. During soft start, the off time limit gradually shortens from $48\mu\text{s}$ to $24\mu\text{s}$, and finally to the $12\mu\text{s}$ normal operation off time limit (see Figure 2).

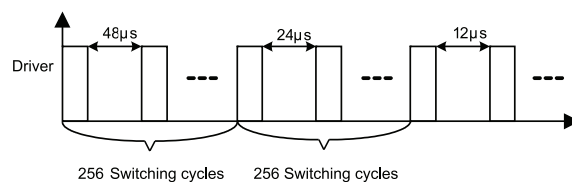


Figure 2: $\tau_{\text{Min_off}}$ at Start-Up

Constant Voltage Operation

The MP174A acts as a fully-integrated regulator when used in the buck topology (see the Typical Application on page 1).

It regulates the output voltage by monitoring the sampling capacitor.

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55V reference voltage, which indicates insufficient output voltage. The peak current limitation determines the ON period. After the ON period elapses, the integrated MOSFET turns off. The sampling capacitor (C3) voltage is charged to the output voltage when the freewheeling diode (D1) turns on. This allows the sampling capacitor (C3) to sample and hold the output voltage for the output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation under CCM in detail.

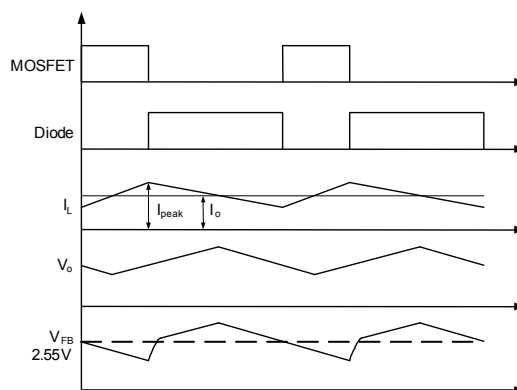


Figure 3: V_{FB} vs. V_{O}

Use Equation (2) to determine the output voltage:

$$V_o = 2.55V \times \frac{R1+R2}{R2} \quad (2)$$

Frequency Foldback and Peak Current Compression

The MP174A remains highly efficient under a light-load condition by reducing the switching frequency automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increases the MOSFET off time. Thus, the frequency decreases as the load decreases.

Determine the switching frequency with Equation (3) and Equation (4):

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}}, \text{ for CCM} \quad (3)$$

$$f_s = \frac{2(V_{in} - V_o)}{LI_{peak}^2} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM} \quad (4)$$

At the same time, the peak current limit decreases from 660mA as the off time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. As a result, peak-current compression helps further reduce no-load consumption. The peak current limit can be estimated with Equation (5). τ_{off} is the power module's off time.

$$I_{Peak} = 660mA - (4.8mA / \mu s) \times (\tau_{Off} - 12\mu s) \quad (5)$$

EA Compensation

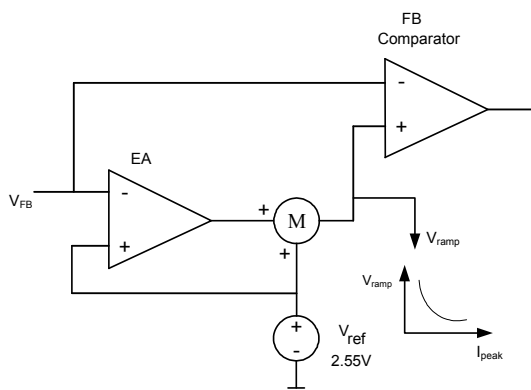


Figure 4: EA and Ramp Compensation

The MP174A has an internal error amplifier (EA) compensation loop. It samples the feedback

voltage 6 μ s after the MOSFET turns off and regulates the output based on the 2.55V reference voltage.

Ramp Compensation

An internal ramp compensation circuit improves the load regulation. There is an exponential voltage signal added to pull down the reference voltage of the feedback comparator (see Figure 4). The ramp compensation is a function of the load conditions: the compensation is 1mV/ μ s under full-load conditions; compensation increases exponentially as the peak current decreases.

Over-Load Protection (OLP)

The maximum output power of the MP174A is limited by the maximum switching frequency and peak current limit. If the load current is too large, the output voltage drops, so the FB voltage drops.

When the FB voltage drops below 1.7V it is considered an error flag and the timer starts. If the timer reaches 220ms ($f_s=28kHz$), OLP occurs. This timer duration avoids triggering OLP when the power supply starts up or the load transitions. The power supply should start up in less than 220ms ($f_s=28kHz$). The OLP delay time is calculated using Equation (6):

$$\tau_{Delay} \approx 220ms \times \frac{28kHz}{f_s} \quad (6)$$

Short-Circuit Protection (SCP)

The MP174A monitors the peak current and shuts down when the peak current rises above the SCP threshold through short-circuit protection. The power supply resumes operation with the removal of the fault. During soft start and the following 512 switching cycles, the SCP is blanked, in order to guarantee successful start-up with a large output capacitor.

Thermal Shutdown (OTP)

To prevent thermal induced damage, the MP174A stops switching when the junction temperature exceeds 150°C. During the thermal shutdown (OTP), the VCC capacitor is discharged to 2.4V, and the internal high-voltage regulator re-charges. The MP174A recovers when the junction temperature drops below 120°C.

Open-Loop Detection

If V_{FB} is less than 0.5V, the IC will stop switching and a re-start cycle will begin. During soft start and the following 512 switching cycles, the open-loop detection is blanked, in order to guarantee successful start-up with a large output capacitor.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to a turn-on spike. A turn-on spike is caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET. Figure 5 shows the leading-edge blanking.

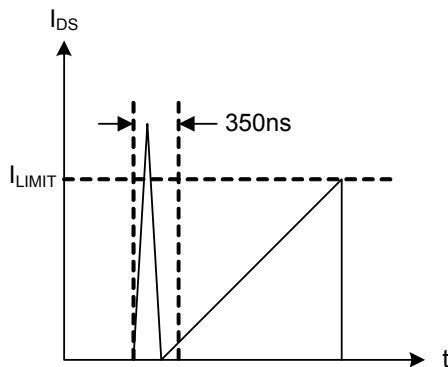
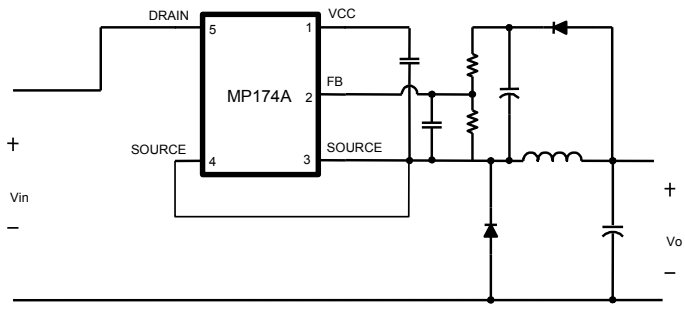
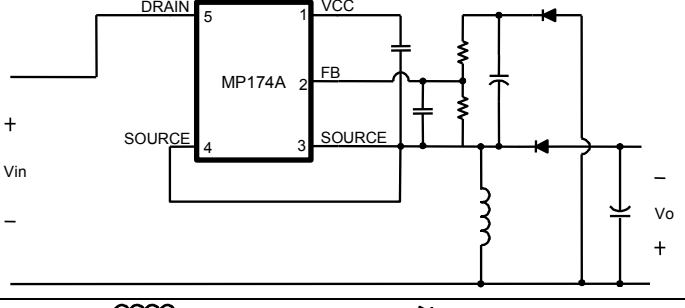
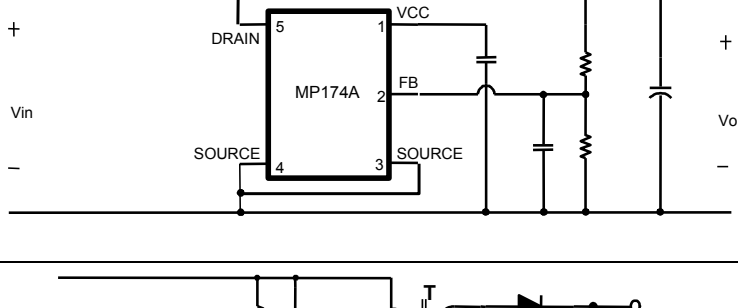
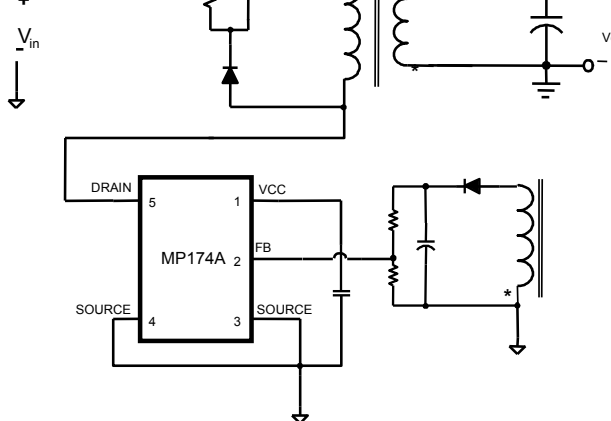


Figure 5: Leading-Edge Blanking

APPLICATION INFORMATION

Table 1: Common Topologies Using the MP174A

Topology	Circuit Schematic	Features
High-Side Buck		1. Non-isolation 2. Positive output 3. Low cost 4. Direct feedback
High-Side Buck-Boost		1. Non-isolation 2. Negative output 3. Low cost 4. Direct feedback
Boost		1. Non-isolation 2. Positive output 3. Low cost 4. Direct feedback
Flyback		1. Isolation 2. Positive output 3. Low cost 4. Indirect feedback

Topology Options

The MP174A can be used in common topologies, such as buck, buck-boost, boost, and flyback. See Table 1.

Component Selection

Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a half-wave rectifier and a full-wave rectifier.

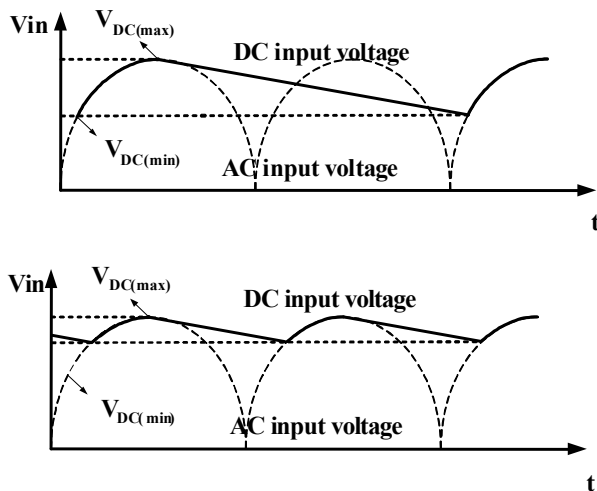


Figure 6: Input Voltage Waveform

Typically, the use of a half-wave rectifier requires an input capacitor rated at $3\mu\text{F}/\text{W}$ for the universal input condition. When using the full-wave rectifier, choose an input capacitor between $1.5\sim 2\mu\text{F}/\text{W}$ for a universal input condition. Avoid a minimum DC voltage below 70V; a low DC input voltage can cause thermal issues. A half-wave rectifier is recommended for $<2\text{W}$ output application, and a full-wave rectifier is recommended for $>2\text{W}$ output application.

Inductor

The MP174A has a minimum off time limit that determines the maximum power output. The maximum power increases as the inductor increases. Using a very small inductor may cause failure at full load, but a larger inductor means a higher OLP load. It is recommended to select an inductor with the minimum value that can supply the rated power. Estimate the maximum power with Equation (6) and Equation (7):

$$P_{O_max} = V_O(I_{Peak} - \frac{V_O \tau_{Min_off}}{2L}), \text{ for CCM} \quad (6)$$

$$P_{O_max} = \frac{1}{2} L I_{Peak}^2 \cdot \frac{1}{\tau_{Min_off}}, \text{ for DCM} \quad (7)$$

For mass production, tolerance on the parameters, such as peak current limitation and minimum off time, should be taken into consideration.

Figure 7 shows an example of a P_{Min} curve with a 12V output. $I_{Peak}=0.6\text{A}$ and $T_{Min_off}=15\mu\text{s}$ are used as the worst case for P_{Min} calculation.

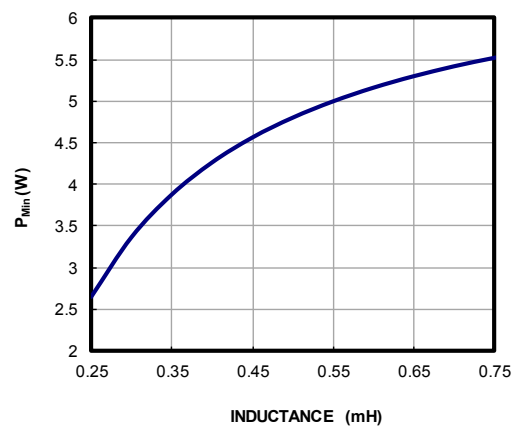


Figure 7: P_{Min} vs. L at 12V

For a 3.6W output converter (12V, 0.3A), the minimum inductor value is about 0.36mH. Using a 0.36mH causes the switching frequency to be too high, which causes poor efficiency. It is recommended to use an inductor that allows a switching frequency higher than 20kHz (but not too high in large output current applications).

To reduce costs, use a standard off-the-shelf inductor no less than the calculated value.

Freewheeling Diode

The diode should be selected based on the maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation for a CCM condition, so use an ultrafast diode, such as the EGC10JH.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple with Equation (8) and Equation (9):

$$V_{\text{CCM_ripple}} = \frac{\Delta i}{8f_s C_o} + \Delta i \cdot R_{\text{ESR}}, \text{ for CCM} \quad (8)$$

$$V_{\text{DCM_ripple}} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{\text{Peak}} - I_o}{I_{\text{Peak}}} \right)^2 + I_{\text{Peak}} \cdot R_{\text{ESR}}, \text{ for DCM} \quad (9)$$

It is recommended to use ceramic, tantalum, or low ESR electrolytic capacitors to reduce the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Appropriate R1 and R2 values should be chosen to maintain the V_{FB} at 2.55V. R2 is typically 5kΩ to 10kΩ. Avoid a large R2 value.

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor regulation at light loads, and large capacitors effect the circuit operation. Roughly estimate an optimal capacitor value using Equation (10):

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \leq C_{\text{FB}} \leq \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \quad (10)$$

Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. Normally a 3mA dummy load is needed and can be adjusted according to the regulated voltage. It is a compromise between small, no load consumption and good, no load regulation, especially for applications requiring a 30mW no load consumption. Use a Zener diode to reduce the no load consumption if no load regulation is not a concern.

Auxiliary VCC Supply

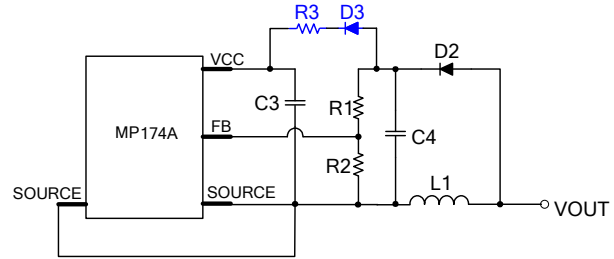


Figure 8: Auxiliary Vcc Supply Circuit

For V_o above 7V applications, the MP174A can achieve the 30mW no load power requirement. In order to do this, the chip requires an external VCC supply to reduce overall power consumption.

This auxiliary VCC supply is derived from the resistor connected between C3 and C4. C4 should be set larger than the recommendation above. D3 is used in case VCC interferes with FB. R3 is determined with Equation (11):

$$R3 \approx \frac{V_o - 5.8V}{I_s} \quad (11)$$

Where I_s is the VCC consumption under a no load condition. R3 should be adjusted to meet the actual I_s , because it varies in different applications. In a particular configuration, I_s is measured at about 250μA.

Surge Performance

An appropriate input capacitor value should be selected to obtain good surge performance. Figure 9 shows the half-wave rectifier. Table 2 shows the capacitance required under a normal condition for different surge voltages. FR1 is a 20Ω/2W fused resistor, and L1 is 1mH for this recommendation.

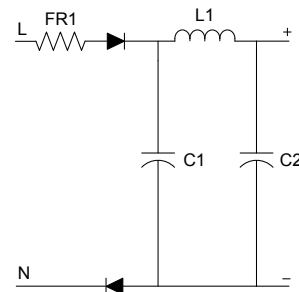


Figure 9: Half-Wave Rectifier

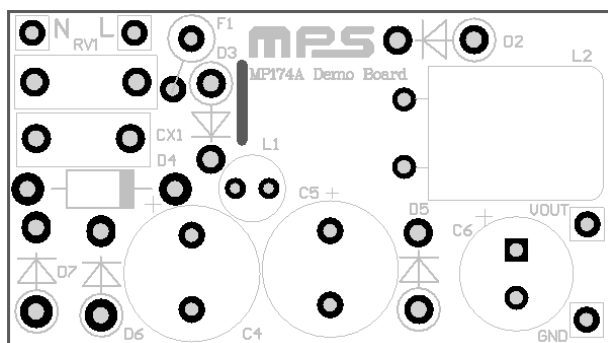
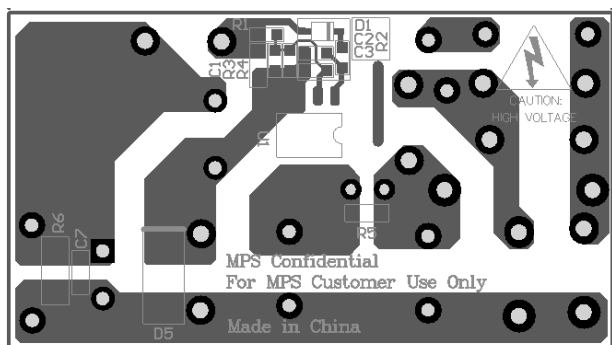
Table 2: Recommended Capacitance

Surge voltage	500V	1000V	2000V
C1	1 μ F	2.2 μ F	3.3 μ F
C2	1 μ F	2.2 μ F	3.3 μ F

Layout Guide

PCB layout is critical for reliable operation, good EMI, and thermal performance. Refer to Figure 10 and follow the guidelines below to optimize performance:

- 1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
- 2) Place the power inductor far away from the input filter while minimizing the loop area to the inductor.
- 3) Place a capacitor valued at several hundred pF between the FB pin and source as close to the IC as possible.
- 4) Connect the exposed pads or large copper area with the DRAIN pin to improve thermal performance.


Top

Bottom Layer
Figure 10: PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications below:

Table 3: Design Example

V _{IN}	85VAC to 265VAC
V _{OUT}	12V
I _{OUT}	300mA

The detailed application schematic is shown in Figure 11. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device application, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

Figure 11 shows a typical application example of a 12V, 300mA non-isolated power supply using the MP174A.

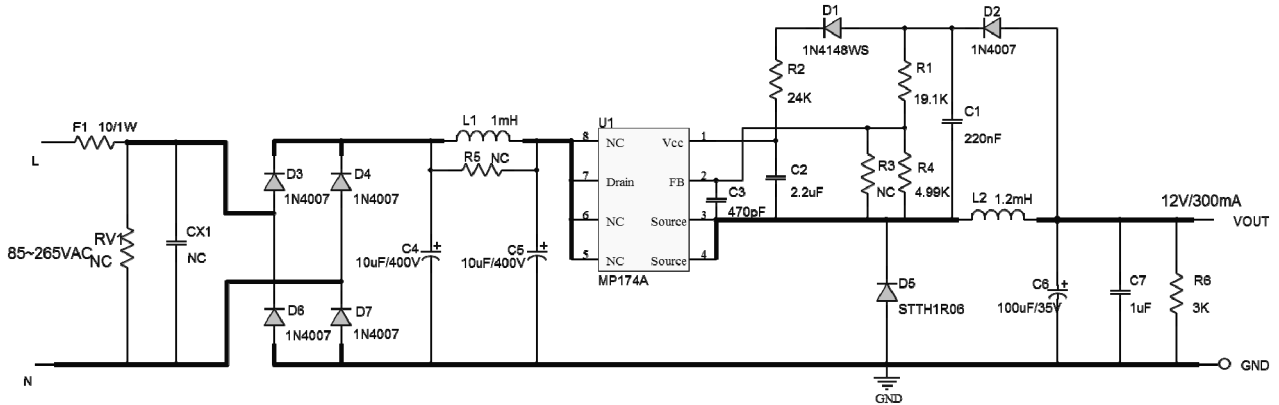
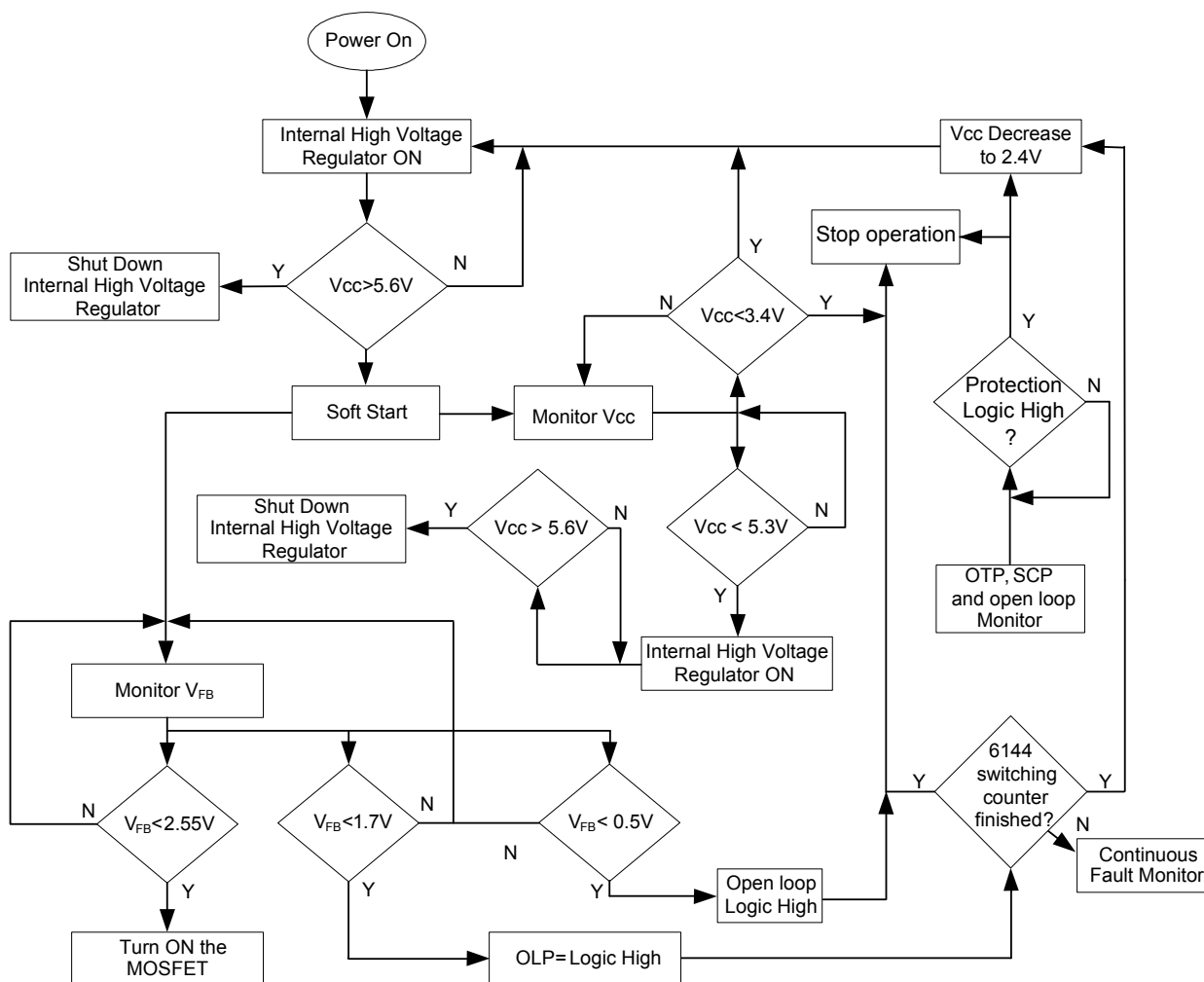


Figure 11: Typical Application at 12V, 300mA

FLOW CHART



UVLO, SCP, OLP, OTP and Open loop protections are auto restart

Figure 12: Control Flow Chart

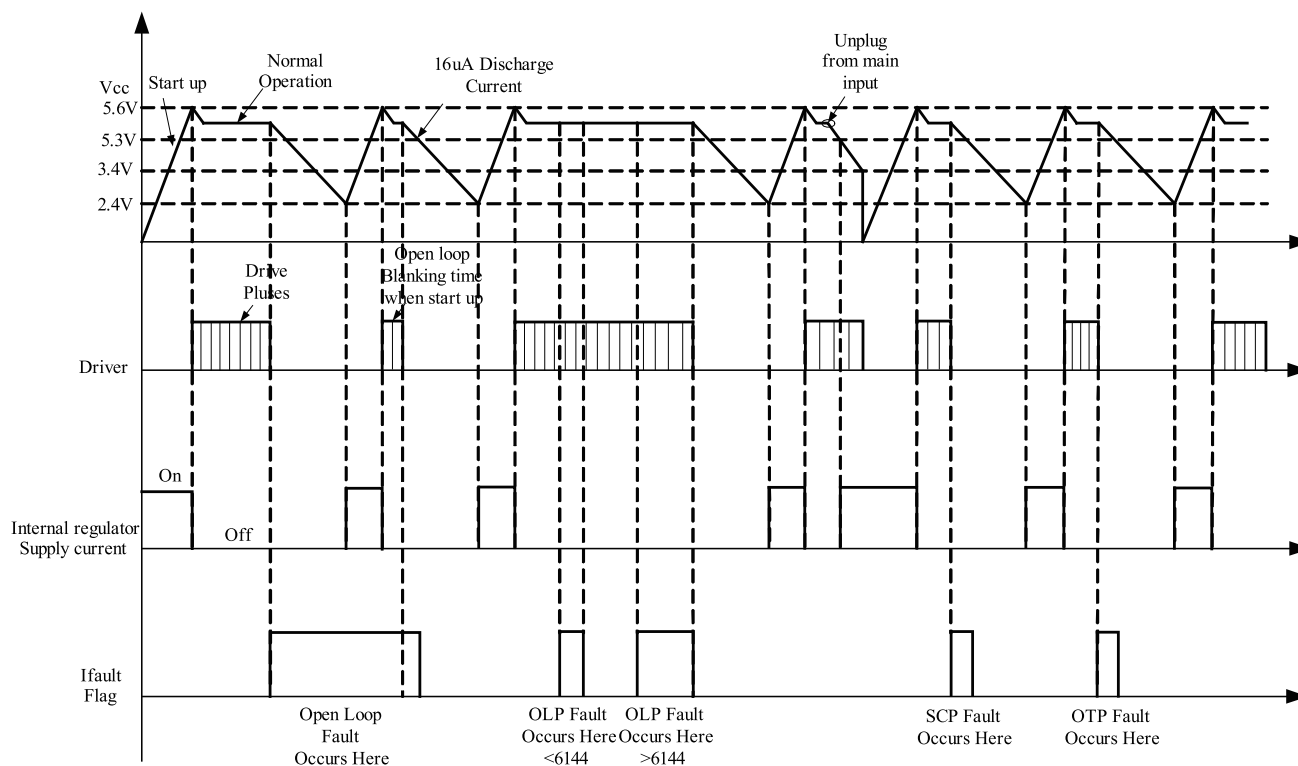
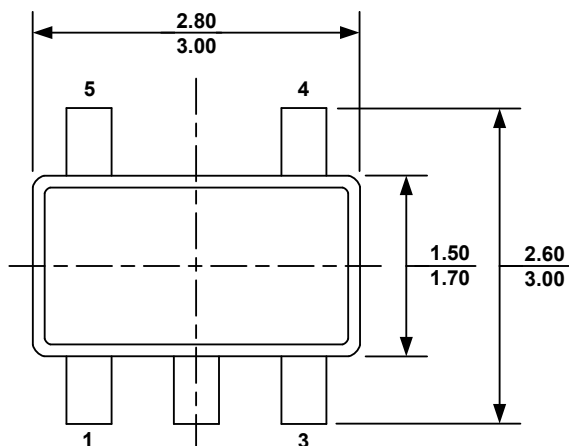


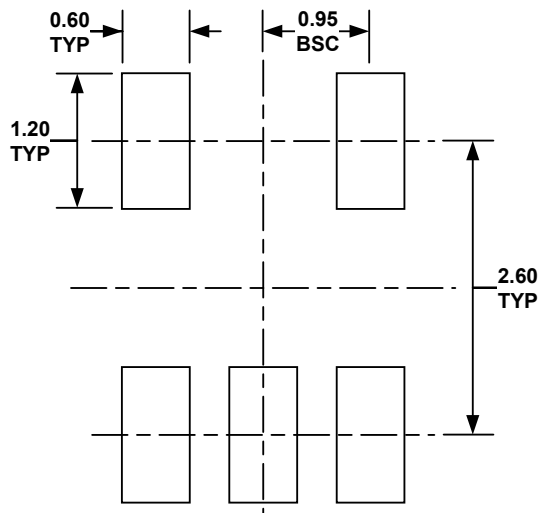
Figure 13: Signal Evolution in the Presence of a Fault

PACKAGE INFORMATION

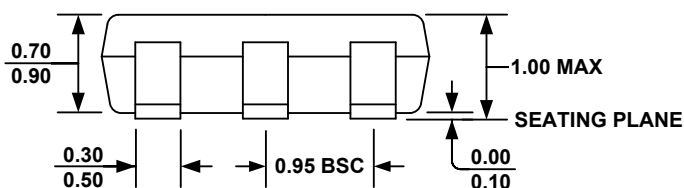
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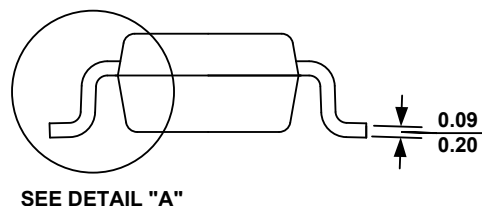
TOP VIEW



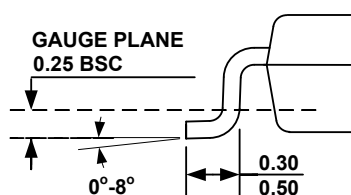
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



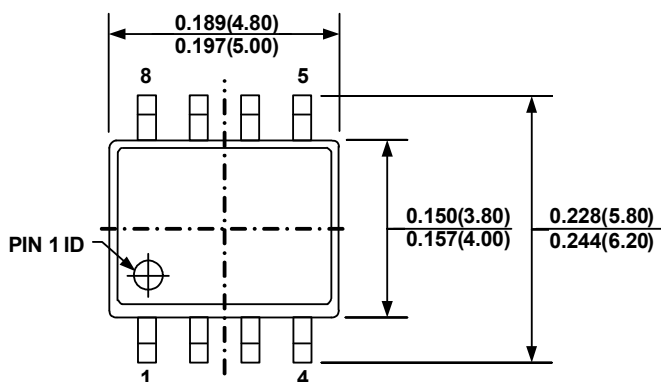
DETAIL "A"

NOTE:

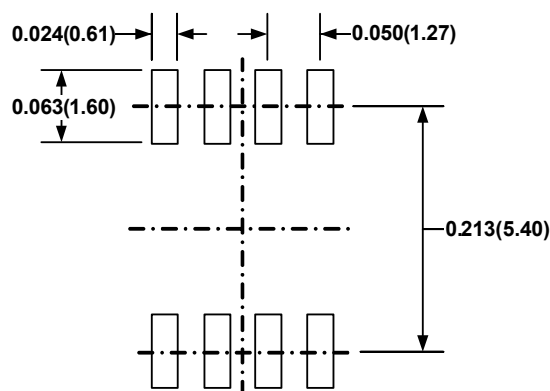
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

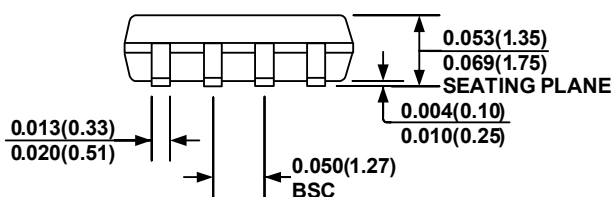
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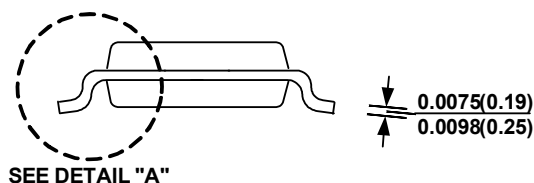
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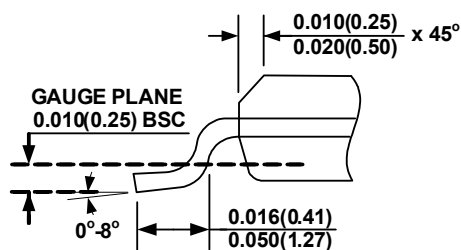
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES DIMENSION IN BRACKET IS IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS012, VARIATION AA
- 6) DRAWING IS NOT TO SCALE

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