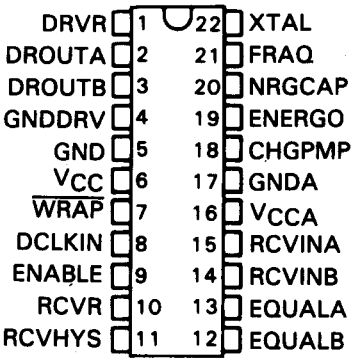
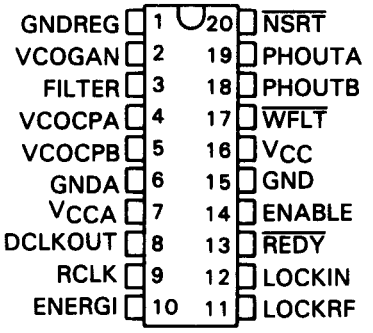
SEPTEMBER 1985 – REVISED MAY 1986

- Token Ring Electrical Connection
- Compatible with Electrical Interface of IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications
- Phase-Lock Loop for Clock Generation from Data Signal
- 4 Megabit per Second Differential Manchester-Encoded Data Rate
- Independent Transmit and Receive Channels
- Phantom Drive for Physical Insertion into Ring
- Cable Wire-Fault Indication
- Receive Data-Loss Detection
- Receiver Frequency Equalization and Low-Level Hysteresis Circuit
- Loop Back (Wrap Mode) for Self-Test Diagnostics
- Two Chip Set
  - —TMS38051 Ring Interface Transceiver (22 Pin)
  - —TMS38052 Ring Interface Controller (20 Pin)
- Single 5-V Supply
- Low-Power Schottky Technology

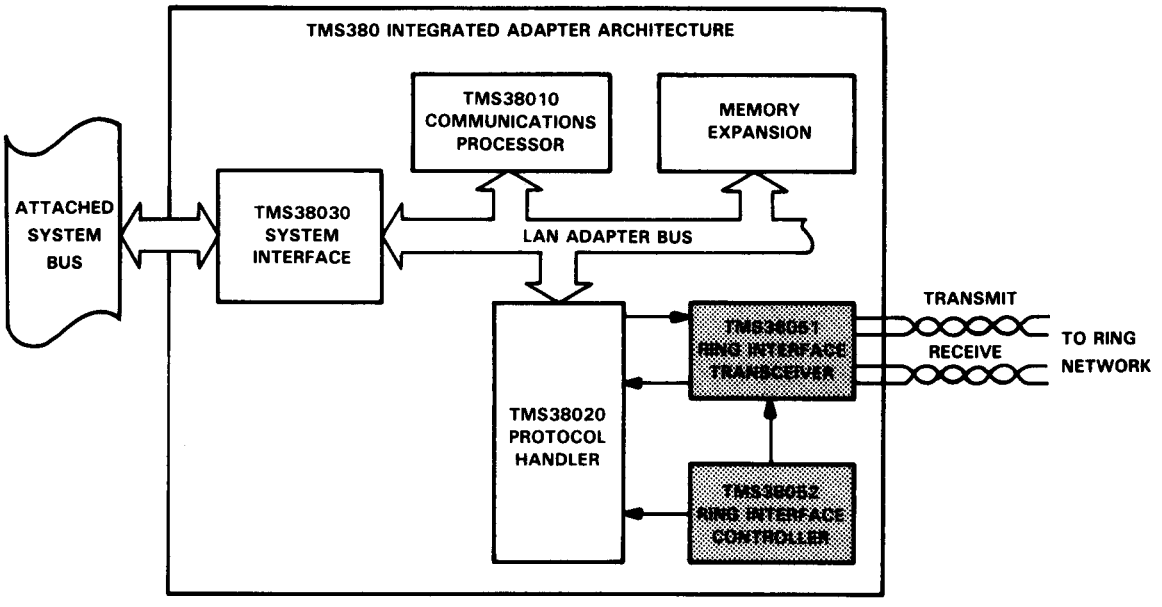
TMS38051 . . . N PACKAGE
(TOP VIEW)



TMS38052 . . . N PACKAGE
(TOP VIEW)



token ring LAN application diagram



A

pin descriptions

TMS38051

NAME	I/O	DESCRIPTION
RCVINA	I	Receiver Input A
RCVINB	I	Receiver Input B
EQUALA	I	Equalization/Gain Point A
EQUALB	I	Equalization/Gain Point B
RCVHYS	I	Receiver Hysteresis Resistor
RCVR	O	Receive Data
DRVR	I	Driver Data Input
DROUTA	O	Driver Output A
DROUTB	O	Driver Output B
CHGPMP	O	Charge-Pump Output
DCLKIN	I	Data-Latch Clock
NRGCAP	I	Energy-Detect Capacitor
ENERGO	O	Energy-Detect Output Signal to TMS38052
$\overline{\text{WRAP}}$	I	Internal Wrap-Mode Control
ENABLE	I	Output-Enable Control
FRAQ	I	Frequency Acquisition Control
XTAL	I	Crystal-Oscillator Input
V_{CC}		General 5-V Power
V_{CCA}		Analog 5-V Power
GND		General Ground
GNDDRV		Ground for Driver Output
GNDA		Analog Ground

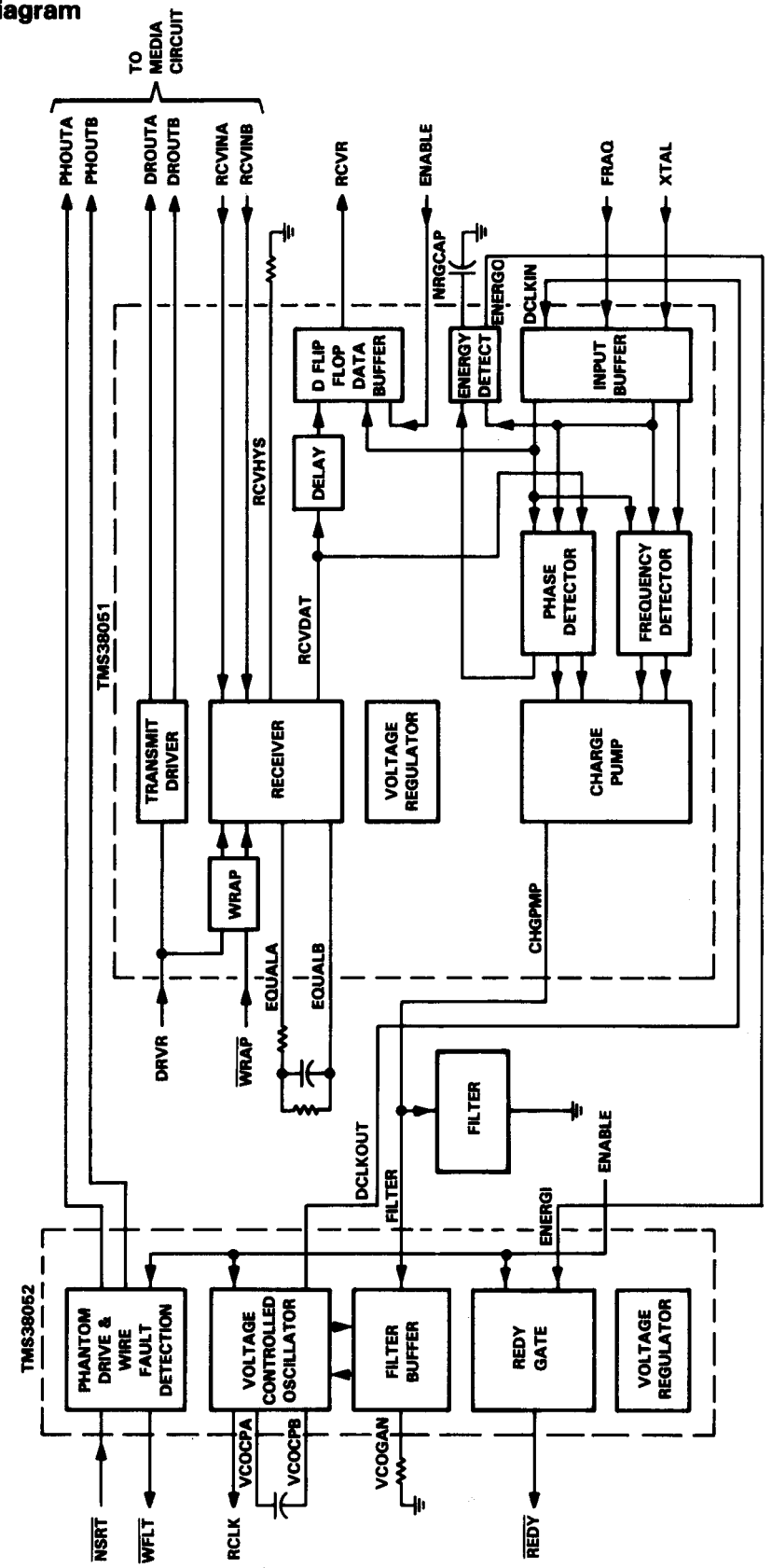
TMS38052

NAME	I/O	DESCRIPTION
$\overline{\text{NSRT}}$	I	Phantom-Driver Control
PHOUTA	O	Phantom-Driver Output A
PHOUTB	O	Phantom-Driver Output B
$\overline{\text{WFLT}}$	O	Wire-Fault Indicator
FILTER	I	Filter-Buffer Input
VCOGAN	I	VCO-Gain Resistor
VCOCPA	I	VCO Timing Capacitor Pin A
VCOCPB	I	VCO Timing Capacitor Pin B
RCLK	O	Recovered Clock
DCLKOUT	O	Data-Latch Clock
LOCKIN	I	Reserved, must be tied to ground.
LOCKRF	I	Reserved, must be tied to ground.
ENERGI	I	Energy-Detect Input Signal
$\overline{\text{REDY}}$	O	Ready Signal
ENABLE	I	Output-Enable Control
V_{CC}		General 5-V Power
V_{CCA}		Analog 5-V Power
GND		General Ground
GNDREG		Ground for Voltage Regulator
GNDA		Analog Ground

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



A

description

The TMS38051 Ring Interface Transceiver and the TMS38052 Ring Interface Controller combine with passive components (Figure 1) to form a full duplex electrical interface compatible with IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications. A 4 megabit per second Differential-Manchester-encoded data stream is received by the TMS38051 Ring Interface Transceiver and phase aligned using an on-chip phase-lock loop. Both the recovered clock and data are passed to the TMS38020 Protocol Handler for serial-to-parallel conversion. On transmit, the TMS38020 Protocol Handler provides the TMS38051 a TTL-level signal which is converted to the appropriate levels for transmission on the wiring media.

The TMS38052 contains the Voltage-Controlled Oscillator (VCO) for the Phase-Lock Loop (PLL), the phantom drive for control of relays contained within a Trunk-Coupling Unit (TCU), and error detection for wire faults in the cable connected to the TCU.

The TMS38051 and TMS38052, when coupled with the TMS38010 Communications Processor, the TMS38020 Protocol Handler, and the TMS38030 System Interface, form a highly integrated Token Ring LAN Adapter compatible with IEEE Std 802.5-1985 Token Access Method and Physical Layer Specifications.

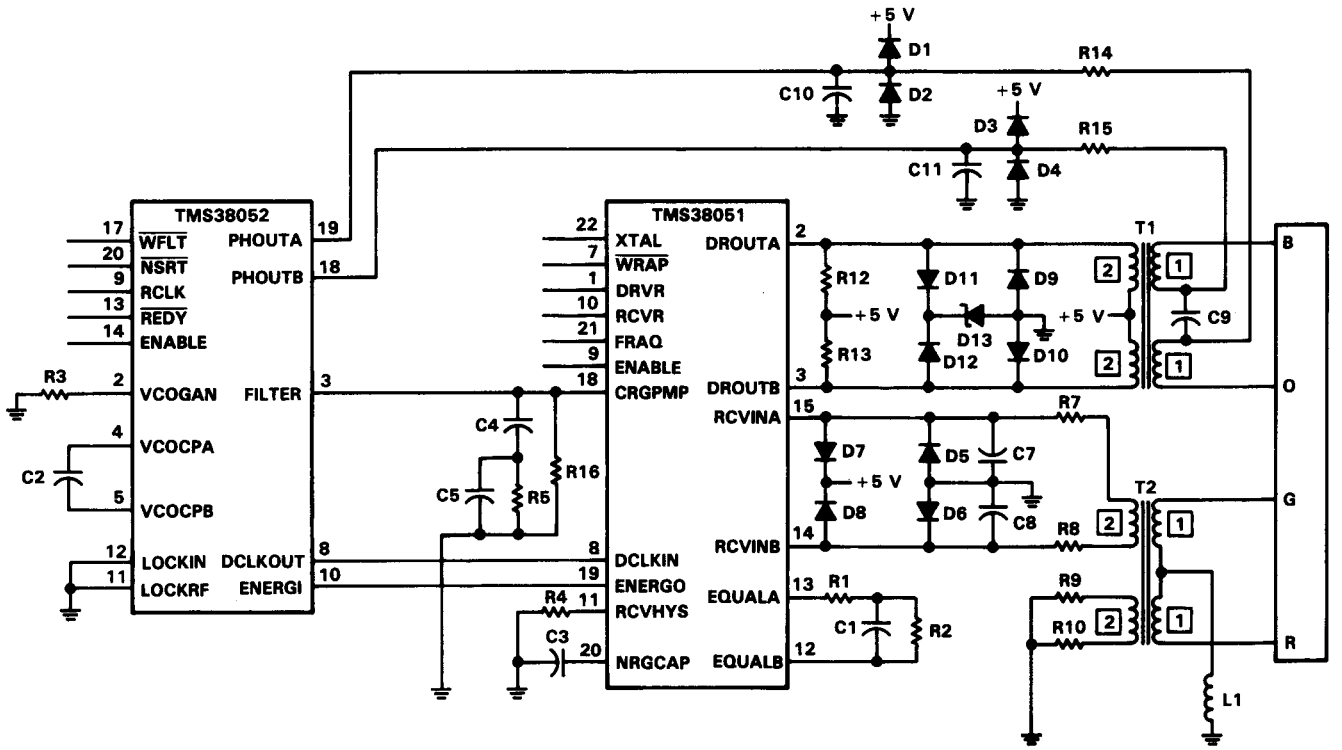


FIGURE 1. TOKEN RING INTERFACE CIRCUIT

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TABLE 1. TYPICAL COMPONENT VALUES FOR FIGURE 1

SYMBOL(S)	VALUE/TYPE	FUNCTION	SYMBOL(S)	VALUE/TYPE	FUNCTION
C1	180 pF 5%	Equalizer	L1	56 μH 10%	Phantom Return
C2	200 pF 5%	VCO	R1	121 Ω 1%	Equalizer
C3	6800 pF 10%	Energy Detect	R2	604 Ω 1%	Equalizer
C4	8.2 μF 10%	PLL Filter	R3, R4	2.49 kΩ 1%	VCO and Hysteresis
C5	680 pF 10%	PLL Filter	R5	825 Ω 1%	PLL
C7, C8	62 pF 5%	Filter	R7, R8	121 Ω 1%	Receive Filter
C9	0.1 μF 10%	Wire Fault Isolation	R9, R10	75 Ω 1%	Impedance Match
C10, C11	8.2 μF 20%	Phantom Drive Noise Isolation	R12, R13	300 Ω 5%	Transmit Termination
D1-D4	1N4004	Phantom Surge Suppression	R14, R15	50 Ω 5%	Phantom Drive
D5-D8	1N4148	Receiver Surge Suppression	R16	330 kΩ 5%	Jitter Compensation
D9-D12	1N4148	Driver Surge Suppression	T1, T2	TNI2837	Transformer
D13	1N5347B	Driver Surge Suppression		or	
				PE63838-001	

architecture

The major functional blocks of the TMS38051 Ring Interface Transceiver are the receiver, data buffer, transmit driver, wrap function, voltage regulator, phase and frequency detectors, charge pump, and energy detector.

The major blocks of the TMS38052 Ring Interface Controller are the phantom drive, wire-fault detector, voltage-controlled oscillator (VCO), VCO-filter buffer, and voltage regulator.

These blocks are described in the paragraphs that follow.

receiver function

The receiver circuit provides DC bias for the differential input (RCVINA and RCVINB), clamping of large signal swings, amplification, equalization, definition of thresholds and hysteresis for data detection. Gain (and consequently input threshold values) is set by the equalizer impedance. Equalization characteristics are determined by the external equalization resistors (R1 and R2) and the equalization capacitor (C1). Hysteresis is set by the hysteresis resistor (R4). The circuit is suitable for Differential-Manchester-encoded data up to four megabits per second. In the internal-wrap mode, provided for self test of the chip, the normal input path is disabled by removing the bias voltage from the input circuit and enabling the wrap path. The wrap function is enabled by pulling $\overline{\text{WRAP}}$ active-low. Receiver gain, thresholds, equalization and hysteresis are unchanged in the internal-wrap mode.

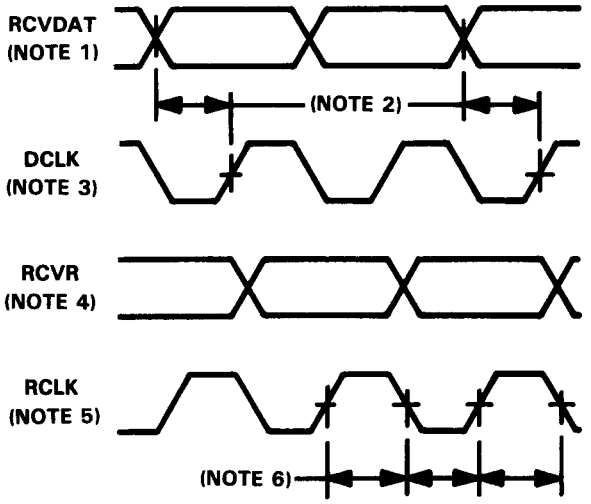
Each of the differential inputs, RCVINA and RCVINB, are independently biased to half the supply voltage and have a series resistor, nominal value 1 kΩ internally. Large transients are clamped by two external diode strings, each of two diodes series connected back to back (see Figure 1). The low frequency gain is set by the sum of the two equalization resistors, R1 + R2, connected from pin EQUALA to pin EQUALB in the emitter circuit of the differential input stage. High-frequency gain is set by resistor R1 because R2 is bypassed by the equalization capacitor C1. The frequency at which equalization becomes effective is determined by the values of R1 and C1. Hysteresis is set by external resistor R4 connected from pin RCVHYS to ground. Equalization is effective at low signal amplitudes. At larger signal levels, nonlinear effects reduce the effective equalization. The signal level where saturation occurs is determined by the impedance between EQUALA and EQUALB.

A

data buffer

The output of the receiver (the internal TMS38051 signal named RCVDAT) drives two internal circuits: a D-type flip-flop data buffer clocked by the VCO (DCLKIN) to sample the received data at the optimum time to generate the signal RCVR, and the phase detector used to control the VCO. RCVR is the retimed received data signal sent to the TMS38020 Protocol Handler for decoding of the Differential-Manchester-encoded data. RCLK is the clock used by the TMS38020 to sample RCVR. Logic state changes at RCVR occur at the rising edges of DCLK. Data is stable and may be sampled at the rising edges of RCLK. Data is delayed by the propagation delay of the receiver and data buffer plus one-half of an 8 MHz clock period from the receiver inputs to pin RCVR. The relative timing of these signals is indicated in Figure 2.

Static-timing offset is defined as the delay from a rising data transition (internally at RCVDAT) to the time data is sampled (rising transition at DCLKIN after buffering), minus 62.5 ns. At 4 megabits per second (8 MHz clock), an offset of zero is optimum sampling as this places the rising edge of the sampling clock in the middle of the data pulse. A positive offset represents late sampling.



NOTES: 1. Output of the receiver (internal signal derived from RCVIN pins)
2. PLL Static timing offset plus 62.5 ns
3. VCO clock to detectors and D-type flip-flop
4. Output of data buffer D-type flip-flop
5. Inverted clock to sample RCVR
6. Half clock period delays caused by internal latching.

FIGURE 2. RECEIVE DATA TIMING

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

transmit driver

The transmit driver provides differential current drive at a suitable level for driving the ring. Both outputs (DROUTA and DROUTB) are open collector, intended to drive a center-tapped transformer, with the center tap connected to V_{CC}. The output stage steers a fixed current between the two outputs, under the control of the driver data input (DRVR), with as little skew as possible. Transmitted data is not retimed within the TMS38051. Consequently, low skew in the transmitter is important in order to avoid degrading the waveform. The transmitter-drive outputs are not affected by the ENABLE signal. The driver data input (DRVR), when high, directs the output current to driver output DROUTA and, when low, to output DROUTB.

wrap function

The wrap function is designed to provide a signal path used for system self-test diagnostics. When the internal wrap-mode control input ($\overline{\text{WRAP}}$) is taken low, the transmitter outputs are disabled and the receiver inputs are ignored. An attenuating path is provided from the transmitter output circuitry to the receiver input circuitry through the wrap circuit. There is then a signal path from the transmitter input DRVR back to the data buffer output RCVR. The path to RCVR is inverting with an added delay of an 8 MHz one-half clock period. In the internal-wrap mode, attenuation can be checked by observing the signal amplitude at the equalization pins EQUALA and EQUALB. Equalization will be active at this signal level although the signal will not exhibit the high-frequency attenuation effects for which equalization is intended to compensate.

phantom driver and wire-fault detector

The phantom-drive circuit under control of the $\overline{\text{NSRT}}$ input generates a dc signal on both of the two drive outputs, PHOUTA and PHOUTB. This signal is sent over the transmit-signal wire pair to the Trunk-Coupling Unit (TCU) to request that the station be inserted into the ring. The signal current is detected at the TCU causing the external-wrap path from the transmitter outputs back to the receiver inputs to be broken, the ring to be broken, and a connection to be made from the ring to the receiver inputs and from the transmitter outputs to the ring. The phantom-drive outputs are short circuit protected and will detect a short circuit from either output to ground or an abnormally low load current at either output corresponding to an open circuit in the signal or TCU wiring. Either type of fault results in the wire-fault indicator output ($\overline{\text{WFLT}}$) to be driven low. The logic state of $\overline{\text{WFLT}}$ will go high when $\overline{\text{NSRT}}$ is high. All three outputs, PHOUTA, PHOUTB and $\overline{\text{WFLT}}$, are in a high-impedance state when the output-enable control (ENABLE) is low.

voltage regulator

The internal voltage regulator is used to make the performance of both the TMS38051 and TMS38052 less dependent on the supply voltage. The regulator consists of a "band gap" reference, scaled up to a nominal 3.9 V, with a temperature coefficient designed to compensate for coefficients in circuits referenced to the voltage regulator.

phase-lock loop

The TMS38051 and TMS38052 together implement a phase-lock loop (PLL) for recovering a data clock from the received bit stream. The elements of the phase-lock loop are: phase and frequency detectors, a charge pump, an external filter, a filter buffer and a voltage-controlled oscillator. Figure 3 illustrates these blocks and their partition between the TMS38051 and TMS38052. The following paragraphs describe the PLL elements.

A

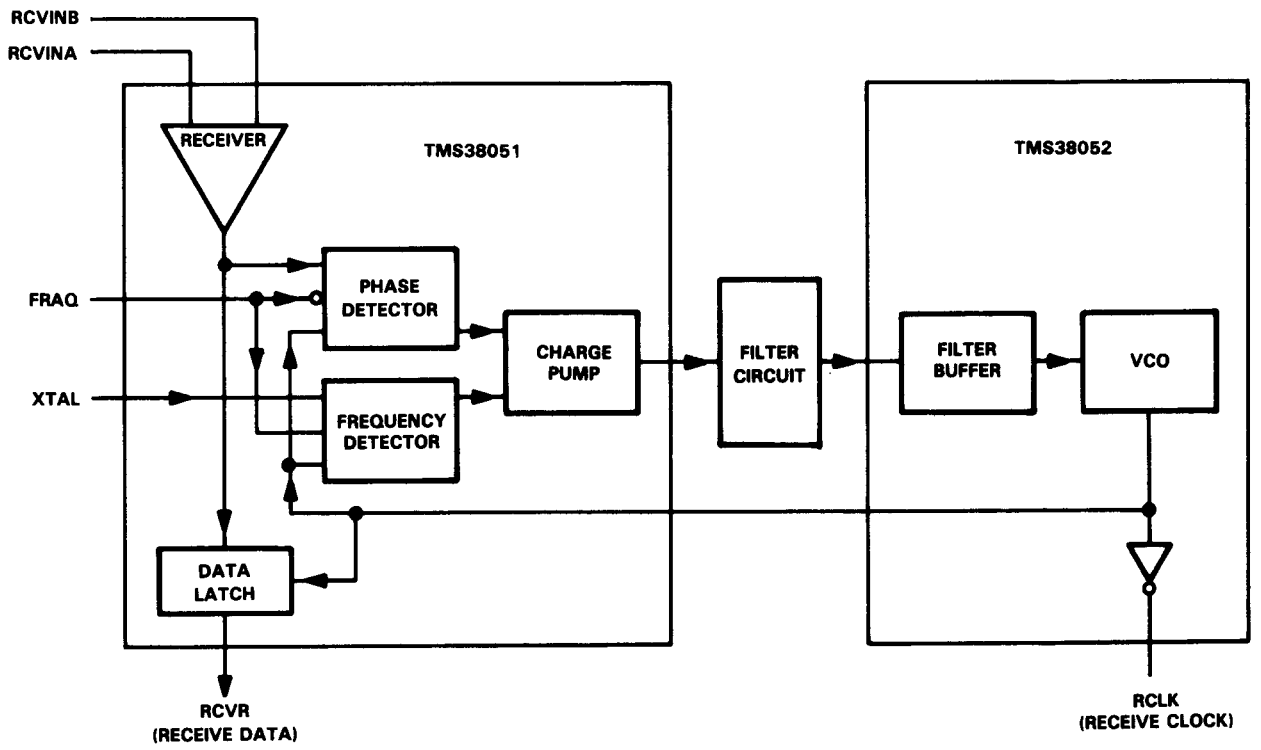


FIGURE 3. PHASE LOCK LOOP

phase and frequency detectors

The phase and frequency detectors are blocks of logic that generate control signals suitable for controlling the charge pump. The frequency detector will cause the voltage-controlled oscillator (VCO) frequency to be the same as the crystal-oscillator input, XTAL. The phase detector provides more accurate phase discrimination but could indicate a false lock where one frequency is a multiple of the other.

A multiplexer selects the required detection mode during insertion into the ring. The frequency-detection mode is selected by taking FRAQ high and the phase-detection mode is selected by taking FRAQ low. The phase or frequency detectors supply the necessary "charge" and "discharge" control signals to the charge pump. All gates not required for normal operation in either mode are prevented from switching to minimize the noise that might be coupled into the PLL.

charge pump

The output of either the phase detector or frequency detector drives the charge pump as selected by the FRAQ input. The charge pump drives the external filter (passive components R5, C4, and C5) and the filter-buffer input (FILTER). The charge pump has the ability to supply charge ("up" current into the filter) and to remove charge ("down" current out of the filter into the charge pump). A small amount of charge is required to provide the filter-buffer input current and any leakage in the external filter. Additional net charge affects the filter voltage. If the up current exceeds the down current, the voltage on the filter will increase, increasing the "controlled voltage" and the frequency of the VCO. The charge pump has two inputs so there are four possible states for the charge pump.

1. Pump up—current into the filter increasing the voltage.
2. Pump down—current out of the filter reducing the voltage.
3. No pump—high-impedance state, holding the voltage on the filter.
4. Pump up and pump down—both currents on, not allowed by the detector logic.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

The charge-pump block has two constant current circuits operating continuously, one for pump up and one for pump down. They are designed to be stable and equal under all operating conditions. Charge-pump circuitry determines which, if either, of the two currents is connected to pin FILTER and the external PLL filter. The magnitude of the charge-pump currents affects the loop gain and damping which affects static-timing offset. Leakage in the "no pump" state affects jitter.

external filter

The external filter consists of three external components, two capacitors (C4 and C5) and one resistor (R5) connected from the FILTER pin to ground.

filter buffer

The filter-buffer amplifier is designed to present a high impedance to the filter and to convert the filter voltage into two equal currents, proportional to the filter voltage, for use in the voltage-controlled oscillator. The current level or constant of proportionality is set by the external resistor (R3) to ground connected at pin VCOGAN. This constant is critical to loop gain and damping. The filter voltage range over which the current level tracks the voltage determines the pull-in range of the VCO. The bandwidth must be adequate to ensure that the filter-buffer amplifier has no significant effect on the loop characteristics.

voltage-controlled oscillator

The voltage-controlled oscillator (VCO) is an emitter-coupled astable multivibrator. The frequency is set by internal circuit parameters, the currents from the filter buffer (set by the filter voltage and resistor R3 from the VCOGAN pin to ground), and the VCO timing capacitor C2 connected between the VCOCPA and VCOCPB pins. Symmetrical circuit design helps ensure symmetrical waveforms. The VCO is buffered and converted to TTL-signal levels at the DCLKOUT pin. DCLKOUT is used to drive the frequency and phase detectors, clock the data buffer D-type flip-flop, and after an extra inversion at pin RCLK, is passed on to the TMS38020 Protocol Handler for processing of the received data.

energy detect

The energy detect circuit distinguishes between potentially valid data at the receiver input and a quiet condition (or absence of data). Normally, the data transitions occur between a rate of 2 MHz and 4 MHz. Each rising data transition results in a current pulse into the integrating capacitor C3 connected at the NRGCAP pin. The energy detector is reset (the capacitor is discharged) whenever the input FRAQ is switched in either direction.

The value of the capacitor (C3) determines how rapidly a change in signal condition will be reflected in a change in $\overline{\text{REDY}}$. A value of capacitance too small results in $\overline{\text{REDY}}$ being asserted before the PLL has obtained frequency lock (approximately 2 μs worst case). A large value of capacitance reduces $\overline{\text{REDY}}$ response time. Based upon system ring verification, a value of 6800 pF (10%) has been selected.

Although an energy detect capacitor (C3) value is chosen to be 6800 pF, the energy detect circuit is tested with a capacitor value of 1000 pF. The following signal conditions are met by the energy detect circuit for C3 = 1000:

1. ENERGO will remain asserted if there are at least 24 rising transitions in a 16 μs interval. This transition rate allows a dropped baud every 2 μs for a minimum transition pattern of all "1's."
2. ENERGO will remain de-asserted if there are less than 3 rising transitions in a 16 μs interval.
3. In a transition from no signal (less than 3 rising transitions in 16 μs) to signal (at least 24 rising transitions in a 16 μs interval) ENERGO transition time ($\overline{\text{REDY}}$ asserted) is 0.75 μs minimum to 100 μs maximum.

A

4. In a transition from signal (at least 24 rising transitions in a 16 μs interval) to no signal (less than 3 rising transitions in 16 μs), the ENERGO transition time to a de-asserted state ($\overline{\text{REDY}}$ de-asserted) is 16 μs.

Note that for proper operation of the $\overline{\text{REDY}}$ output, the LOCKIN and LOCKRF pins must be tied together and grounded such that no more than ± 2 mV of differential signal occurs between these two pins.

test mode

The TMS38051 and TMS38052 feature a test mode for board-level testing with the components in circuit. This facilitates testing by board-of-nails testers. This test mode is enabled by tying the ENABLE pin to ground. This has the effect of driving all the TTL outputs and the phantom-drive outputs to a high-impedance state. The media-driver outputs (DROUTA and DROUTB) are not affected by this function. When the ENABLE pin is high, the TMS38051 and TMS38052 operate normally. When this pin is low, the circuit will continue to operate except that pins PHOUTA, PHOUTB, RCVR, $\overline{\text{WFLT}}$, RCLK and DCLKOUT are driven to the high-impedance state, and pin $\overline{\text{REDY}}$ is driven to the high state. Pin ENERGO is not affected by ENABLE.

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range V_{CC} . . . . . −0.5 V to 7 V
Input voltage range (Note 7) . . . . . −0.5 V to 7 V
Output voltage range: Driver outputs . . . . . −0.5 V to 11 V
All other outputs (Note 8) . . . . . −0.5 V to 7 V
Power dissipation (Note 9) . . . . . 0.8 W
Operating free-air temperature range (Note 10) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 7. Inputs may be taken to more negative voltages if the current is limited to 20 mA.
8. These outputs may not be taken more than 0.5 V above the V_{CC} pins.
9. Maximum power dissipation per package.
10. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperature should be maintained at or below 80°C for the TMS38051 and 75°C for the TMS38052.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage	DRVR, $\overline{WRAP}$, ENABLE, DCLKIN, FRAQ, XTAL, ENERGI, $\overline{INSRT}$		2			V
V_{IL}	Low-level input voltage	DRVR, $\overline{WRAP}$, ENABLE, DCLKIN, FRAQ, XTAL, ENERGI, $\overline{NSRT}$				0.8	V
	Receiver input bias voltage (Note 11)			0.5 V_{CC}−1		0.5 V_{CC}+1	V
I_{OH}	High-level output current	RCVR, $\overline{WFLT}$, RCLK, DCLKOUT				−0.4	mA
		ENERGO, $\overline{REDY}$				−0.1	mA
I_{OL}	Low-level output current	V_{OL} <0.5 V	RCVR, $\overline{WFLT}$, RCLK, DCLKOUT, $\overline{REDY}$			4	mA
		V_{OL} <0.4 V				1	mA
		V_{OL} <0.5 V	ENERGO			0.5	mA
T_A	Operating free-air temperature (Note 10)			0		70	°C

†"Recommended Operating Conditions" indicate the conditions that must be met to ensure that the device will function as intended and meet the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device ground pins. Currents into the device are considered to be positive.

NOTES: 10. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperature should be maintained at or below 80°C for the TMS38051 and 75°C for the TMS38052.
11. Input bias voltage must be between 0.5 V_{CC} − 1 V and 0.5 V_{CC} + 1 V, or the self-generated bias may be used.

A

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

TTL input

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI, $\overline{NSRT}$, DCLKIN, FILTER	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI, $\overline{NSRT}$, DCLKIN, FILTER	V_I = 0.4 V			−0.4	mA
V_{IK}	Input clamp voltage	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI $\overline{NSRT}$, DCLKIN, FILTER	I_I = −12 mA			−1.5	V
I_I	Input current at maximum input voltage	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$ DCLKIN, FILTER	V_I = 7 V			100	μA
		ENERGI	V_I = 5.5 V			100	μA

TTL output

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{WFLT}$, DCLKOUT	I_{OH} = −0.4 mA	2.5			V
		RCVR, RCLK	I_{OH} = −0.4 mA	2.8			V
		ENERGO, $\overline{REDY}$	I_{OH} = −0.1 mA	2.5			V
V_{OL}	Low-level output voltage	RVCR, $\overline{WFLT}$, RCLK, DCLKOUT, $\overline{REDY}$	I_{OL} = 4 mA			0.5	V
			I_{OL} = 1 mA			0.4	V
		ENERGO	I_{OL} = 0.5 mA			0.5	V
I_{OZH}	Off-state output current with high-level voltage applied	RCVR, $\overline{WFLT}$ RCLK, DCLKOUT	V_O = 2.7 V			100	μA
		$\overline{REDY}$				−1.5	mA
I_{OZL}	Off-state output current with low-level voltage applied	RCVR, $\overline{WFLT}$ RCLK	V_O = 0.4 V			−100	μA
		DCLKOUT		100		−600	μA
		$\overline{REDY}$				−1.5	mA
I_{OS}	Short-circuit output current	RCVR, $\overline{WFLT}$, RCLK, DCLKOUT	V_O = 0	−20		−100	mA
		ENERGO, $\overline{REDY}$		−0.5		−2	mA

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

receiver input

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rising input threshold voltage, V_{T+}		RCVINA, RCVINB	V_{IC} = V_{SB}, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 12, 13, and 14			20	mV
Falling input threshold voltage, V_{T-}			V_{IC} = V_{SB}, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 12, 13, and 14			−20	mV
Noise threshold voltage $\lvert V_{T+} - V_{T-} \rvert$			V_{IC} = V_{SB}, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 12, 13, and 14	10			mV
Asymmetry threshold voltage $\lvert V_{T+} + V_{T-} \rvert$			V_{IC} = V_{SB}, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 12, 13, and 14			14	mV
Common mode rejection voltage	$V_T + (V_{SB} + 0.5\ V)$ $-V_T + (V_{SB} - 0.5\ V)$		R_{tst} = 330 Ω, R4 = 2.49 kΩ, See Notes 12, 13, and 14			10	mV
	$V_T - (V_{SB} + 0.5\ V)$ $-V_T - (V_{SB} - 0.5\ V)$					10	mV
Receiver input current			R_{tst} = 330 Ω, V_{CC} = 5 V, Both inputs at 2.5 V	−28		56	μA
			R_{tst} = 330 Ω, V_{CC} = 5 V, Input under test at 3.5 V, other input at 1.5 V	300		750	μA
			R_{tst} = 330 Ω, V_{CC} = 5 V, Input under test at 1.5 V, other input at 3.5 V	−200		−650	μA
Equalizer bias current			RCVINA and RCVINB open, EQUALA and EQUALB at 3 V	1.125		1.875	mA

NOTES: 12. R_{tst} is a resistor connected between pins 12 and 13; it replaces R1, R2, and C1 (Figure 2).
13. V_{IC} is the common mode voltage applied to RCVINA and RCVINB.
14. V_{SB} is the self-bias point for pins RCVINA and RCVINB. The exact value varies from device to device but is approximately $V_{CC}/2$.

transmitter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current, on	DROUTA, DROUTB	R_L = 75 Ω load to V_{CC}	20		30	mA
Output current, off	DROUTA, DROUTB	V_O = 8 V			100	μA

A

phantom driver

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	PHOUTA, PHOUTB	I_{OH} = −1 mA	4.1			V
			I_{OH} = −2 mA	3.8			V
I_{OS}	Short curcuit output current	PHOUTA, PHOUTB	V_O = 0, $\overline{NSRT}$ = V_{IL}	−4		−20	mA
I_{OH}	High-level output current	PHOUTA, PHOUTB	V_O = V_{CC}, $\overline{NSRT}$ = V_{OH}			100	μA
I_{OL}	Low-level output current	PHOUTA, PHOUTB	V_O = 0, $\overline{NSRT}$ = V_{IH}			−100	μA
I_{OZH}	Off-state output current with high-level voltage applied	PHOUTA, PHOUTB	V_O = 5.5 V, ENABLE = V_{IL}			100	μA
I_{OZL}	Off-state output current with low-level voltage applied	PHOUTA, PHOUTB	V_O = 0, ENABLE = V_{IL}			−100	μA

wire fault (see Note 15)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output-normal condition	$\overline{WFLT}$	2.9 kΩ ≤ R_{L1} ≤ 5.5 kΩ, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16	2.5			V
Output-open condition	$\overline{WFLT}$	9.9 kΩ ≤ R_{L1}, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16			0.5	V
Output-short condition	$\overline{WFLT}$	R_{L1} ≤ 0.1 kΩ, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16			0.5	V

NOTES: 15. The wire-fault logic will recognize a load condition corresponding to greater than 9.9 kΩ to ground as an open-circuit fault, but will not recognize a load condition less than 5.5 kΩ to ground as an open. The wire-fault logic will recognize a load condition corresponding to less that 100 Ω to ground as a short-circuit fault, but will not recognize a load condition corresponding to greater than 2.9 kΩ to ground as a short. Figure 4 illustrates this with R_{L1} connected from PHOUTA to ground and R_{L2} connected from PHOUTB to ground.

16. R_{L1} is connected from pin 19 to ground; R_{L2} is connected from pin 18 to ground.

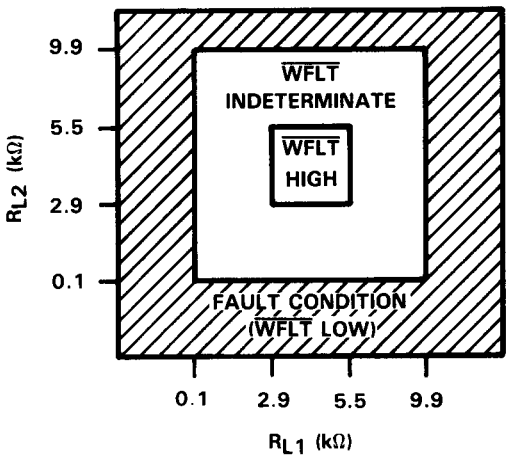


FIGURE 4. WIRE-FAULT PIN TEST

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PU}	Pump-up current	CHGPMP at 2 V–3 V, See Figures 5 and 6	−340		−460	μA
I_{PD}	Pump-down current		340		460	μA
I_{PU}-I_{PD}	Pump current matching				±20	μA
I_{PO}	Pump-off input current		0.5		−1.5	μA
I_{OS}	Short-circuit output current	V_O = 0			−3	mA

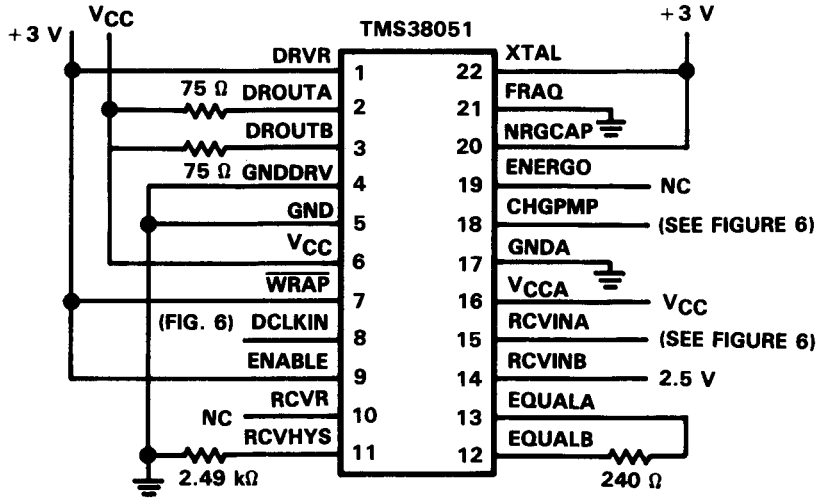


FIGURE 5. CHARGE-PUMP TEST CIRCUIT

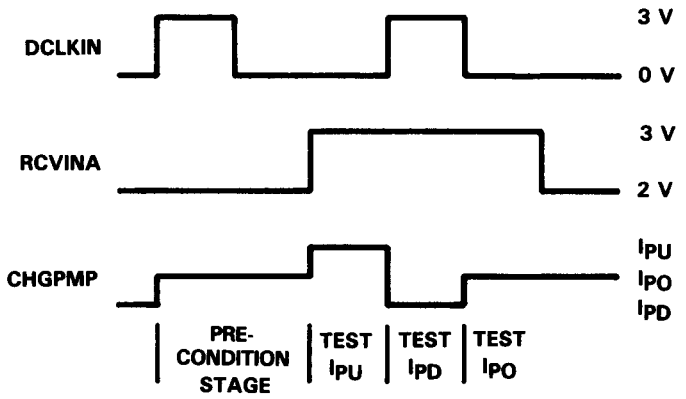


FIGURE 6. WAVEFORMS FOR CHARGE-PUMP TEST CIRCUIT

A

filter buffer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at FILTER	FILTER at 2 V – 3 V	–0.5		1.5	μA

energy detect

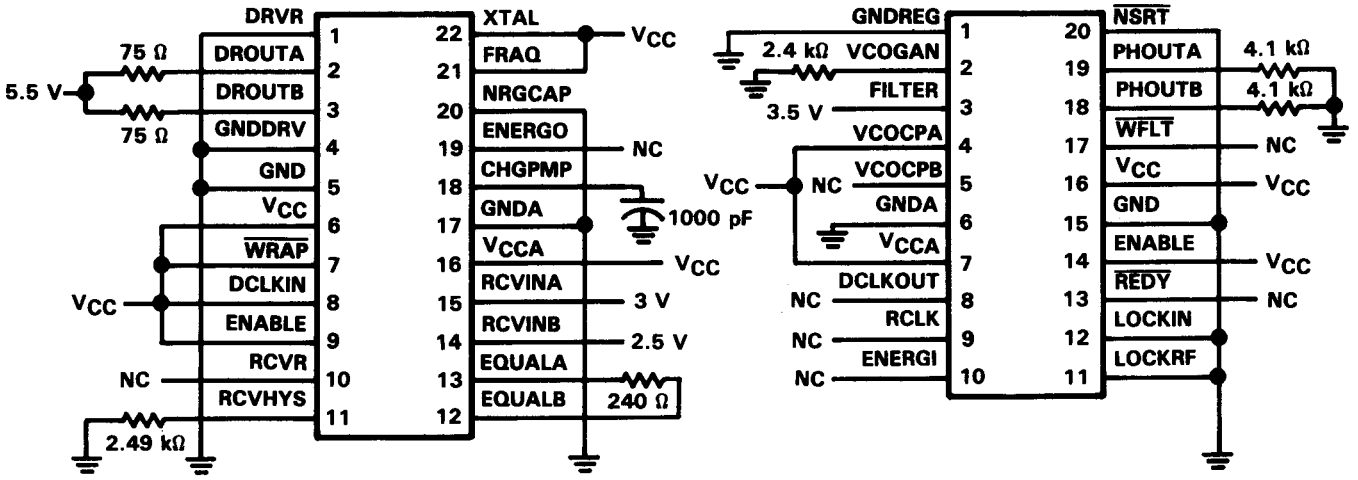
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	NRGCAP	ENERGO low	0.5			V
V_{IH}	High-level input voltage	NRGCAP	ENERGO high			2	V
V_{HYS}	Energy detect hysteresis	NGRCAP	$V_{HYS} = V_{IH} = V_{IL}$	0.1			V
t_d	Delay time, ENERGI valid to $\overline{REDY}$ valid	ENERGI, REDY				1	μS

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	TMS38051	See Figure 7(a)			93	mA
			See Figure 7(a), V_{CC} = 5.5 V, t_c = 80°C			88	mA
		TMS38052	See Figure 7(b)			59	mA
			See Figure 7(b), V_{CC} = 5.5 V, t_c = 75°C			53	mA

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001



NOTE 17: V_{CC} at 5.5 V.

FIGURE 7. I_{CC} TEST CIRCUITS

switching characteristics over full range of recommended operating conditions (unless otherwise noted)†

TTL output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	RCLK, RCVR	See Figures 10 and 14		16	ns
t_f	Output fall time				16	ns
t_r	Output rise time	DCLKOUT	See Figure 14		12	ns
t_f	Output fall time				12	ns

data buffer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static timing offset	See Note 18	8		−13	ns

†All parameters assume a load capacitance of 30 pF which includes probe and jig capacitance.

NOTE 18: Static timing offset may be measured indirectly by decreasing the duty cycle of a 4 MHz data signal at the receiver inputs (high time at RCVINA reduced, low time increased) until the TMS38051 recognizes a '0000' pattern in place of a '1010' pattern. Static offset is the high time at the point of transition minus 62.5 ns. Static timing offset may be determined by adjusting the duty cycle of a 4 MHz input signal (an all zeros data pattern) fed to the receiver inputs. Starting with a 50% duty cycle, the VCO will synchronize to the rising edge of the test waveform and the data buffer flip-flop will recognize a '10' pattern for each full cycle of 4 MHz signal. The high time of the input signal is reduced until, at about 25% duty cycle, the data buffer flip-flop is at the point of recognizing a '00' pattern. The static timing offset is this input signal high time less 62.5 ns. The input signal should be coupled into pin RCVINA with high and low levels of 0.5 V_{CC} ± 0.5 V, pin RCVINB held at 0.5 V_{CC}, with high time measured at the point where the differential input voltage is zero.

A

transmitter

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output rise time, t_r		DROUTA, DROUTB	V_L = V_{CC}, See Figures 9 and 11			20	ns
Output fall time, t_f						20	ns
Output asymmetry time, $t_A - t_B$		DROUTA, DROUTB	V_L = V_{CC}, See Figures 12 and 16			11	ns
Output skew time	$t_2 - t_1$ / $t_3 - t_4$	DROUTA, DROUTB	V_L = V_{CC}, See Figures 12 and 16			5	ns

internal wrap

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_1 Signal-to-receiver voltage swing	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Note 19 and Figures 8 and 9	150		500	mV
V_2 Noise signal voltage at driver	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Note 20 and Figure 9			10	mV
t_{PHL} Propagation delay, high-to-low-level output	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Figures 9 and 15			45	ns
t_{PLH} Propagation delay, low-to-high-level output	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Figures 9 and 15			45	ns

NOTES: 19. Peak-to-peak voltage swing between EQUALA and EQUALB. The differential between RCVINA and RCVINB is held at 0.5 V to assure that the receiver signal does not affect wrap mode.
20. Peak-to-peak voltage swing between DROUTA and DROUTB. The differential between RCVINA and RCVINB is held at 0.5 V to assure that the receiver signal does not affect wrap mode.

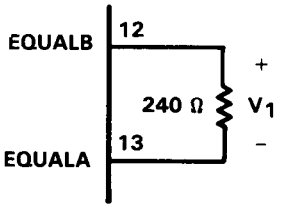


FIGURE 8

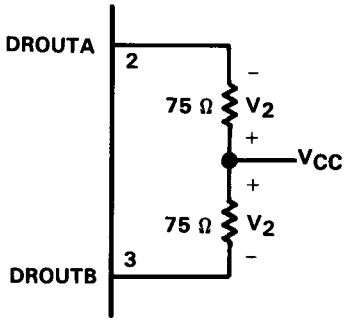


FIGURE 9

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

data buffer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay, high-to-low-level output, t_{PHL}	R_{L2} = 75 Ω, DCLKIN = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IH}, See Figures 9, 17 and Note 21			35	ns
Propagation delay, low-to-high-level output, t_{PLH}				35	ns
Output skew time				5	ns

NOTE 21: Output skew time = $|t_{PLH} - t_{PHL}|$

voltage-controlled oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Center frequency, fc	R3 = 2.49 kΩ, C2 = 200 pF, FILTER at 2.5 V See Figure 1	7.2	8	8.8	MHz
VCO gain	R3 = 2.49 kΩ, C2 = 200 pF, FILTER at 2 V-3 V See Figure 1	2.77	3.19	3.53	MHz/V
DCLKOUT asymmetry	f = 8 MHz, See Note 22 and Figure 13			8	%
RCLK asymmetry	f = 8 MHz, See Note 22 and Figure 13			10	%
Pulse duration, RCLK low, t_{wL2}	See Figure 18	46			ns
Pulse duration, RCLK high, t_{wH2}	See Figure 18	35			ns

NOTE 22: Asymmetry is defined as 100 $(t_{wH}-t_{wL})/(t_{wH} + t_{wL})$ where t_{wH} and t_{wL} represent the time above and below the 1.5-V level (see Figure 13). The filter voltage for nominal 8 MHz VCO frequency is predicted from the frequency measurements with FILTER at 2 V, 2.5 V, and 3 V assuming linear interpolation between these data points.

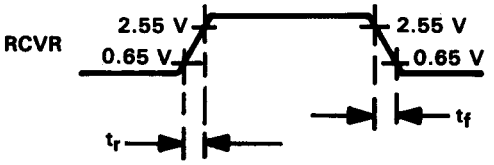


FIGURE 10. RCVR RISE AND FALL TIMES

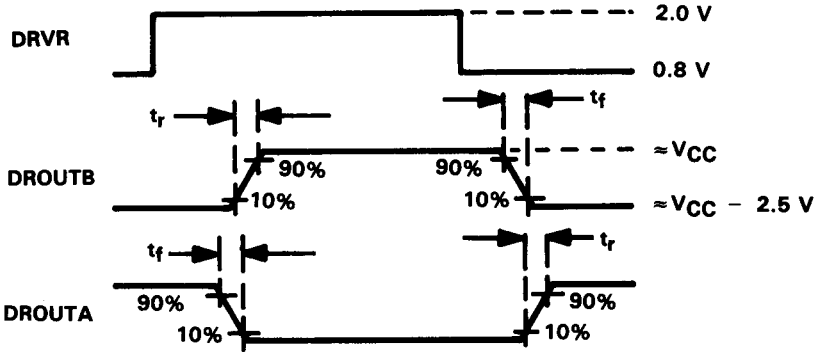
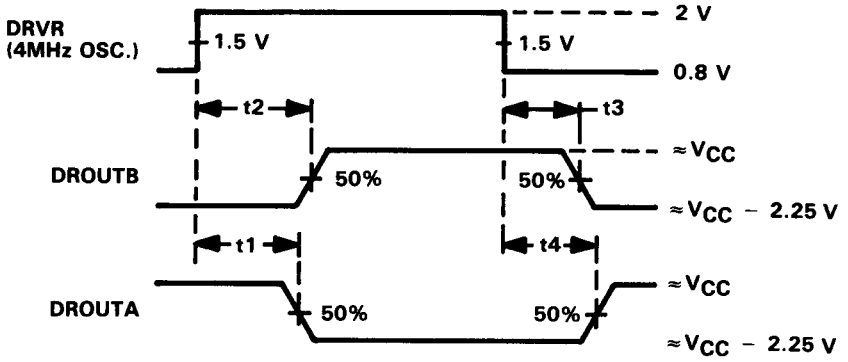


FIGURE 11. DROUTA AND DROUTB RISE AND FALL TIMES

A



t_A	$\frac{t_1 + t_2}{2}$
t_B	$\frac{t_3 + t_4}{2}$

FIGURE 12. SKEW AND ASYMMETRY FROM DRVR TO DROUTA AND DROUTB

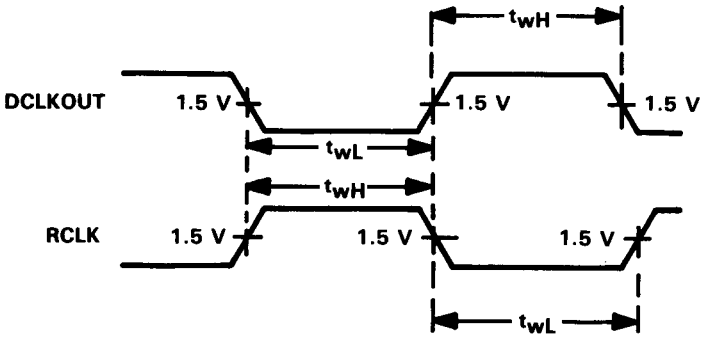


FIGURE 13. VCO ASYMMETRY

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

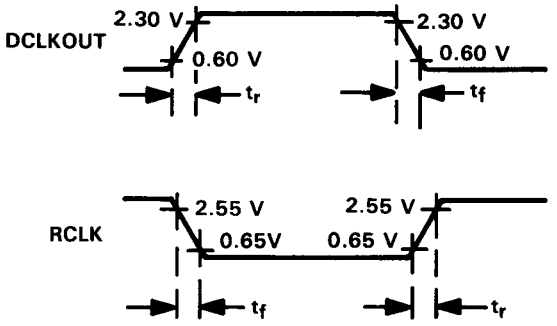


FIGURE 14. RCLK AND DCLK RISE AND FALL TIMES

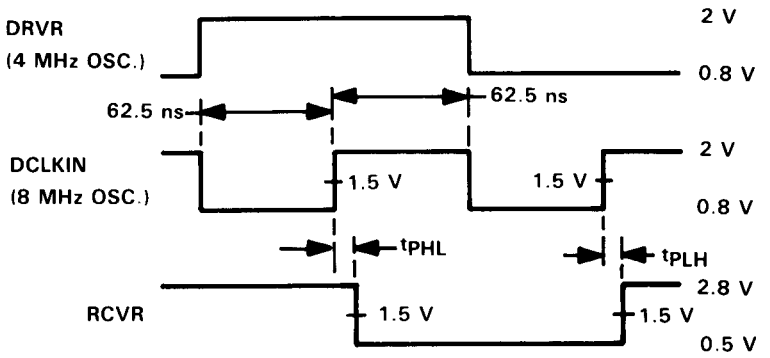
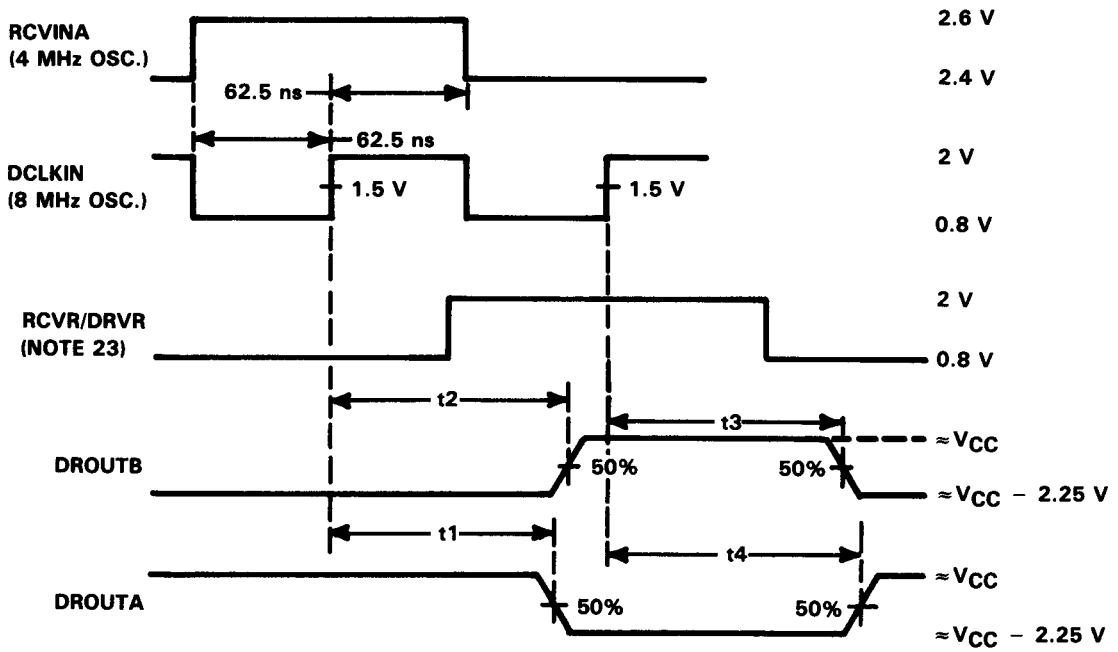


FIGURE 15. PROPAGATION DELAYS FROM DCLKIN TO RCVR WITH INTERNAL WRAP MODE

A



NOTE 23: For this test the RCVR output is tied directly to the DRVR input to test the asymmetry of the transmitter in a repeater configuration.

t_A	$\frac{t_1 + t_2}{2}$
t_B	$\frac{t_3 + t_4}{2}$

FIGURE 16. SKEW AND ASYMMETRY FROM DCLKIN TO DROUTA AND DROUTB

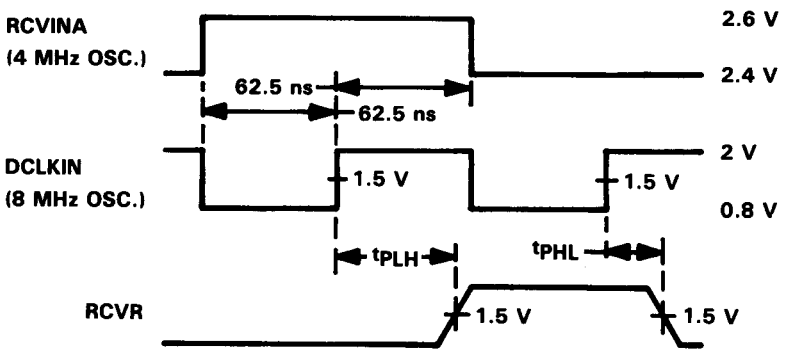


FIGURE 17. PROPAGATION DELAYS FROM DCLKIN TO RCVR

A

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

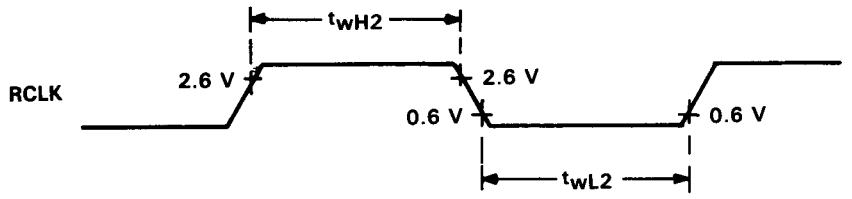


FIGURE 18. RCLK PULSE DURATIONS

A