8/7/6/5/4/3/2/1 Multi-Phase Buck Controller with PWM_VID and I²C Interface

NCP81610

Description

The NCP81610 is a multiphase synchronous controller optimized for new generation computing and graphics processors. The device is capable of driving up to 8 phases and incorporates differential voltage and phase current sensing, adaptive voltage positioning and PWM_VID interface to provide and accurately regulated power for computer or graphic controllers. The integrated power saving interface (PSI) allows for the processors to set the controller in one of three modes, i.e. all phases on, dynamic phases shedding or fixed low phase count mode, to obtain high efficiency in light−load conditions. The dual edge PWM multiphase architecture ensures fast transient response and good dynamic current balance.

Features

- Compliant with NVIDIA OVR4i+ Specifications
- Supports up to 8 Phases
- 2.8 V to 20 V Supply Voltage Range:
- 250 kHz to 1.2 MHz Switching Frequency (8 Phase)
- Power Good Output
- Under Voltage Protection (UVP)
- Over Voltage Protection (OVP)
- Per Phase Over Current Limiting (OCL)
- System Over Current Protection (OCP)
- Startup into Pre−Charged Loads while Avoiding False OVP
- Configurable Load Line
- High Performance Operational Error Amplifier
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Phase−to−Phase Dynamic Current Balancing
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Power Saving Interface (PSI)
- Automatic Phase Shedding with User Settable Thresholds
- PWM_VID and I²C Control Interface
- Compact 40 Pin QFN Package (5 x 5 mm Body, 0.4 mm Pitch)
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- GPU and CPU Power
- Graphic Cards
- Desktop and Notebook Applications
- Docking Stations
- Power Banks

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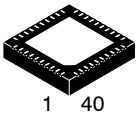
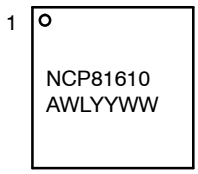


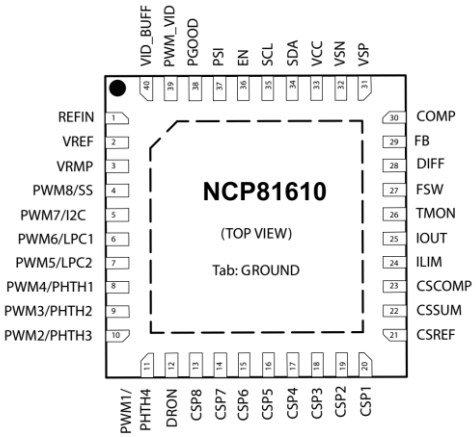
QFN40 5x5, 0.4P
CASE 485CR

MARKING DIAGRAM



NCP81610 = Device Code
A = Assembly Site
WL = Wafer Lot Number
YY = Year of Production, Last Two Numbers
WW = Work Week Number

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP81610MNTXG	QFN40 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

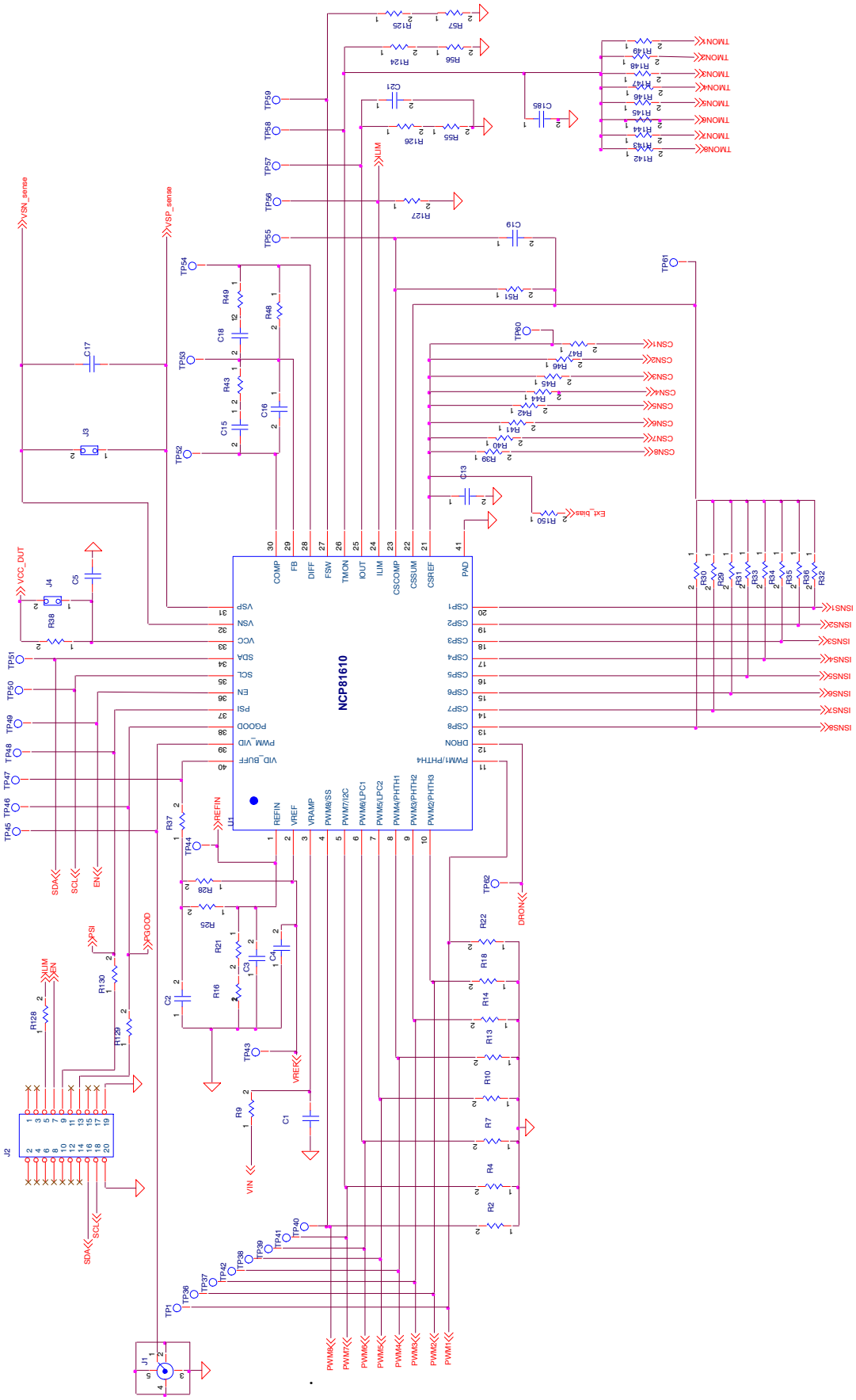


Figure 1. Typical Controller Application Circuit

PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	REFIN	I	Reference voltage input for output voltage regulation.
2	VREF	O	2.0 V output reference voltage. A 10 nF ceramic capacitor is required to connect this pin to ground.
3	VRMP	I	Feed−forward input of VIN for the ramp slope compensation.
4	PWM8/SS	I/O	PWM 8 output / Soft Start setting. During startup it is used to program the soft start time with a resistor to ground.
5	PWM7/I2C	I/O	PWM 7 output / I^2C address. During startup it is used to program I^2C address with a resistor to ground.
6	PWM6/LPC1	I/O	PWM 6 output / Low phase count 1. During startup it is used to program the warm boot−up power zone (PSI set low) with a resistor to ground.
7	PWM5/LPC2	I/O	PWM 5 output / Low phase count 2. During startup it is used to program the cold boot−up power zone (PSI set low) with a resistor to ground.
8	PWM4/PHTH1	I/O	PWM 4 output / Phase Shedding Threshold 1. During startup it is used to program the phase shedding threshold 1 (PSI set to mid state) with a resistor to ground.
9	PWM3/PHTH2	I/O	PWM 3 output / Phase Shedding Threshold 2. During startup it is used to program the phase shedding threshold 2 (PSI set to mid state) with a resistor to ground.
10	PWM2/PHTH3	I/O	PWM 2 output / Phase Shedding Threshold 3. During startup it is used to program the phase shedding threshold 3 (PSI set to mid state) with a resistor to ground.
11	PWM1/PHTH4	I/O	PWM 1 output / Phase Shedding Threshold 4. During startup it is used to program the phase shedding threshold 4 (PSI set to mid state) with a resistor to ground.
12	DRON	I/O	Bidirectional gate driver enable for external drivers.
13	CSP8	I	Non−inverting input to current balance sense amplifier for phase 8. Pull−up to VCC with a 2 kΩ resistor to disable the PWM8 output.
14	CSP7	I	Non−inverting input to current balance sense amplifier for phase 7. Pull−up to VCC with a 2 kΩ resistor to disable the PWM7 output.
15	CSP6	I	Non−inverting input to current balance sense amplifier for phase 6. Pull−up to VCC with a 2 kΩ resistor to disable the PWM6 output.
16	CSP5	I	Non−inverting input to current balance sense amplifier for phase 5. Pull−up to VCC with a 2 kΩ resistor to disable the PWM5 output.
17	CSP4	I	Non−inverting input to current balance sense amplifier for phase 4. Pull−up to VCC with a 2 kΩ resistor to disable the PWM4 output.
18	CSP3	I	Non−inverting input to current balance sense amplifier for phase 3. Pull−up to VCC with a 2 kΩ resistor to disable the PWM3 output.
19	CSP2	I	Non−inverting input to current balance sense amplifier for phase 2. Pull−up to VCC with a 2 kΩ resistor to disable the PWM2 output.
20	CSP1	I	Non−inverting input to current balance sense amplifier for phase 1. Pull−up to VCC with a 2 kΩ resistor to disable the PWM1 output.
21	CSREF	I	Total output current sense amplifier reference voltage input.
22	CSSUM	I	Inverting input of total current sense amplifier.
23	CSCOMP	O	Output of total current sense amplifier.
24	ILIM	I/O	Over current limit (OCL) threshold setting input. The threshold is set by a shunt resistor to the ground.
25	IOUT	O	Total output current. A resistor to GND is required to provide a voltage drop of 2V at the maximum output current.
26	TMON	I	DRMOS temperature monitoring.
27	FSW	I	Resistor to ground from this pin sets the operating frequency of the regulator.
28	DIFF	O	Output of the regulators differential remote sense amplifier.
29	FB	I	Error amplifier inverting (feedback) input.
30	COMP	O	Output of the error amplifier and the inverting input of the PWM comparator.

PIN DESCRIPTION (continued)

Pin No.	Pin Name	Pin Type	Description
31	VSP	I	Differential Output Voltage Sense Positive terminal.
32	VSN	I	Differential Output Voltage Sense Negative terminal.
33	VCC	I	Power for the internal control circuits. A 1 μF decoupling capacitor is requires from this pin to ground.
34	SDA	I/O	Serial Data bi−directional pin, requires pull−up resistor to VCC.
35	SCL	I	Serial Bus clock pin, requires pull−up resistor to VCC.
36	EN	I	Logic input. Logic high enables regulator output logic low disables regulator output.
37	PSI	I	Power Saving Interface control pin. This pin can be set low, high or left floating.
38	PGOOD	O	Open Drain power good indicator.
39	PWM_VID	I	PWM_VID buffer input.
40	VID_BUFF	O	PWM_VID pulse output from internal buffer.
41	AGND	GND	Analog ground and thermal pad, connected to system ground.

MAXIMUM RATINGS

Pin Symbol	Rating	Min	Typ	Max	Unit
VSN	Pin Voltage Range (Note 1)	GND−0.3	–	GND+0.3	V
VCC		−0.3	–	6.5	V
VRMP		−0.3	–	25	V
PWM_VID		−0.3 (−2, <50 ns)	–	VCC+0.3	V
All other pins		−0.3	–	VCC+0.3	V
COMP	Pin Current range	−2	–	2	mA
CSCOMP					
DIFF					
PGOOD					
VSN		−1	–	1	mA
MSL	Moisture Sensitivity Level	–	1	–	–
T_{SLD}	Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	–	260	–	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. All signals referenced to GND unless noted otherwise
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Symbol	Rating	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Characteristics, QFN40, 5 x 5 mm) Thermal Resistance, Junction−to−Air (Note[1])	–	68	–	°C/W
T_J	Operating Junction Temperature Range (Note [2])	−40	–	125	°C
T_A	Operating Ambient Temperature Range	−10	–	100	°C
T_{STG}	Maximum Storage Temperature Range	−55	–	150	°C

[1] JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM)
[2] JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM)

ELECTRICAL CHARACTERISTICS ($-10°C < T_A < 100°C$; $4.6\ V < VCC < 5.4\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCC SUPPLY						
VCC	Supply voltage range		4.6	–	5.4	V
ICC	VCC Quiescent current	Enable low, 2nd time	–	–	100	μA
		8 phase operation	–	40	–	mA
		1 phase – DCM operation	–	10	–	mA
$UVLO_{Rise}$	UVLO Threshold	VCC Rising	–	–	4.5	V
$UVLO_{Fall}$		VCC Falling	4	–	–	V
$UVLO_{Hyst}$	VCC UVLO Hysteresis		–	200	–	mV
SWITCHING FREQUENCY						
F_{SW}	Switching Frequency Range	8 phase configuration	250	–	1200	kHz
ΔF_{SW}	Switching Frequency Accuracy	F_{SW} = 810 kHz	–4	–	+4	%
ENABLE INPUT						
I_L	Input Leakage	EN = 0 V or VCC	–1.0	–	1.0	μA
V_{IH}	Upper Threshold		1.2	–	–	V
V_{IL}	Lower Threshold		–	–	0.6	V
DRON						
V_{OH}	Output High Voltage	Sourcing 500 μA	3.0	–	–	V
V_{OL}	Output Low Voltage	Sinking 500 μA	–	–	0.1	V
t_R, t_F	Rise time (Note 3)	Cl (PCB) = 20 pF, ΔVo = 10% to 90%	–	160	–	ns
	Fall time (Note 3)	Cl (PCB) = 20 pF, ΔVo = 10% to 90%	–	3	–	ns
$R_{PULL-UP}$	Internal Pull–up Resistance (Note 3)		–	2.0	–	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance (Note 3)	Vcc = 0 V	–	12	–	kΩ
PGOOD						
V_{OL}	Output low voltage	I_{PGOOD} = 10 mA (sink)	–	–	0.4	V
I_L	Leakage Current	P_{GOOD} = 5 V	–	–	0.2	μA
T_init	Output voltage initialization time	From EN to ramp starts, 2nd ENABLE	–	–	0.5	ms
T_total	Total Soft Startup Period	T_Ramp ≤ 0101, RT_Ramp ≤ 41.2 kΩ; From EN to PGOOD	–	–	2.0	ms
VRMP						
VRMP	Supply Range		2.8	–	20	V
$V_{RMPrise}$	UVLO	VRMP rising	–	–	2.8	V
$V_{RMPfall}$		VRMP falling	2.5	–	–	V
$V_{RMPhyst}$	VRMP UVLO Hysteresis		–	150	–	mV
PROTECTION FEATURES: OVP, UVP, TMON, ILIM, CLIM, TSD						
UVP	Under Voltage Protection (UVP) Threshold	Relative to REFIN Voltage	–	–	–400	mV
T_{UVP}	Under Voltage Protection (UVP) Delay (Note 3)		–	5	–	μs
OVP	Over Voltage Protection (OVP) Threshold	Relative to REFIN Voltage	500	–	–	mV
T_{OVP}	Over Voltage Protection (OVP) Delay (Note 3)		–	5	–	μs
T_{MON}	External Temperature Monitoring (TMON) Linear Range		0.6	–	1.9	V
T_{MONLT}	TMON Latch Threshold	Default	1.9	2.0	2.1	V

ELECTRICAL CHARACTERISTICS (−10°C < T_A < 100°C; 4.6 V < VCC < 5.4 V; C_{VCC} = 0.1 μF unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PROTECTION FEATURES: OVP, UVP, TMON, ILIM, CLIM, TSD						
T_{MONLN}	TMON Linear Range		0	–	2.0	V
T_{MON_ADC}	TMON Input to ADC Accuracy		–	5	–	%
T_{SD}	Chip Thermal Shutdown Temperature (Note 3)	Temperature Rising	145	155	–	C
T_{SD_HYS}	Chip Thermal Shutdown Hysteresis (Note 3)		–	15	–	C
$CLIM_{FALL}$	CLIM Overall Current Limit Entering	CSCOMP Falling	–	225	–	mV
I_{LIM}	ILIM Sourcing Current		9	10	11	μA
V_{ILIM}	ILIM range		0	–	2	V
R_{ILIM}	RILIM range		0	–	200	kΩ
PWM OUTPUTS						
V_{OH}	Output High Voltage	Sourcing 500 μA	VCC−0.2	–	–	V
V_{MID}	Output Mid Voltage		1.4	1.5	1.6	V
V_{OL}	Output Low Voltage	Sinking 500 μA	–	–	0.6	V
t_R, t_F	Rise and Fall Time (Note 3)	C_L(PCB) = 50 pF, ΔVo = 10% to 90% of VCC	–	10	–	ns
I_L	Tri−State Output Leakage	Gx = 2.0 V, x = 1 − 8, EN = Low	−1.0	–	1.0	μA
Ton	Minimum On Time (Note 3)	FSW=600 kHz	–	12	–	ns
$VCOMP_{0\%}$	0% Duty Cycle	Comp voltage when PWM = Low	–	1.3	–	V
$VCOMP_{100\%}$	100% Duty Cycle	Comp voltage when PWM = High	–	2.5	–	V
∅	PWM Phase Angle Error	Between Adjacent phases	–	±15	–	°
PHASE DETECTION						
V_{PHDET}	Phase Detection Threshold Voltage	CSP2 to CSP8	–	–	VCC−0.1	V
T_{PHDET}	Phase Detect Timer (Note 3)	CSP2 to CSP8	–	1.1	–	ms
ERROR AMPIFIER						
I_{BIAS}	Input Bias Current		−400	–	400	nA
G_{OL}	Open Loop DC Gain (Note 3)	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	80	–	dB
GBW	Open Loop Unity Gain Bandwidth (Note 3)	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	20	–	MHz
SR	Slew Rate (Note 3)	ΔVin = 100 mV, G = −10 V/V, ΔVout = 0.75 V − 1.52 V, C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	5	–	V/μs
V_{OUT}	Maximum Output Voltage	I_{SOURCE} = 2mA	3.5	–	–	V
V_{OUT}	Minimum Output Voltage	I_{SINK} = 2mA	–	–	1	V
DIFFERENTIAL SUMMING AMPLIFIER						
I_{BIAS}	Input bias current		−400	–	400	nA
V_{IN}	VSP input voltage		0	–	2	V
V_{IN}	VSN input voltage		−0.3	–	0.3	V
BW	−3 dB Bandwidth (Note 3)	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	12	–	MHz
G	Closed loop DC gain (VSP−VSN to DIFF)	VSP to VSN = 0.5 to 1.3 V	–	1	–	V/V
V_{OUT}	Maximum output voltage	I_{SOURCE} = 2 mA	3	–	–	V
V_{OUT}	Minimum output voltage	I_{SINK} = 2 mA	–	–	0.8	V

ELECTRICAL CHARACTERISTICS ($-10°C < T_A < 100°C$; $4.6\ V < VCC < 5.4\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CURRENT SUMMING AMPLIFIER						
V_{OS}	Offset Voltage		−500	–	500	μV
I_L	Input Bias Current	CSSUM = CSREF = 1 V	−7.5	–	7.5	μA
G	Open Loop Gain (Note 3)		–	80	–	dB
GBW	Current sense Unity Gain Bandwidth (Note 3)	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	10	–	MHz
V_{OUT}	Maximum CSCOMP Output Voltage	I_{SOURCE} = 2 mA	3.5	–	–	V
V_{OUT}	Minimum CSCOMP Output Voltage	I_{SINK} = 1 mA	–	–	0.3	V
PHASE CURRENT AMPLIFIER						
I_{BIAS}	Input Bias Current	CSPX − CSPX + 1 = 1.2 V	−50	–	50	nA
V_{CM}	Common Mode Input Voltage Range (Note 3)	CSPx = CSREF	0	–	2	V
V_{DIFF}	Differential Mode Input Voltage Range	CSREF = 1.2 V	−250	–	250	mV
	Closed loop Input Offset Voltage Matching	CSPx = 2 V, Measured from the average	−1.5	–	1.5	mV
G	Current Sense Amplifier Gain	−250 mV < CSPx − CSREF < 250 mV	5.5	6.0	6.5	V/V
BW	−3dB Bandwidth (Note 3)		–	8	–	MHz
V_{ZCD}	Single Phase ZCD comparator threshold CSP1 − CSREF	PSI = 0, Single Phase, By Default	–	0	–	mV
T_{ZCD}	ZCD Comparator Delay (Note 3)		–	150	–	ns
V_{ZCD_UNIT}	ZCD User Trim Resolution (Note 3)		–	1.2	–	mV
IOUT						
V_{OS}	Input Reference Offset Voltage	CSCOMP to CSREF	−10	–	10	mV
I_{OUT}	Output Current Max	10 μA on Rcur	–	100	–	μA
G_{IOUT}	IOUT Current Gain	Iout / I_{Rcur}	–	10	–	A/A
V_{IOUT_RG}	IOUT Linear Range		0	–	3	V
V_{IOUT_ADC}	IOUT Input to ADC Accuracy	$0 < V_{IOUT} < 2$ V	–	5	–	%
VOLTAGE REFERENCE						
VREF	VREF Reference Voltage	I_{REF} = 1 mA	1.98	2	2.02	V
ΔVREF	VREF Reference accuracy	Over Temp	–	1	1.5	%
PWM_VID BUFFER						
V_{IH}	Upper threshold		1.4	–	–	V
V_{IL}	Lower threshold		–	–	0.5	V
F_{PWM_VID}	PWM_VID switching frequency		400	–	5000	kHz
t_R	Output Rise Time (Note 3)		–	3	–	ns
t_F	Output Fall Time (Note 3)		–	3	–	ns
Δt	Rising and falling edge delay (Note 3)	$\Delta t = t_R - t_F$	–	0.5	–	ns
t_{PD}	Propagation Delay (Note 3)	$t_{PD} = t_{PDHL} = t_{PDLH}$	–	8	–	ns
Δt_{PD}	Propagation Delay Error (Note 3)	$\Delta t_{PD} = t_{PDHL} - t_{PDLH}$	–	0.5	–	ns
VOCL_min						
VOCL_min	VOCL_min voltage range		0.2	–	1.3	V
VOCL_min_var	VOCL_min accuracy	VOCL_min = 1 V	–	2	–	%
PSI						
V_{IH}	PSI high Threshold		1.45	–	–	V

ELECTRICAL CHARACTERISTICS ($-10°C < T_A < 100°C$; $4.6\ V < VCC < 5.4\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PSI						
V_{MID}	PSI mid threshold	Auto Phase Shedding Enabled	0.8	–	1	V
V_{IL}	PSI low threshold		–	–	0.575	V
I_L	PSI input leakage current	V_{PSI} = 0 V o VCC	–1	–	1	μA
VMON						
V_{MONLN}	VMON Linear Range		0	–	2.0	V
V_{MON_ADC}	VMON Input to ADC Accuracy		–	5	–	%
REFIN						
R_{DISCH}	REFIN Discharge Switch ON– Resistance (Note 3)	$I_{REEFIN\ (SINK)}$ = 2 mA	–	10	–	Ω
$V_{ORP/VREFIN}$	Ratio of Output voltage ripple transferred from REFIN / REFIN Voltage ripple (Note 3)	F_{PWM_VID} = 400 kHz, $F_{SW} \le$ 600 kHz	–	10	–	%
$V_{ORP/VREFIN}$		F_{PWM_VID} = 1000 kHz, $F_{SW} \le$ 600 kHz	–	30	–	
I²C (Note 3)						
V_{IH}	Logic High Input Voltage		1.4	–	5	V
V_{IL}	Logic Low Input Voltage		0	–	0.5	V
	Hysteresis		–	80	–	mV
V_{OL}	Output Low Voltage	I_{SDA} = –6 mA	–	–	0.4	V
I_L	Input Current		–1	–	1	μA
C_{SDA}, C_{SCL}	Input Capacitance		–	5	–	pF
f_{SCL}	Clock Frequency	see Figure 2	–	–	400	kHz
t_{LOW}	SCL Low period		1.3	–	–	μs
t_{HIGH}	SCL High period		0.6	–	–	μs
t_R	SCL/SDA rise time		–	–	300	ns
t_F	SCL/SDA fall time		–	–	300	ns
$t_{SU;STA}$	Start condition setup time		600	–	–	ns
$t_{HD;STA}$	Start condition hold time (Note 4)		600	–	–	ns
$t_{SU;DAT}$	Data setup time (Note 5)		100	–	–	ns
$t_{HD;DAT}$	Data hold time (Note 5)		300	–	–	ns
$t_{SU;STO}$	Stop condition setup time (Note 6)		600	–	–	ns
t_{BUF}	Bus free time between stop and start		1.3	–	–	μs

3. Guaranteed by design, not production tested.
4. Time from 10% of SDA to 90% of SCL
5. Time from 10% or 90%of SDA to 10% of SCL
6. Time from 90% of SCL to 10% of SDA

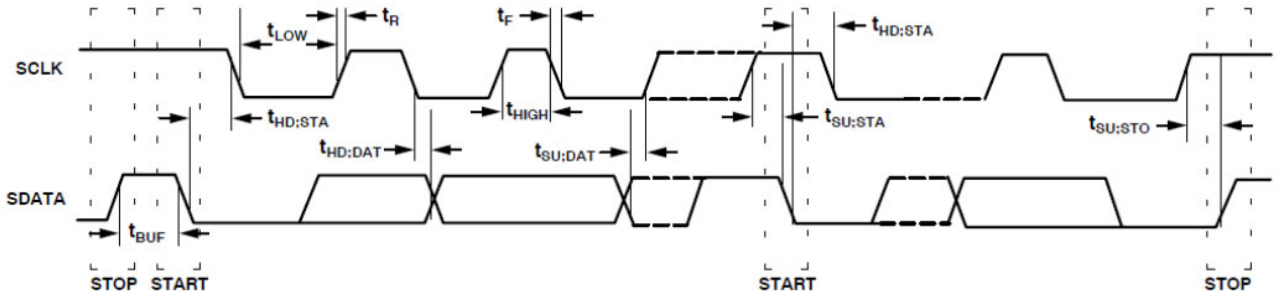


Figure 2. I²C Timing Diagram

Applications Information

The NCP81610 is a multi−phase buck converter controller optimized for the next generation computing and graphic processor applications. It contains eight PWM channels which can be individually configured to operate from one to eight phases.

The output voltage is set by applying a PWM signal to the PWM_VID input of the device. The controller converts the PWM_VID signal (400 kHz ~ 5 MHz) with variable high and low levels into a 2 V PWM signal which is then being filtered and averaged, and applied to the REFIN pin for internal regulation reference.

The remote output voltage and ground are differentially sensed and the REFIN value is subtracted from sensed voltage. The result is biased ,combined with loadline input and applied to the error amplifier. If the loadline is disabled, any difference between the sensed output voltage and the REFIN pin average voltage will change the PWM outputs duty cycle until the two voltages are identical. The load current is current is continuously monitored on each phase and the PWM outputs are adjusted to ensure adjusted to ensure even distribution of the load current across all phases. Per phase current is monitored cycle by cycle with current limiting.

The device incorporates different fault protections including per phase overcurrent limiting (OCL), on chip over temperature (TSD), external power stage over temperature monitoring (TMON), output under voltage (UVP) and output overvoltage (OVP) protections.

The communication between the NCP81610 and the user is handled with two interfaces, PWM_VID to set the output voltage and I^2C to configure or monitor the status of the controller. The operation of the internal blocks of the device is described in more details in the following sections.

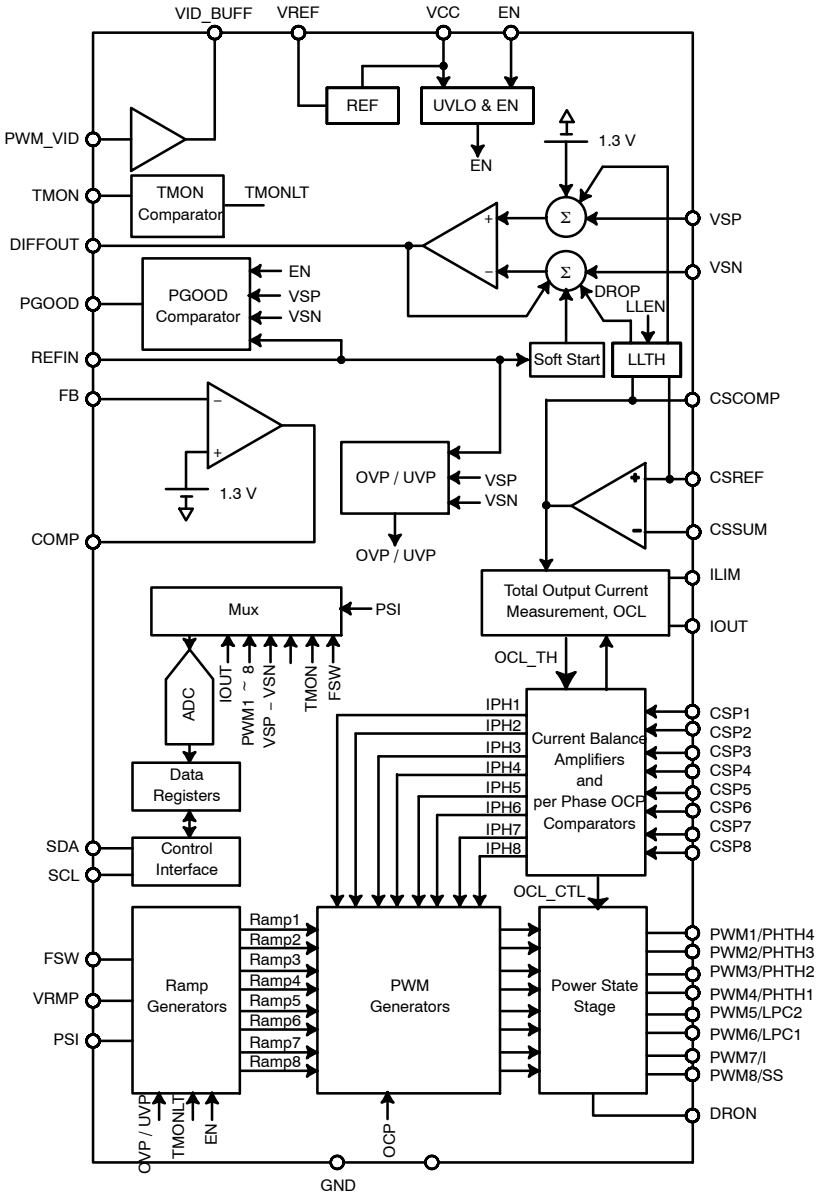


Figure 3. NCP81610 Functional Block Diagram

Soft Start

Soft start is defined as the transition from Enable assertion high to the assertion of Power good as shown in Figures 4, 5.

The output is set to the desired voltage in two steps: T_init is a fixed initialization step of less than 1 ms followed by a ramp−up step T_ramp where the output voltage is ramped to the final value set by the PWM_VID interface and REFIN. During the soft start phase, PGOOD pin is initially set low and will be set high when the output voltage is within regulation and the soft start is complete. The PGOOD signal only de−asserts (pull low) when the controller shuts down due to a fault condition (UVLO, OVP or UVP event).

The output voltage ramp−up time is user settable by connecting a resistor between pin PWM8/SS and GND. The controller will measure the resistance value at power−up by sourcing a 10 μA current through this resistor and set the ramp time (T_ramp) as shown in Table 11. To prevent false over current claim, CSREF signal of the current summing amplifier needs to be ready before the soft start is complete.

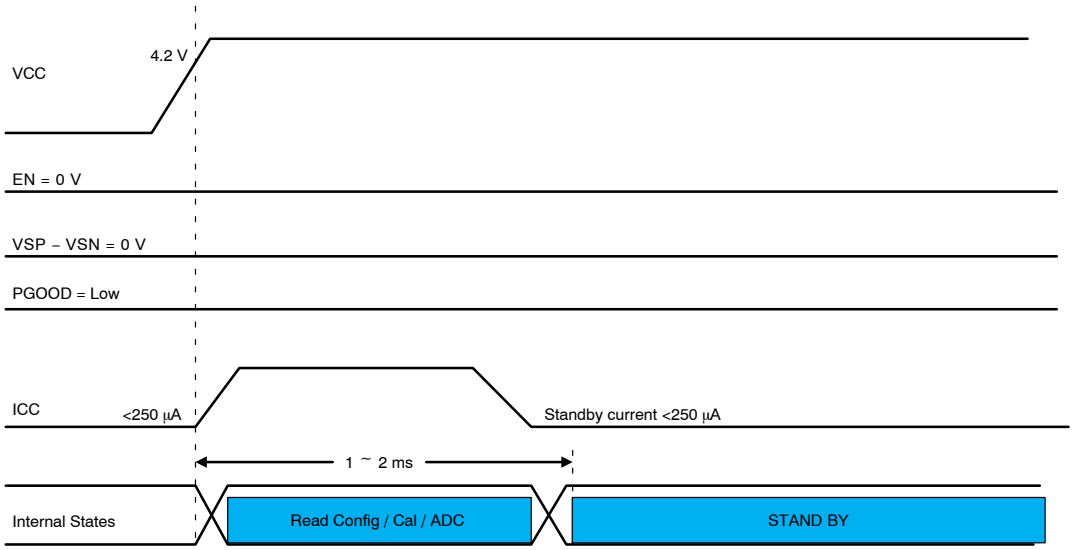


Figure 4. VCC across UVLO with EN = 0

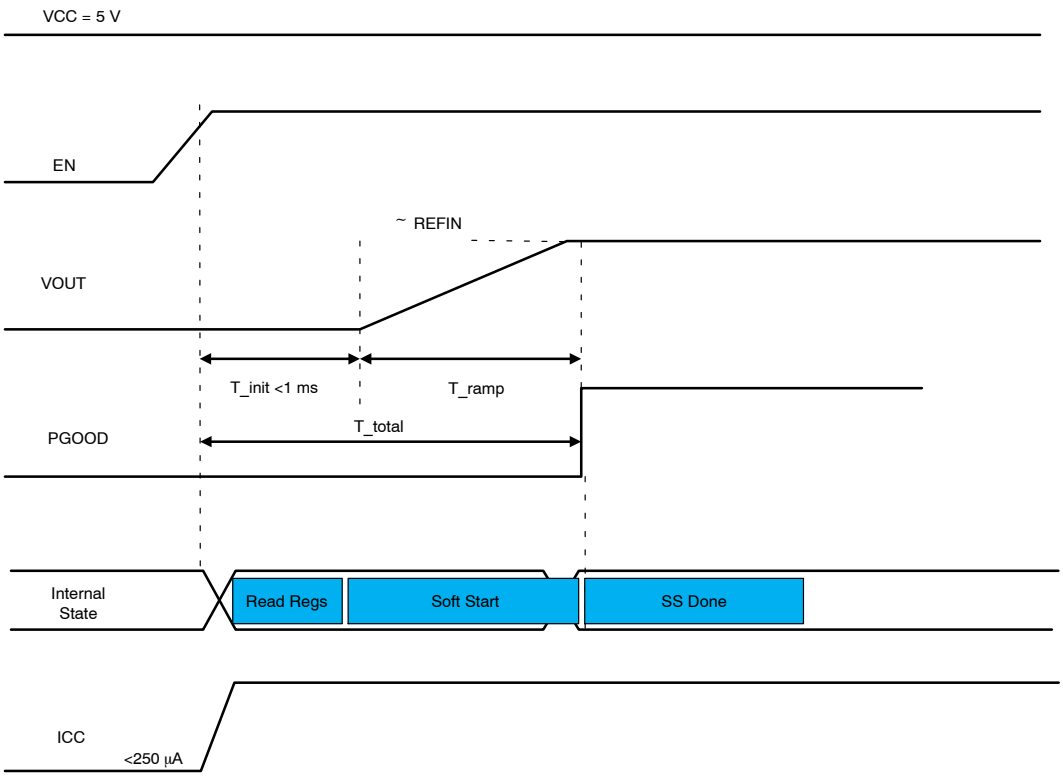


Figure 5. Soft Start by Toggling EN

PWM_VID Interface

PWM−VID is a single wire dynamic voltage control interface where the regulated voltage is set by the duty cycle of the PWM signal applied to the controller.

The device controller converts the variable amplitude PWM signal into a constant 2 V amplitude PWM signal while preserving the duty cycle information of the input signal. In addition, if the PWM_VID input is left floating, the VID_BUFF output is tri−stated (floating).

The constant amplitude PWM signal is then connected to the REFIN pin through a scaling and filtering network (see Figure 6). This network allows the user to set the minimum and maximum REFIN voltages corresponding to 0% and 100% duty cycle values.

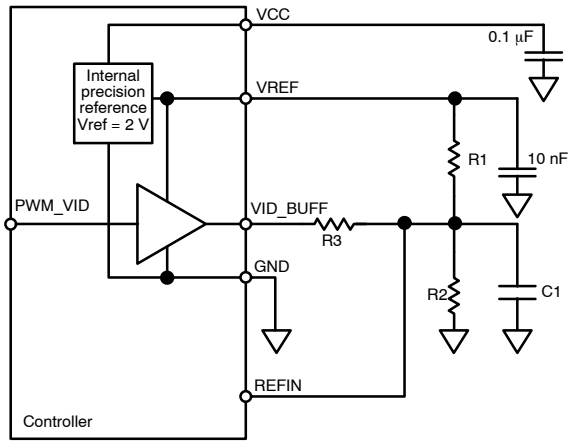


Figure 6. PWM VID Interface

The minimum (0% duty cycle), maximum (100% duty cycle) and boot (PWM_VID input floating) voltages can be calculated with the following formula:

$$V_{MAX} = V_{REF} \cdot \frac{1}{1 + \frac{R_1 \cdot R_3}{R_2 \cdot (R_1 + R_3)}} \quad \text{(eq. 1)}$$

$$V_{MIN} = V_{REF} \cdot \frac{1}{1 + \frac{R_1 \cdot (R_2 + R_3)}{R_2 \cdot R_3}} \quad \text{(eq. 2)}$$

$$V_{BOOT} = V_{REF} \cdot \frac{1}{1 + \frac{R_1}{R_2}} \quad \text{(eq. 3)}$$

Remote Voltage Sense

A high performance true differential amplifier allows the controller to measure the output voltage directly at the load using the VSP (VOUT) and VSN (GND) pins. This keeps the ground potential differences between the local controller ground and the load ground reference point from affecting regulation of the load. The output voltage of the differential amplifier is set by the following equation:

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{REFIN}) + (V_{DROOP} - V_{CSREF}) \quad \text{(eq. 4)}$$

where,

V_{DIFOUT} is the output voltage of the differential amplifier

$V_{VSP}−V_{VSN}$ is the regulated output voltage sensed at the load

V_{REFIN} is the voltage at the output pin set by the PWM_VID interface

$V_{DROOP}−V_{CSREF}$ is the expected drop in the regulated voltage as a function of the load current (load−line)

1.3 V is an internal reference voltage used to bias the amplifier inputs to allow both positive and negative output voltage for V_{DIFOUT}

Error Amplifier

A high performance wide bandwidth error amplifier is provided for fast response to transient load events. Its inverting input is biased internally with the same 1.3 V reference voltage as the one used by the differential sense amplifier to ensure that both positive and negative error voltages are correctly handled.

An external compensation circuit should be used (usually type III) to ensure that the control loop is stable and has adequate response.

Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used to generate the PWM signals using internal comparators (see Figure 7) The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage.

The VRMP pin also has a UVLO function. The VRMP UVLO rising threshold is 2.8 V, only active after the EN is toggled high. The VRMP pin is a high impedance input when the controller is disabled.

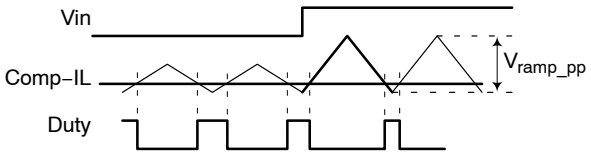


Figure 7. Ramp Feed−Forward Circuit

PWM Output Configuration

By default the controller operates in 8 phase mode, however the phases can be disabled by connecting the corresponding CSP pins to VCC. At power−up the NCP81610 measures the voltage present at each CSP pin and compares it with the phase detection threshold. If the voltage exceeds the threshold, the phase is disabled. The phase configurations that can be achieved by the device are listed in Table 2. The active phase (PWM_X) information is also available to the user in the phase status register.

PSI, LPC_X, $PHTH_X$

The NCP81610 incorporates a power saving interface (PSI) to maximize the efficiency of the regulator under various loading conditions. The device supports up to five distinct operation modes, called power zones using the PSI, LPC_X and $PHTH_X$ pins (see Table 3). At power−up the controller reads the PSI pin logic state and sources a 10 μA current through the resistors connected to the LPC_X and $PHTH_X$ pins, measures the voltage at these pins and configures the device accordingly.

The configuration can be changed by the user by writing to the LPC_X and $PHTH_X$ configuration registers.

After EN is set high, the NCP81610 ignores any change in the PSI pin logic state until the output voltage reaches the nominal regulated voltage.

When PSI = High, the controller operates with all active phases enabled regardless of the load current. If PSI = Mid, the NCP81610 operates in dynamic phase shedding mode where the voltage present at the IOUT pin (the total load current) is measured every 10 μs and compared to the $PHTH_X$ thresholds to determine the appropriate power zone.

The resistors connected between the $PHTH_X$ and GND should be picked to ensure that with a 10 μA source current the voltage reading will match the voltage drop at the IOUT pin at the desired load current. Please note that the maximum allowable voltage at the IOUT pin at the maximum load current is 2 V. Any $PHTH_X$ threshold can be disabled if the voltage drop across the $PHTH_X$ resistor is ≥2 V for a 10 μA current, the pin is left floating or 0xFF is written to the appropriate $PHTH_X$ configuration register. The automatic phase shedding mode is only enabled after the output voltage reaches the nominal regulated voltage.

When PSI = low, the controller is set to a fixed power zone regardless of the load current, programmable through user register 0x34 and 0x36. The LPC2 setting controls the power zone used during cold boot−up (After power on VCC UVLO, EN is set high) while the LPC1 configuration sets the power zone in the consecutive soft startup by toggling EN only (soft boot−up).

NCP81610 has the internal zero current detection function (ZCD) enabled by default; if PSI = Low and the system is configured to single phase mode (Power Zone = 4), the single phase switching circuit operates in diode emulation mode. The NCP81610 controller will sense the current information from CSP1−CSREF differential voltage in the internal ZCD mode with PWM1 toggling between High, Mid and Low voltage levels accordingly. The controller ZCD threshold can be adjusted by I^2C command to accommodate different power stages and the propagation delay.

The ZCD function within the NCP81610 can be disabled through the I^2C command. While internal ZCD function is disabled, PWM1 can be configured to either toggle between High and Low or High and Mid−level depending on type of the power stage devices; In this case the power stage current sensing circuit will be used for zero current detection function if necessary.

NCP81610 I^2C Address

On power up, a 10 μA current is sourced from PWM7/I2C pin to the shunt resistor to configure the I2C slave address of the NCP81610. There are four I2C addresses available for this chip associated with different shunt resistor values.

Table 1. I2C ADDRESS SETTING

Resistance (kΩ)	I^2C Address
10	0x20
41.2	0x30
100	0x40
249	0x50

Table 2. PWM OUTPUT CONFIGURATION

Configuration	Phase Configuration	CSP Pin Configuration (✓ = Normal Connection, X = Tied to VCC)								Enabled PWM Outputs (PWM_X Pins)
		CSP1	CSP2	CSP3	CSP4	CSP5	CSP6	CSP7	CSP8	
1	8 phase	✓	✓	✓	✓	✓	✓	✓	✓	1, 2, 3, 4, 5, 6, 7, 8
2	7 phase	✓	✓	✓	✓	✓	✓	✓	X	1, 2, 3, 4, 5, 6, 7
3	6 phase	✓	✓	✓	✓	✓	✓	X	X	1, 2, 3, 4, 5, 6
4	5 phase	✓	✓	✓	✓	✓	X	X	X	1, 2, 3, 4, 5
5	4 phase	✓	✓	✓	✓	X	X	X	X	1, 2, 3, 4
6	3 phase	✓	✓	✓	X	X	X	X	X	1, 2, 3
7	2 phase	✓	✓	X	X	X	X	X	X	1, 2
8	1 phase	✓	X	X	X	X	X	X	X	1

Table 3. PSI, LPC_X, $PHTH_X$ CONFIGURATION

PSI Logic State	LPC1, LPC2 Resistor (kΩ)	IOUT vs. $PHTH_X$ Comparison	Power Zone							
			8 Phase	7 Phase	6 Phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
High	Disabled	Function Disabled	0	0	0	0	0	0	0	0
Low	10		0	0	0	0	0	0	0	0
	23.2		1	1	0	0	0	0	0	0
	37.4		2	2	2	0	2	0	0	0
	54.9		3	3	3	3	3	3	3	0
	78.7		4	4	4	4	4	4	4	4
Mid	Function Disabled	IOUT > PHTH4	0	0	0	0	0	0	0	0
		PTHT4 > IOUT > PHTH3	1	1	0	0	0	0	0	0
		PHTH3 > IOUT > PHTH2	2	2	2	0	2	0	0	0
		PHTH2 > IOUT > PHTH1	3	3	3	3	3	3	3	0
		IOUT < PHTH1	4*	4	4	4	4	4	4	4

NOTES: Power zone 4 is usually DCM, while zones 0 to 3 are CCM.

Table 4. PSI, LPC_X, $PHTH_X$ CONFIGURATION

Power Zone	PWM Output Configuration	PWM Output Status (✓ = Enabled, X = Disabled)							
		PWM1	PWM2	PWM3	PWM4	PWM5	PWM6	PWM7	PWM8
0	8 phase	✓	✓	✓	✓	✓	✓	✓	✓
1		✓	X	✓	X	✓	X	✓	X
2		✓	X	X	X	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	7 phase	✓	✓	✓	✓	✓	✓	✓	X
1		✓	X	✓	✓	✓	X	✓	X
2		✓	X	X	✓	X	X	✓	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	6 phase	✓	✓	✓	✓	✓	✓	X	X
2		✓	X	✓	X	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	5 phase	✓	✓	✓	✓	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	4 phase	✓	✓	✓	✓	X	X	X	X
2		✓	X	✓	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X

Table 4. PSI, LPC_X, $PHTH_X$ CONFIGURATION

Power Zone	PWM Output Configuration	PWM Output Status (✓ = Enabled, X = Disabled)							
		PWM1	PWM2	PWM3	PWM4	PWM5	PWM6	PWM7	PWM8
0	3 phase	✓	✓	✓	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	2 phase	✓	✓	X	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	1 phase	✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X

Power Zone Transition / Phase Shedding

The power zones supported by the NCP81610 are set by the resistors connected to the LPC_X pins (PSI = Low) or $PHTH_X$ pins (PSI = Mid).

When PSI is set to the Mid−state, the NCP81610 employs a phase shedding scheme where the power zone is automatically adjusted for optimal efficiency by continuously measuring the total output current (voltage at the IOUT pin) and compare it with the $PHTH_X$ thresholds. When the comparison result indicates that a lower power zone number is required (an increase in the IOUT value), the controller jumps to the required power zone immediately.

A decrease in IOUT that indicates that the controller needs to switch into a higher power zone number, the transition will be executed with a delay of 200 μs set by the phase shed delay configuration register. The value of the delay can be adjusted by the user in steps of 10 μs if required.

To avoid excessive ripple on the output voltage, all power zone changes are gradual and include all intermediate power zones between the current zone and the target zone set by the comparison of the output current with the $PHTH_X$ thresholds, each transition introducing a programmable 200 μs delay.

To avoid false changes from one power zone to another caused by noise or short IOUT transients, the comparison between IOUT and $PHTH_X$ threshold uses hysteresis. The switch to a lower power zone is executed if IOUT exceeds the $PHTH_X$ threshold values while a transition to a higher power zone number is only executed if IOUT is below $PHTH_X$−Hysteresis value. The hysteresis value is set to 0x44h and can be changed by the user by writing to the phase shedding configuration register. If a power zone/$PHTH_X$ threshold is disabled, the controller will skip it during the power zone transition process.

When PSI = Low and the user requires to change the power zone, the transition to the new power zone is identical to the transition process used when PSI is set to the Mid−state. The only exception is when the target power zone is disabled in automatic phase shedding mode. In this case, the controller will automatically enable the target power zone and allow the transition. When the controller is set to automatic phase shedding, the power zone will be automatically disabled.

VID Down Operation in Single Phase Mode

When VID Down change bit (0x31) is enabled and there is a fast VID down transition (REFIN down) detected in single phase operation power zone (Zone 3 or Zone 4), the controller will force all phases to turn on for 2 ms to protect the external power stage against damage from large discharging current and achieve fast and smooth VID down transition in the meantime.

Switching Frequency

A programmable precision oscillator is provided for the switching frequency. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the FSW pin. The FSW pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the resistor. Table 14 lists the switching frequencies that can be set using discrete resistor values for each phase configuration. Also, the switching frequency information is available in the FSW configuration register and it can be changed by the user by writing to the FSW configuration register.

Total Current Summing: IMON Sensing Method

The controller sums the phase currents from each current sense power stage device into a single total current signal (Figure 8). This signal is then used to generate the output voltage droop, total current limit, and the current monitoring output. The total current signal is the difference between CSCOMP and CSREF with CSREF connected to an external voltage bias as required by the power stage current sense output.

The DC gain equation for the current sensing is given by the following equation:

$$CSREF - CSCOMP = Iout \cdot Aips \cdot Rcssum \quad \text{(eq. 5)}$$

Where Aips is the current sense gain of the power stage.

Programming Load Line

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage if the load line is enabled.

$$V_{DROOP} = LLTH \cdot (CSREF - CSCOMP) \quad \text{(eq. 6)}$$

The load line Coefficient LLTH can be configured by I2C register 0x39 to 0% (default), 25%, 50%, 100%.

Programming IOUT

The IOUT pin sources a current in proportion to the total output current summed up through the current summing amplifier. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to system max current generates a 2 V signal on IOUT. A pull−up resistor to VCC can be used to offset the IOUT signal if needed.

$$Iout\_max \cdot Aips \cdot Rcssum = CSSUM - CSCOMP = CSREF - CSCOMP \quad \text{(eq. 7)}$$

As an example, if CSREF bias voltage is 1.3 V and the minimum summing amplifier output voltage is set to 0.3 V, the Aips x Rcssum has to be chosen to ensure Iout x Aips x Rcssum = CSREF − CSCOM always less than 1 V in all the normal operating conditions. Since the internal resistor Rcur is 100 kΩ, that means a less than 10 μA pulling through Rcur in the normal operating conditions. For a 2 V maximum output voltage of IOUT pin, the shunt resistor Riout can be calculated by the following equation:

$$Riout = \frac{2V}{10\ \mu A \cdot 10} = 20\ k\Omega \quad \text{(eq. 8)}$$

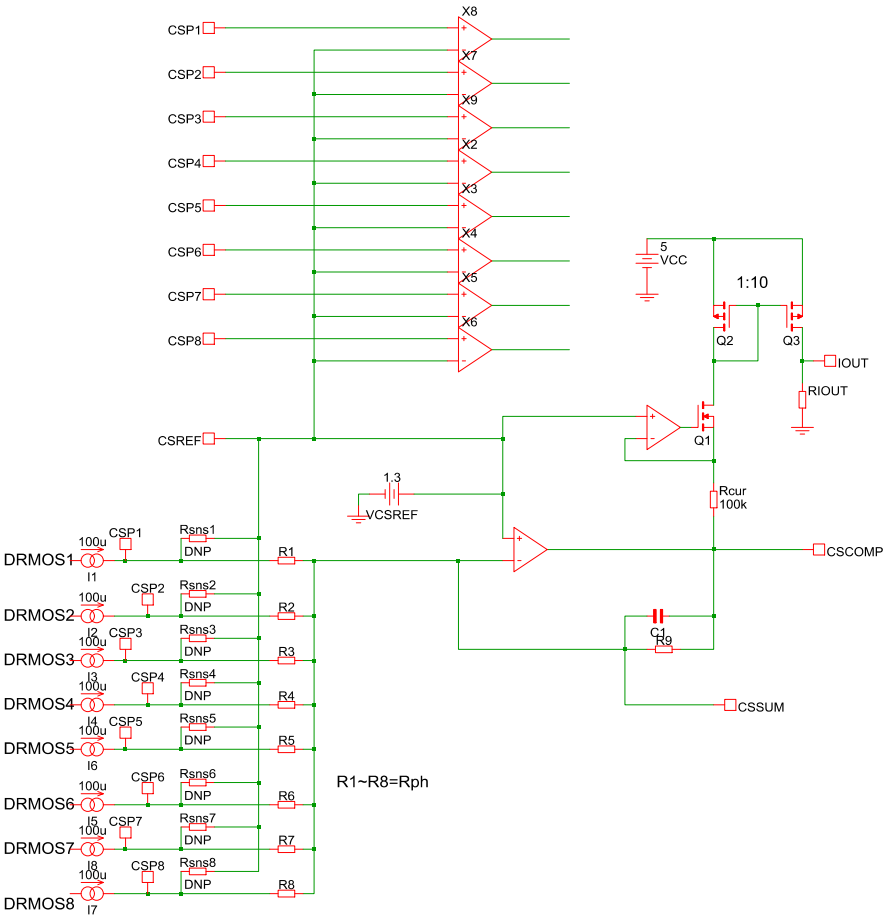


Figure 8. Total Current Summing Amplifier, DRMOS IMON Sensing

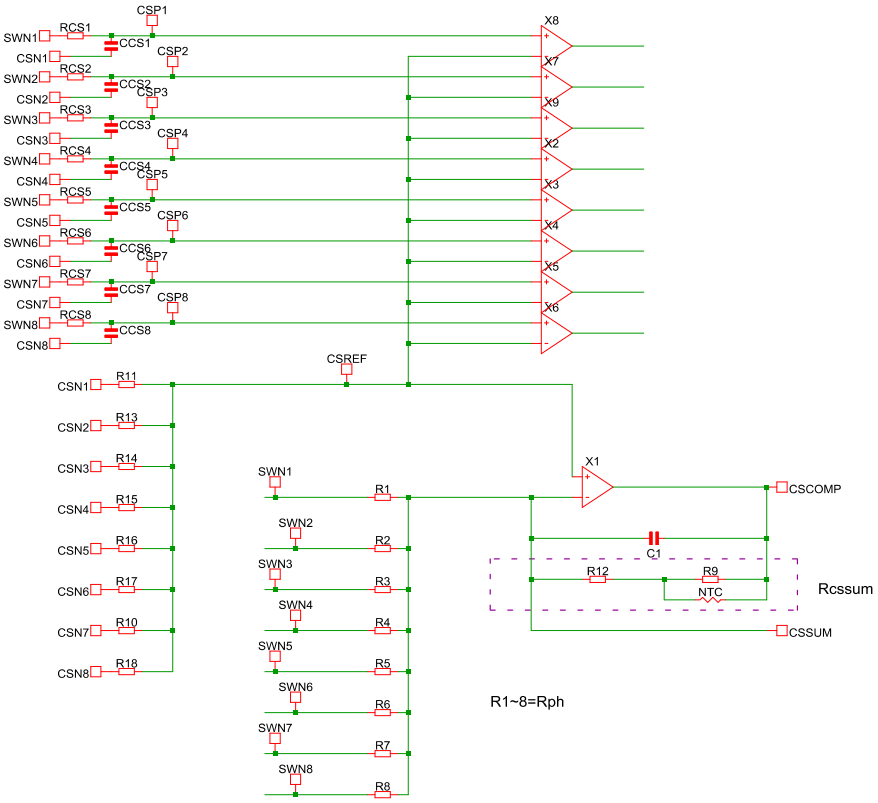


Figure 9. Total Current Summing Amplifier, DCR Sensing Example

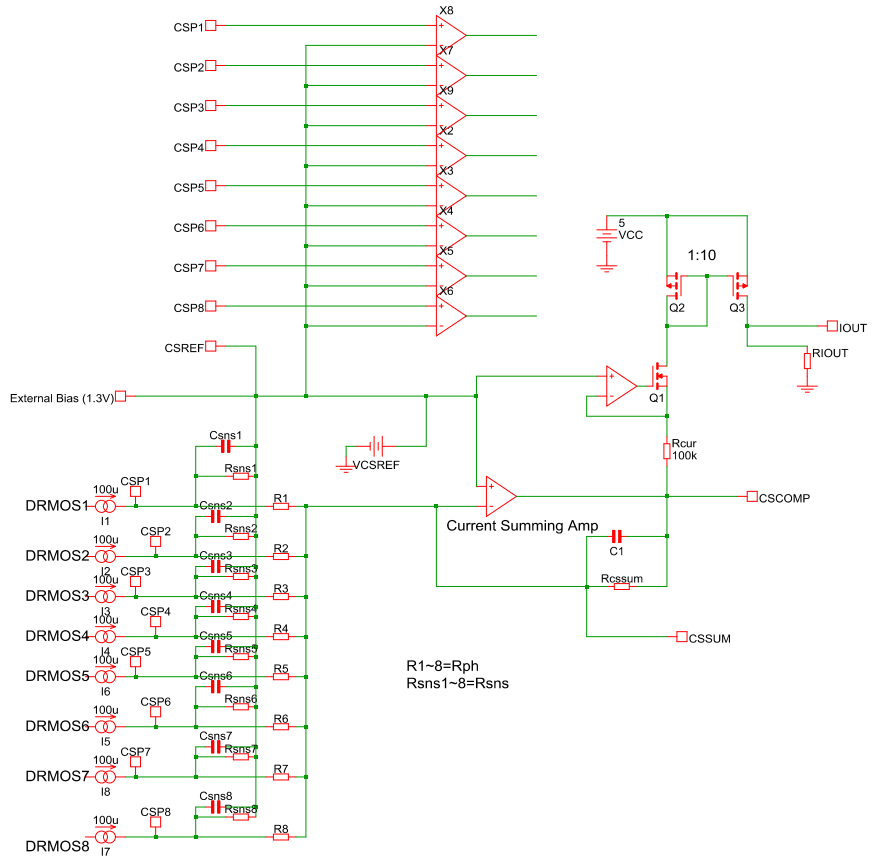


Figure 10. Total Current Summing Amplifier, Pseudo DCR Sensing Example

Total Current Summing: DCR or Pseudo DCR Methods

Two current summing methods in Figure 9, 10 are similar, they both convert the current signals drop across inductor DCR or DRMOS IMON current signal across a low value resistor to low impedance voltage signals and then sums them up with the current summing amplifier.

For DCR method,

$$CSREF - CSCOMP = Iout \cdot DCRL \cdot Rcssum/Rph \quad \text{(eq. 9)}$$

Where Rcssum = Rcs2 + Rcs1 // NTC, and the pole frequency of CSCOMP filter needs to be selected to be equal to the zero frequency from the inductor DCRL, or Rcssum * C1 = L / DCRL to recover the inductor DCR drop current signal.

For Pseudo DCR method,

$$CSREF - CSCOMP = Iout \cdot Aips \cdot Rsns \cdot Rcssum/Rph \quad \text{(eq. 10)}$$

Where Aips is the current sense gain of the power stage, and Aips * Rsns = DCRps is the equivalent DCR.

The selection of IOUT resistor, and DROOP configuration are similar to the IMON sensing method in previous sections.

Programming the Current Limit ILIM

By default, per phase current limit threshold is programmed through an external shunt resistor of the ILIM pin on the fly.

$$RILIM = \frac{perphase\_CLIM \cdot DCRps \cdot 6}{10\ \mu A} \quad \text{(eq. 11)}$$

Where DCRps is the equivalent DCR of the power stage, it can be inductor current sensing (DCRL) or DRMOS IMON sensing (Aips * Rpu) or DRMOS pseudo DCR sensing (Aips* Rsns).

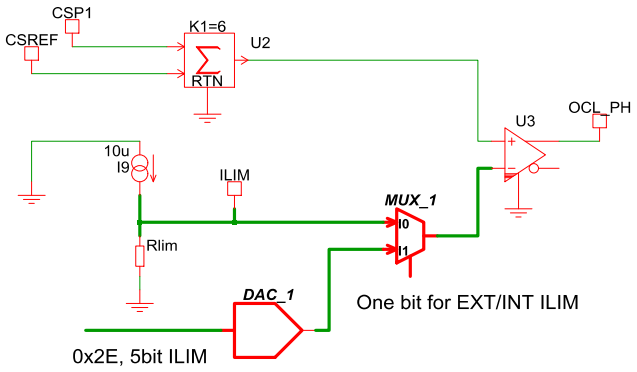


Figure 11. External / Internal ILIM Setting

During power on, a 10 μA current is sourced from ILIM pin to generate ILIM voltage, it is sampled and stored into register 0x2D on the fly. As an option, the ILIM threshold can also be configured through an internal register 0x2E. The external ILIM voltage ranges from 0 V to 2 V. Internal ILIM value controlled by a 5 bit register (0x2E) has a range from 0.2 V to 1.75 V. One ILIM configuration bit in register 0x46 and 0x47 determines whether the external resistor value or internal register value is selected.

Protections

TMON Monitoring

External power stages can send signals with its own temperature information or other fault information through TMON pin. The TMON signal proportional to the corresponding power stage temperature usually ranges from 0 V to 2 V. When the power stage device is over heated or under other fault conditions, the signal will be pulled high to across TMON trigger threshold (0x4A, 2.0 V by default), NCP81610 will be able to detect this fault and force the system into two different subsequent states based on the TMON configuration register setting: latch up(by default), or timer based hiccup mode. The TMON fault can also be masked through register 0x22. Once masked, the controller will ignore TMON warning from the power stages.

Overcurrent Limiting (OCL) and Undervoltage Protection (UVP)

The device incorporates a per phase overcurrent limiting (OCL) mechanism to limit per phase current and the energy transferred from input to the output to protect against damage due to an over current event. The current limit threshold can be programmed with a shunt resistor on ILIM pin, as shown in the Programming the Current Limit ILIM section.

By default, OCL will always be functional, a large overcurrent event will pull the output below the Under Voltage Protection threshold (UVP) or 400 mV below REFIN to enforce a system latch up. Once latched up, the system will remain disabled until the EN pin is toggled.

VOCL_min is a threshold level to allow the OCL function to be temporarily disabled when the output voltage is below the threshold; by default VOCL_min function is disabled. If the VOCL_min function is enabled during a current limiting event, the output will droop to the VOCL_min threshold if UVP is disabled or VOCL_min is set to above UVP threshold, OCL function will be disabled for a 2ms period to allow the system to go back to output voltage regulation. It is recommended that the system designer be aware of this over load condition to avoid per phase current exceeding the inductor saturation current.

VOCL_min threshold can be configured through the I^2C interface with a range of 0.2 V to 1.3 V and a 35 mV step resolution.

Latched Mode Over−Current Protection (OCP)

To prevent catastrophic system failure, NCP81610 is able to detect the total output current exceeding the overall current limit and force the chip to latch up. When current summing amplifier has its output CSCOMP voltage droop to less than 225 mV (CLIM), the system is considered as total current OCP and enter latched mode protection

immediately with all the PWMs going to the mid−state, toggling EN is required to restart the system.

Under Voltage Lock−Out (VCC UVLO)

VCC is constantly monitored for the under voltage lockout(UVLO). During power up the VCC pin are monitored Only after VCC exceeds its UVLO threshold will the full circuit be activated and ready for the soft start ramp.

Over Voltage Protection

An output voltage monitor is incorporated into the controller. During normal operation, if the output voltage is 500 mV over the REFIN value, the PGOOD pin will be pulled low, the DRON will assert low and the PWM outputs are set low. The OVP limit will be clamped at 2 V if OVP is disabled. The output will remain disabled until the EN pin is toggled.

VRMP (Line Input) Protection

A line input voltage monitor is incorporated into the controller. During normal operation, if the line voltage is below the VRMP under voltage threshold (2.5 V), the system will be latched up. The output will remain disabled until the EN pin is toggled.

Over Temperature Shutdown (TSD)

NCP81610 constantly monitors its own junction temperature during operation. If its temperature is over 150°C, an over−temperature fault will be reported. The system will either latch up, or enter into a timer based hiccup mode based on internal register (0x4B) settings.

Table 5. REGISTER MAP

Address	R/W	Default Value	Description	Notes:
0x20	R/W	0xFF	IOUT_OC_WARN_LIMIT	
0x21	R	0x00	STATUS BYTE	
0x22	R/W	0x00	FAULT MASK	
0x23	R	0x00	STATUS Fault	
0x24	R	0x00	STATUS Warning	
0x26	R	0x00	READ_IOUT	
0x27	R	0x1A	MFR_ID	
0x28	R	0x10	MFR_MODEL	
0x29	R		MFR_REVISION	
0x2A	R/W	0x00	Lock/Reset	
0x2B	R	0x00	Soft Start status	
0x2C	N/A	0x00	Soft Start configuration	
0x2D	R		OCL status	
0x2E	R/W	0x00	OCL configuration	
0x2F	R		Switching frequency status	
0x30	R/W	0x00	Switching frequency configuration	
0x31	R/W	0x01	VID_DOWN enable	
0x32	R		PSI status	
0x33	R		Phase Status	
0x34	R/W	0x1F	LPC_Zone_enable	
0x35	R		LPC status	
0x36	R/W	0x03	LPC configuration	
0x38	R		LL status	
0x39	R/W	0x03	LL configuration	Default: Load disabled
0x3A	RW	0x00	PHTH1 configuration	
0x3B	R		PHTH1 status	
0x3C	R/W	0x00	PHTH2 configuration	
0x3D	R		PHTH2 status	

Table 5. REGISTER MAP (continued)

Address	R/W	Default Value	Description	Notes:
0x3E	R/W	0x00	PHTH3 configuration	
0x3F	R		PHTH3 status	
0x40	R/W	0x00	PHTH4 configuration	
0x41	R		PHTH4 status	
0x44	R/W	0x08	Phase shedding hysteresis	
0x45	R/W	0x14	Phase shedding delay	
0x46	R/W	0x00	Second function configuration register latch A	
0x47	R/W	0x00	Second function configuration register latch B	
0x48	R		READ_VOUT	
0x49	R		READ_TMON	
0x4A	R/W	0x00	TMON_RESPONSE CONFIG	
0x4B	R/W	0x00	TSD_enable TSD_fault response	
0x4C	R/W	0x00	ZCD_CONFIG	
0x4D	R/W	0x00	ZCD_USER_TRIM	
0x4E	R/W	0x00	VOCL_min: Threshold to disable OCL VOCL_min enable	
0x4F	R/W	0x00	OVP CONFIGURATION	
0x50	R/W	0x00	UVP CONFIGURATION	
0x51	R/W	0xFF	TMON WARNING CONFIGURATION	
0x52	R/W	0x00	CLEAR REG	
0x53	R/W	0x00	CONFIGURATION AUX	

IOUT_OC_WARN_LIMIT Register (0x20)

8 bit register sets the threshold for IOUT voltage output and usually it is to monitor the total current. Once the READ_IOUT register value exceeds this limit, the IOUT_OC bit will be set in the STATUS BYTE register (0x21) and an ALERT is generated. Its default value is 0xFF.

STATUS BYTE Register (0x21)

Table 6. STATUS BYTE REGISTER SETTINGS

Bits	Name	Description
7	TMON	This bit gets set whenever TMON is over its set threshold.
6	TSD	This bit gets set whenever NCP81610 exceeds its thermal shutdown temperature.
5	VOUT_OV	This bit gets set whenever the NCP81610 goes into OVP mode
4	IOUT_OC	This bit gets set if READ_IOUT value is over the IOUT_OC_WARN_LIMIT register value
0:3	Reserved	N/A

Fault Mask Register (0x22)

Table 7. FAULT MASK REGISTER SETTINGS (DEFAULT 0X00)

Bits	Name	Description
7	Reserved	
6	VRMP_UV	Set to 1 means VRMP(VIN) under voltage will not trigger a latchup event but the fault will be reported in the fault status register
5	TMON	Set to 1 means TMON fault will not trigger a latchup or hiccup event but the fault will be reported in the fault status register
4	TSD	Set to 1 means TSD fault will not trigger a latchup or hiccup event but the fault will be reported in the fault status register
3	CLIM	Set to 1 means CLIM_fault will not trigger a latchup or hiccup event but the fault will be reported in the fault status register
2	per phase ILIM	Set to 1 means OCL per phase per phase current limiting function is disabled.
1	OVP	Set to 1 means OVP will not trigger a latchup event but the fault will be reported in the fault status register
0	UVP	Set to 1 means UVP will not trigger a latchup event but the fault will be reported in the fault status register

STATUS Fault Register (0x23)

Table 8. STATUS FAULT REGISTER SETTINGS

Bits	Name	Description
7	Reserved	
6	VRMP_UV_fault	VRMP (VIN) under voltage
5	TMON_fault	TMON over threshold
4	TSD_fault	NCP81610 over temperature
3	CLIM_fault	CLIM fault
2	Per phase_ILIM_fault	Per phase current limiting (of any phase)
1	OVP_fault	Overvoltage fault
0	UVP_fault	Undervoltage fault

STATUS Warning Register (0x24)

Table 9. STATUS WARNING REGISTER SETTINGS

Bits	Name	Description
7:1	Reserved	N/A
0	IOUT Overcurrent Warning	This bit sets if IOUT is over the warning value set by 0x20

READ_IOUT Register (0x26)

Read back output current. ADC conversion 0xff = 2 V on IOUT pin which should equate to max current.

Lock/Reset Register (0x2A)

Table 10. LOCK/RESET REGISTER SETTINGS

Bits	Name	Description
7:2	Reserved	N/A
1	Software reset	Reserved
0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the NCP81610 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings (Lockable).

Soft Start Status and Configuration Register (0x2B, 0x2C)

These registers contain the values that set the slew rate of the output voltage during power−up. When power on, the controller reads the value of the resistor connected to the PWM8/SS pin and sets the slew rate. The codes corresponding to each resistor setting are shown in Table 11**.** The soft start timer can be configured through 0x2C with 4bit resolution. One bit in control registers 0x46, 0x47 needs to be set to select internal soft start settings.

Table 11. SOFT START STATUS AND CONFIGURATION REGISTER SETTINGS

t_{RAMP} Resistor (kΩ)	Bits	Name	Value	t_{RAMP} (ms), REFIN = 1 V	t_{RAMP} (ms), REFIN = 0.8 V
–	7:4	Reserved	N/A	N/A	N/A
10	3:0	T_Ramp	0000	0.15	0.12
14.7			0001	0.3	0.24
20			0010	0.45	0.36
26.1			0011	0.6	0.48
33.2			0100	0.75	0.6
41.2			0101	0.9	0.72
49.9			0110	1	0.8
60.4			0111	2	1.6
71.5			1000	3	2.4
84.5			1001	4	3.2
100			1010	5	4
118.3			1011	6	4.8
136.6			1100	7	5.6
157.7			1101	8	6.4
182.1			1110	9	7.2
249			1111	10	8

OCL_ILIM Status Register and Configuration Register (0x2D, 0x2E)

These registers contain per phase current limit (OCL_ILIM) status and configuration information. By default, a 10 μA constant current will be sourced to the external ILIM resistor and read back the OCL_ILIM threshold level on the fly. OCL_ILIM threshold can also be dynamically configured by 0x2E register with 5bit resolution. One bit in registers 0x46, 0x47 needs to be set to select internal OCL setting shown in Table 13. When one phase is in OCL mode, the corresponding register bit will be set in 0x2D.

Table 12. OCL_ILIM STATUS REGISTER SETTINGS (0X2D)

Bits	Name	Description
7:0	Per phase OCL	Bit 7: Phase 8 current limit triggered. . . . Bit 0: Phase 1 current limit triggered.

Table 13. OCL_ILIM CONFIGURATION REGISTER SETTINGS (0X2E)

Bits	Name	Description
7:5	Reserved	N/A
4:0	Per phase OCL configuration	Configure the threshold for per phase current limit. 0x00: 0.2 V 0x01: 0.25 V … 0x1F: 1.75 V

Switching Frequency Status and Configuration Registers (0x2F, 0x30)

These registers contain the values that set the switching frequency of the controller When power on, the controller reads the value of the resistor connected to the FSW pin and sets the switching frequency according to Table 14.The codes corresponding to each setting are also shown in Table 14**.**

The switching frequency configuration register allows the user to dynamically change the switching frequency through the I^2C interface provided that the FSW bits from the second function configuration registers A and B (0x46, 0x47) are set.

Table 14. SWITCHING FREQUENCY STATUS AND CONFIGURATION REGISTER SETTINGS

FSW Pin Resistor Value (kΩ)	Bits	Value		Switching Frequency (kHz)							
		Status Register	Configuration Register	8 Phase	7 Phase	6 Phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
	7:5	Reserved	Reserved	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	4:0	00000 (default)	00000	221	253	295	355	221	293	223	232
		–	00001	244	276	330	399	244	329	243	252
14.7		00010	00010	266	309	355	425	266	358	264	272
		–	00011	293	327	387	460	293	381	294	297
20		00100	00100	307	351	412	501	307	407	317	322
		–	00101	333	384	441	542	333	450	335	340
26.1		00110	00110	351	409	480	561	351	480	352	361
		–	00111	373	431	499	615	373	510	380	385
33.2		01000	01000	394	451	528	639	394	530	399	413
		–	01001	421	481	559	676	421	562	420	435
41.2		01010	01010	449	495	593	725	449	600	436	456
		–	01011	469	525	612	746	469	614	454	478
49.9		01100	01100	479	563	639	757	479	631	483	500
		–	01101	509	570	681	799	509	663	508	509
60.4		01110	01110	518	588	697	831	518	688	526	518
		–	01111	543	617	722	874	543	722	543	540
71.5		10000	10000	581	665	779	930	581	789	583	578
		–	10001	649	718	881	1043	649	859	656	638
84.5		10010	10010	708	790	937	1129	708	930	698	698
		–	10011	751	868	1010	1211	751	1010	771	758
100		10100	10100	799	918	1073	1278	799	1095	807	818
		–	10101	866	1003	1136	1372	866	1147	860	878
118.3		10110	10110	919	1025	1220	1449	919	1233	899	938
		–	10111	964	1111	1297	1533	964	1260	950	972
136.6		11000	11000	993	1140	1339	6716	993	1341	1003	1014
		–	11001	1059	1198	1438	1687	1059	1372	1052	1067
157.7		11010	11010	1098	1262	1485	1734	1098	1450	1096	1106
		–	11011	1141	1295	1533	1821	1141	1539	1154	1155
182.1		11100	11100	1200	1338	1587	7530	1200	1619	1205	1201
		–	11101	1236	1405	1608	1954	1236	1618	1227	1245
249		11110	11110	1291	1459	1707	2012	1291	1674	1274	1280
		–	11111	1312	1493	1724	2096	1312	1724	1316	1330

VID DOWN Enable Register (0x31)

One control bit to enable or disable VID DOWN phase operation change during DCM mode.

Table 15. STATUS BYTE REGISTER SETTINGS

Bits	Name	Description
7:1	Reserved	N/A
0	VID DOWN enable	0: VID DOWN change disabled 1 (default): VID DOWN change enabled

PSI Status Register (0x32)

The PSI status register provides the information regarding the current status of the PSI pin though the I^2C interface as shown in Table 16.

Table 16. PSI STATUS REGISTER SETTINGS

Bits	Name	Description
7:2	Reserved	N/A
1:0	PSI input level	00 = PSI MID (Auto PSI)
		01 = PSI LOW
		10 = PSI HIGH

Phase Status Register (0x33)

The Phase Status register provides the information about the status of each of the eight available phases as shown in Table 17.

Table 17. PHASE STATUS REGISTER SETTINGS

Bits	Name	Description
7	Phase 8	0 = Disabled
		1 = Enabled
6	Phase 7	0 = Disabled
		1 = Enabled
5	Phase 6	0 = Disabled
		1 = Enabled
4	Phase 5	0 = Disabled
		1 = Enabled
3	Phase 4	0 = Disabled
		1 = Enabled
2	Phase 3	0 = Disabled
		1 = Enabled
1	Phase 2	0 = Disabled
		1 = Enabled
0	Phase 1	0 = Disabled
		1 = Enabled

LPC_Zone_Enable Register (0x34)

The LPC_Zone_enable register allows the user to enable or disable power zones while the controller has the PSI set low using the I^2C interface as shown in Table 18.

Table 18. LPC_ZONE_ENABLE REGISTER SETTINGS

Bits	Name	Description
7:5	Reserved	N/A
4	Zone 5	0 = Disabled
		1(default) = Enabled
3	Zone 4	0 = Disabled
		1(default) = Enabled
2	Zone 3	0 = Disabled
		1(default) = Enabled
1	Zone 2	0 = Disabled
		1(default) = Enabled
0	Zone 1	0 = Disabled
		1(default) = Enabled

LPC Status and Configuration Registers (0x35, 0x36)

These registers contain the values that set the operating power zone when the PSI pin is set low. When power on, the controller reads the value of the resistor connected to the PWM6/LPC1 and PWM5/LPC2 pins and sets the power zone according to Table 3. The codes corresponding to each setting are shown in Table 19**.**

The LPC configuration register allows the user to dynamically change the power zone (PSI = low) through the I^2C interface provided that the LPC bits from the second function configuration registers A and B (0x46, 0x47) are set. The achievable power zone settings are listed in Table 19.

Table 19. LPC STATUS AND CONFIGURATION REGISTER SETTINGS

Bits	Name	Value	Level
7:6	Reserved	N/A	N/A
5:3	LPC1 configuration	000 (default)	0
		001	1
		010	2
		011	3
		100	4
		101 = Reserved	N/A
		111 = Reserved	N/A
2:0	LPC2 configuration	000 (default)	0
		001	1
		010	2
		011	3
		100*	3
		101 = Reserved	N/A
		110 = Reserved	N/A
		111 = Reserved	N/A

Load Line Configuration Registers (0x39)

This register contains the value that set the fraction of the externally configured load line (LL) to be used during the normal operation of the device. The codes corresponding to each setting are shown in Table 20. The LL configuration register allows the user to dynamically change the load line settings through the I^2C. By default, the load line is disabled.

Table 20. LL STATUS AND CONFIGURATION REGISTERS SETTINGS

Bits	Description
7:2	Reserved
1:0	00 = 100% of externally set load line
	01 = 50% of externally set load line
	10 = 25% of externally set load line
	11 (default) = 0% of externally set load line

PHTH1 to PHTH4 Configuration Registers (0x3A, 0x3C, 0x3E, 0x40)

These 8 bit registers contain the values that control the phase shedding thresholds and are active when the $PHTH_X$ bits from the second function configuration registers A and B (0x46 and 0x47) are set. These thresholds allow the user to dynamically change the thresholds through the I^2C interface. The values written to these registers should match the value of the READ_IOUT register (0x26) at the desired load current. If 0xFF is written to a register, the phase shedding threshold corresponding to that register is disabled.

PHTH1 to PHTH4 Status Registers (0x3B, 0x3D, 0x3F, 0x41)

These 8 bit registers contain the phase shedding threshold values set by the resistors connected to the $PHTH_X$ pins. The values of the thresholds are updated during the power on period. The resistor values should be chosen to ensure that the voltage drop across them developed by the 10 μA current sourced by the NCP81610 during power−up (EN set high) matches the value of the READ_IOUT register (0x26) at the desired load current. Setting the resistors to generate a voltage above 2 V will disable the $PHTH_X$ threshold for that pin.

Phase Shedding Hysteresis Register (0x44)

This register sets the hysteresis during a transition from a high count phase to a low count phase configuration. The hysteresis is expressed in codes (LSBs) of the $PHTH_X$ threshold values.

Phase Shedding Delay Register (0x45)

This register sets the delay during a transition from a high count phase to a low count phase configuration. The power−up default value is 200 μs (14H) and it can be dynamically changed in steps of 30 μs (1 LSB) through the I^2C interface.

Second Function Configuration Register Latch A and B Registers (0x46, 0x47)

These registers allow the user to select whether the second functions settings (FSW, Soft Start, OCL, LPC and $PHTH_X$) are controlled by the external resistors or the configuration registers (see Table 21). When power on and enabled (cold start), the default control mode for the functions is the external resistor. Switching between the two modes can be done by simply writing the appropriate byte (the same byte) to both registers (the order doesn't matter).

Table 21. SECOND CONFIGURATION LATCH REGISTER A AND B

Bits	Second Function Configuration Register	Description
7:6	Reserved	N/A
5	FSW	0 (default) = switching frequency set by external resistor
		1 (default) = switching frequency set by register 0x30
4	Reserve	Reserve
3	Soft Start Timer	0 (default) = soft start timer set by external resistor
		1 (default) = soft start timer set by register 0x2C
2	OCL_ILIM	0 (default) = per phase current limit set by external resistor
		1 = per phase current limit set by register 0x2E
1	LPC1,LPC2	0 (default) = low power zone set by external resistor
		1 = low power zone set by register 0x36
0	$PHTH_X$	0 (default) = set by external resistors connected between $PHTH_X$ pins and GND
		1 = set by registers 0x3A, 0x3C, 0x3E and 0x40

VMON Register (0x48)

8 bit regsister to monitor VSP − VSN differential voltage value (Max FFH, 2 V).

TMON External Power Stage Thermal Monitoring Register (0x49)

8 bit register to monitor external power stage thermal temperature (Max FFH, 2 V).

TMON Fault Response Configuration Register (0x4A)

Table 22. TMON CONFIGURATION THRESHOLD

Bits	Name	Description
7:1	Reserved	N/A
0	TMON fault response	0 (default): Latch response
		1: Hiccup mode

TSD Fault Threshold / Response Configuration Register (0x4B)

Table 23. TSD CONFIGURATION THRESHOLD

Bits	Name	Description
7:2	Reserved	N/A
1	TSD enable	0 (default): TSD disabled 1: TSD enabled
0	TSD fault response	0 (default): Latch response
		1: Hiccup mode

ZCD Configuration Register (0x4C)

Table 24. ZCD CONFIGURATION REGISTER

Bits	Name	Description
7:3	Reserved	N/A
2	ZCD PWM level configuration	0 (default): PWM = H/L
		1: PWM = H/M, PWM can go to Mid state
1	ZCD reset	Default 0: reset ZCD threshold
0	ZCD disable	0 (default): ZCD enabled 1: ZCD disabled

ZCD User Trim Register (0x4D)

Allow user to set their own ZCD threshold values.

Table 25. ZCD USER TRIM REGISTER

Bits	Name	Description
7:6	Reserved	N/A
5:0	Trim ZCD threshold	0x111111: +18.6 mV 0x100000: +0.6 mV 0x000000 (Default): 0 mV 0x000001: −0.6 mV 0x011111: −18.6 mV

VOCL_Min Configuration Register (0x4E)

VOUT per phase OCL disable threshold values relative to DIFFOUT. VOCL_min function can be disabled by bit 0.

Table 26. VOCL_MIN CONFIGURATION REGISTER

Bits	Name	Description
5:1	VOCL_min threshold	5 bit, with 35 mV resolution 00000 (default): 0.215 V 00001: 0.250 V … 11111: 1.3 V
0	VOCL_min enable	0 (default): VOCL_min disabled 1: VOCL_min enable

OVP Configuration Register (0x4F)

OVP can be changed by this register with 50 mV resolution.

Table 27. OVP_CONFIGURATION REGISTER

Bits	Name	Description
7:3	Reserved	
2:0	OVPth	000 (default): typ: 600 mV, min: 500 mV 001: +50 mV 010: +100 mV 011: +150 mV 100: OVP Clamped to 2.0 V 101: −50 mV 110: −100 mV 111: −150 mV

UVP Configuration Register (0x50)

UVP configuration can be changed by this register with 50 mV resolution.

Table 28. UVP_THRESHOLD REGISTER

Bits	Name	Description
7:3	Reserved	
2:0	UVPth	000 (default): max: −400 mV; typ: −500 mV 001: −50 mV 010: −100 mV 011: −150 mV 100: UVP disabled 101: +50 mV 110: +100 mV 111: +150 mV

TMON Warning Threshold Register (0x51)

TMON warning threshold is usually less than TMON fault threshold.

Table 29. TMON WARNING THRESHOLD REGISTER

Bits	Name	Description
7:0	TMON WARNING threshold	Default 0xFF or ~2.0 V, 0x00: 0 V 0x01: 0.008 V … 0x0F: 2.040 V

Clear_Reg Register (0x52)

Clear_reg register is used to reset the OCP_ILIM status register by transition from “0” to “1”.

Table 30. CLEAR_REG REGISTER

Bits	Name	Description
7:1	Reserved	N/A
0	Clear_Reg	Bit 0 Transition from 0 to 1 cause the reset of OCP_ILIM status register (0x2D). Please notice that this register remain writable even the lock bit has been set.

Auxiliary Configuration Register (0x53)

Table 31. AUXILIARY CONFIGURATION REGISTER

Bits	Name	Description
7:4	Reserved	N/A
3	SONIC_TMR_EN	0 (default): Ultrasonic timer disabled
		1: Ultrasonic timer enabled
2	I2C_or_fuse_sel	0 (default): select fuse settings 1: select I^2C settings
1	CLIM_sel	0 (default): CSCOMP <0.225 V trigger CLIM 1: CSREFE − CSCOMP >1.0 V trigger CLIM
0	TBD	TBD

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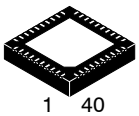
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

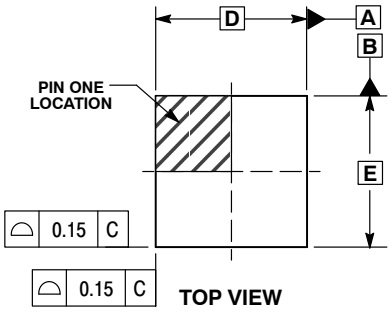
ON Semiconductor®

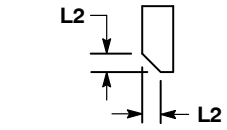
QFN40 5x5, 0.4P
CASE 485CR
ISSUE C

DATE 27 AUG 2013

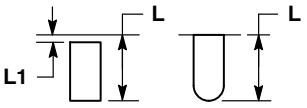


SCALE 2:1

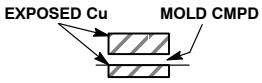




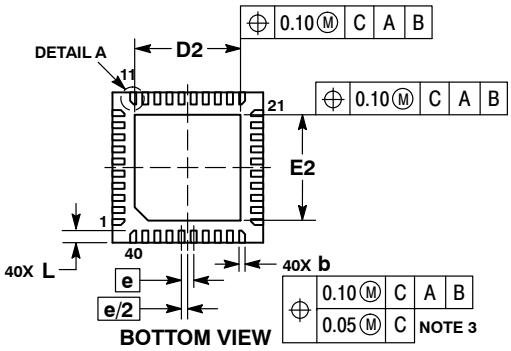
DETAIL A



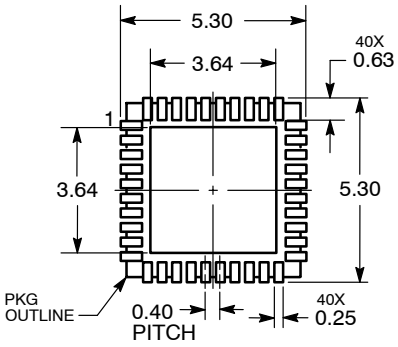
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



RECOMMENDED SOLDERING FOOTPRINT

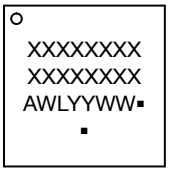


DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.40 BSC	
L	0.30	0.50
L1	---	0.15
L2	0.12 REF	

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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