MP175

700V, Non-Isolated, Offline Regulator, Up to 600mA Output Current

The Future of Analog IC Technology

DESCRIPTION

The MP175 is a primary-side regulator that provides accurate, constant voltage (CV) regulation without an optocoupler. The MP175 supports buck, buck-boost, boost, and flyback topologies. The MP175 has an integrated 700V MOSFET and high-voltage current source, and also has a fixed output option to further simplify the structure and reduce costs. The output voltage can also be adjusted for various applications.

The MP175 is a green-mode-operation regulator. Both the peak current limit and switching frequency decrease with decreasing load. This feature provides excellent efficiency at light-load condition and improves the overall average efficiency.

The MP175 has multiple protections features, including over-temperature protection (OTP), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), brown-out protection (BOP), and open-loop detection (OLD).

These features make the MP175 an ideal regulator for offline, low-power applications, such as home appliances and standby power.

The MP175 is available in a SOIC-8 package.

FEATURES

- Primary-Side CV Control, Supporting Buck, Buck-Boost, Boost, and Flyback Topologies
- Integrated 700V/4.5Ω MOSFET
- Internal 700V High-Voltage Current Source
- Fixed or Adjustable Output Options
- <30mW No-Load Power Consumption
- Up to 10W Output Power
- Maximum CCM Output Current up to 600mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- OTP, UVLO, OLP, SCP, BOP, OLD
- Available in a SOIC-8 Package

APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

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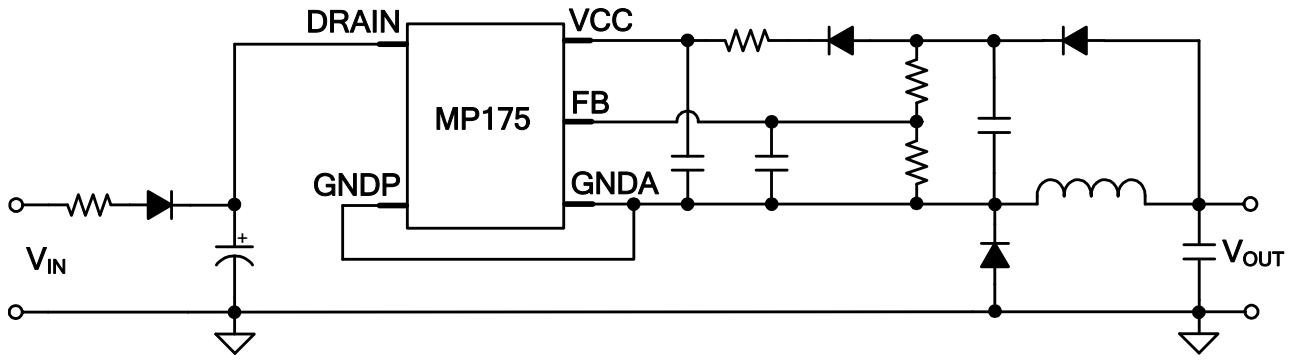
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP175GS	SOIC-8	*See Below*

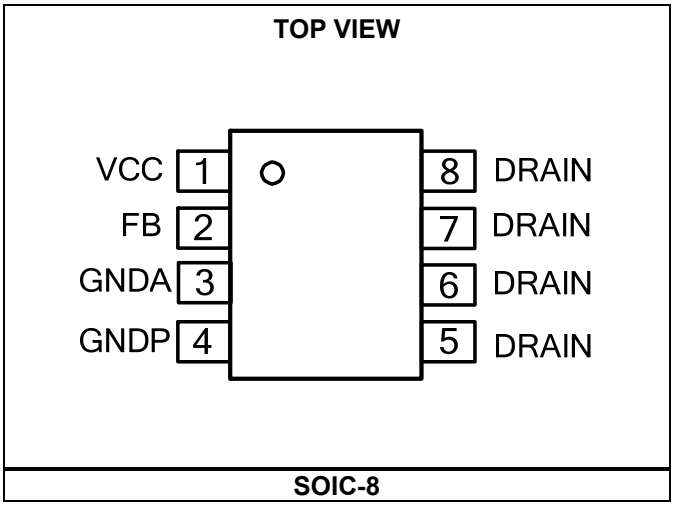
* For Tape & Reel, add suffix –Z (e.g.: MP175GS–Z)

TOP MARKING

MP175
LLLLLLLL
MPSYWW

MP175: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to GND ..... -0.3V to 700V
VCC to GND ..... -0.3V to 30V
FB to GND ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
SOIC-8 ..... 1.64W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to +150°C
ESD capability human body mode 2.0kV
ESD charged device model 2.0kV

Recommended Operating Conditions (3)

Operating junction temp. (T_J) ....-40°C to +125°C

THERMAL RESISTANCE (4) θ_{JA} θ_{JC}

SOIC-8	76	35	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowance continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowance power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 12V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Voltage Current Source and Internal MOSFET (DRAIN)						
Internal current-source regulator supply current	$I_{regulator}$	VCC = 4V, V_{DRAIN} = 100V	3	4.5	6	mA
DRAIN leakage current	I_{Leak}	V_{DRAIN} = 400V			40	µA
Breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	700			V
On resistance	R_{on}	T_J = 25°C		4.5	6.5	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator turns off	V_{HVoff}		8.4	9	9.6	V
VCC level (decreasing) where the internal regulator turns on	V_{HVon}		7.9	8.5	9.1	V
HV regulator on and off hysteresis			200			mV
VCC under-voltage lockout threshold	V_{CCL}		7	7.9	8.7	V
VCC level (decreasing) where the protection phase ends	VCC_{pro}			3.5	4	V
IC consumption (5)	I_{CC}	fs = 50kHz		920	1150	µA
		MOSFET on		900	1050	
		MOSFET off	220	310	400	
Internal IC consumption, under protection	I_{CCpro}			40	65	µA
Regulating voltage	V_{CCref}	FB open	16.7	17.4	18.1	V
Internal Current Sense						
Peak current limit	I_{Limit}	T_J = 25°C	1.02	1.1	1.18	A
Leading-edge blanking	t_{LEB1}			310		ns
SCP threshold	I_{SCP}	T_J = 25°C	135%	155%	175%	I_{Limit}
Leading-edge blanking for SCP	t_{LEB2}			250		ns
Feedback Input (FB)						
Minimum off time	t_{minoff}		11.6	14	16.6	µs
Maximum on time	t_{maxon}		29.5	34	39.5	µs
MOSFET turn-on threshold	V_{FB}		2.31	2.43	2.53	V
OLP counter				8192		Cycle
Open-loop detection	V_{OLD}		0.2	0.3	0.4	V
Thermal Shutdown						
Over-temperature protection threshold (5)				150		°C

NOTES:

5) Guaranteed by design.

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PIN FUNCTIONS

Pin # SOIC-8	Name	Description
1	VCC	**Control circuit power supply.** VCC is also the feedback input for the fixed output set-up.
2	FB	**Regulator feedback.**
3	GNDA	**Short to GNDP in the application.**
4	GNDP	**IC power ground.**
5 - 8	DRAIN	**Internal power MOSFET drain.** DRAIN is the high-voltage current source regulator input.

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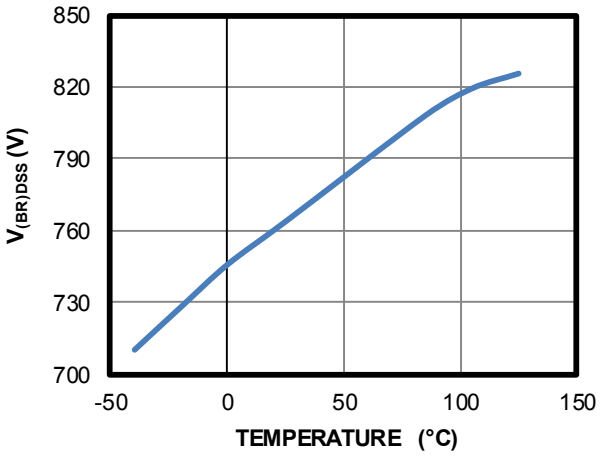
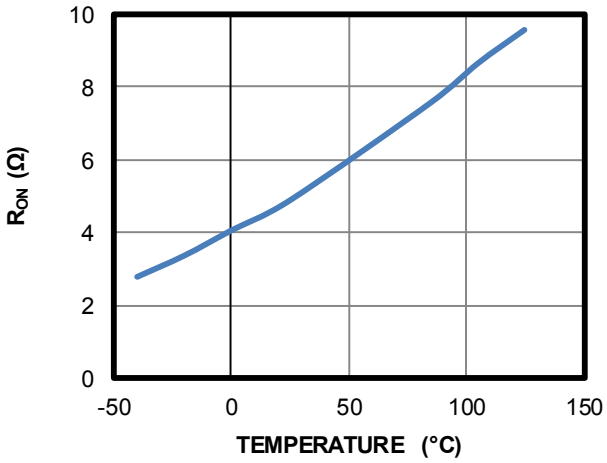
TYPICAL CHARACTERISTICS

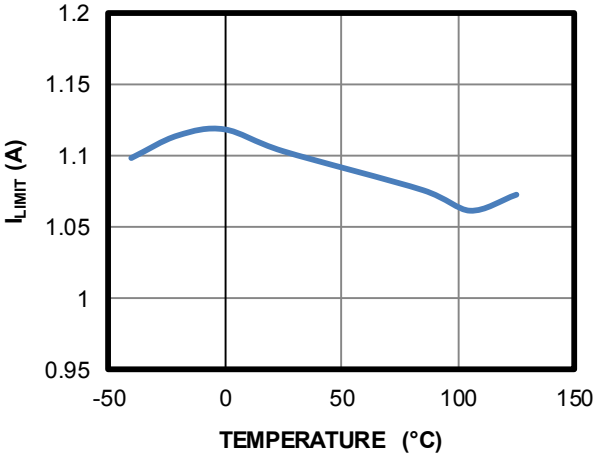
Breakdown Voltage vs. Temperature



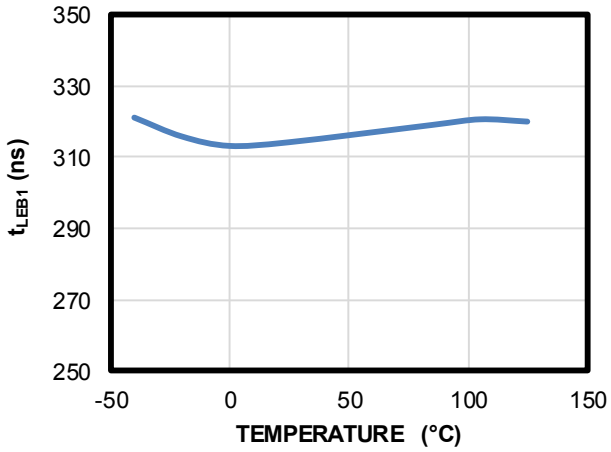
On Resistance vs. Temperature



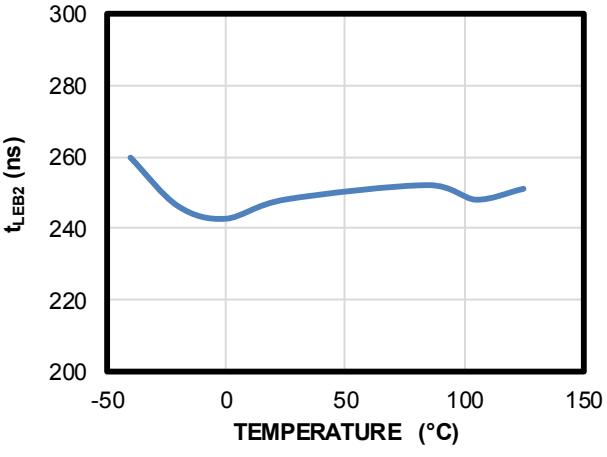
Peak Current Limit vs. Temperature



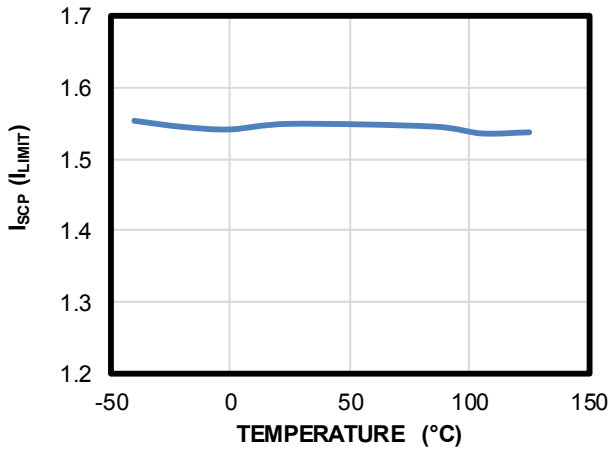
Leading-Edge Blanking vs. Temperature



Leading-Edge Blanking for SCP vs. Temperature



SCP Threshold vs. Temperature



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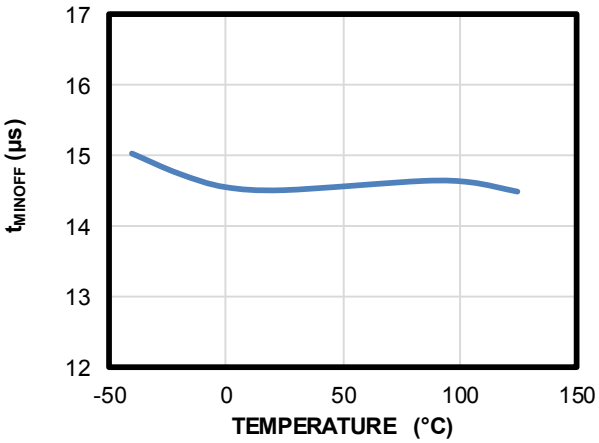
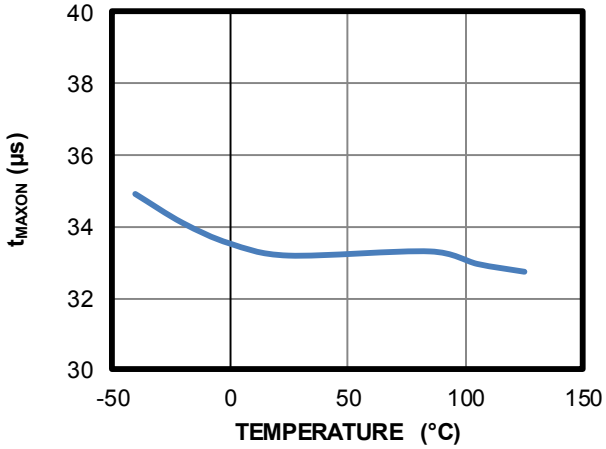
TYPICAL CHARACTERISTICS *(continued)*

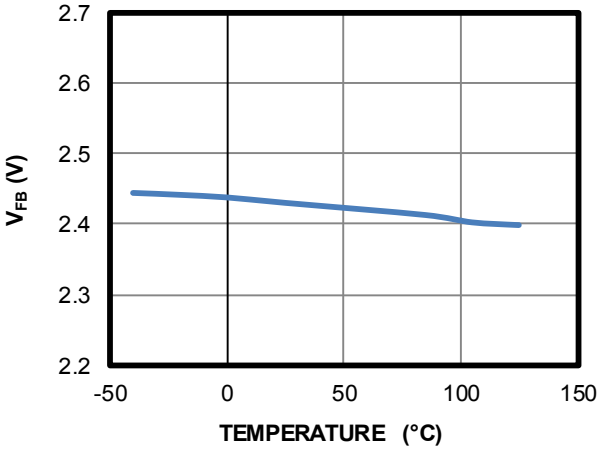
Minimum Off Time vs. Temperature



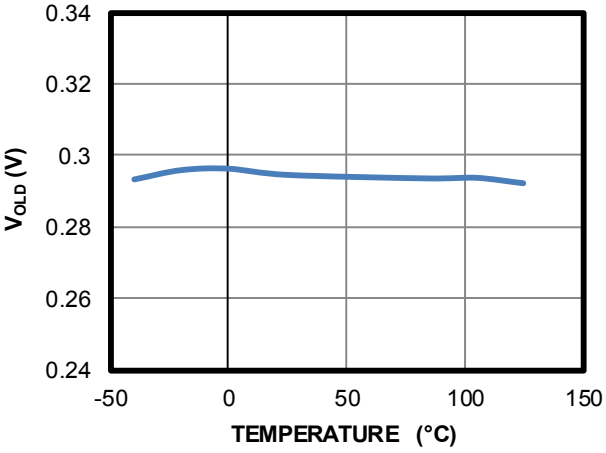
Maximum On Time vs. Temperature



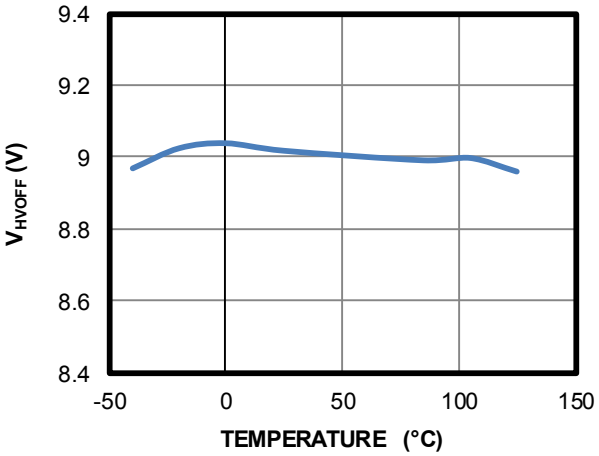
MOSFET Turn-On Threshold vs. Temperature



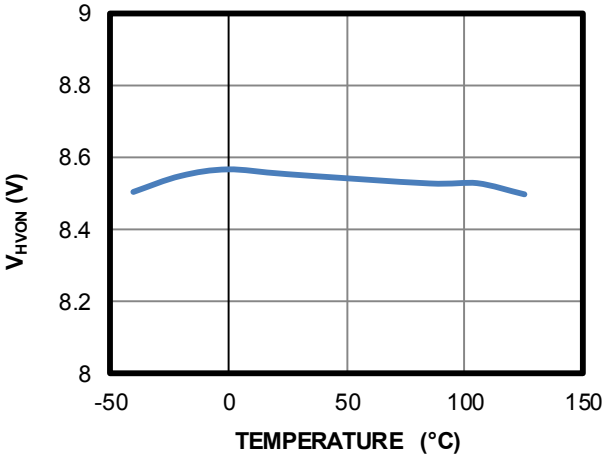
Open-Loop Detection vs. Temperature



VCC Level (Increasing) where the Internal Regulator Turns On vs. Temperature



VCC Level (Decreasing) where the Internal Regulator Turns Off vs. Temperature



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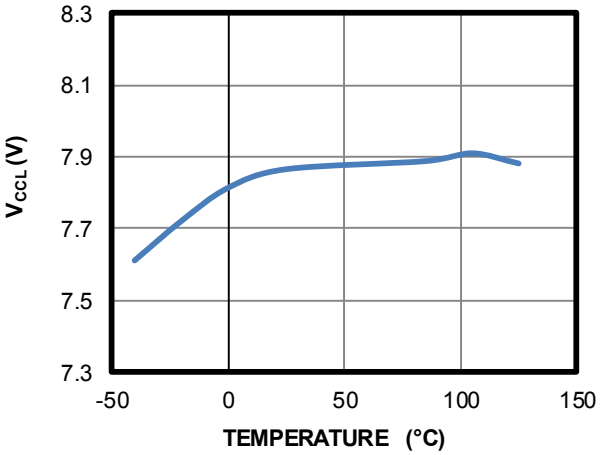
TYPICAL CHARACTERISTICS *(continued)*

VCC Under-Voltage Lockout Threshold vs. Temperature



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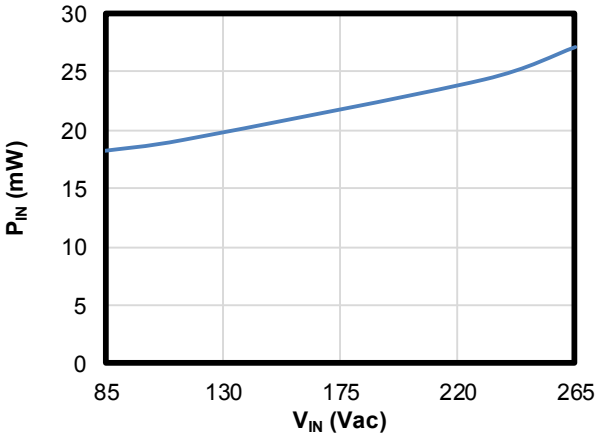
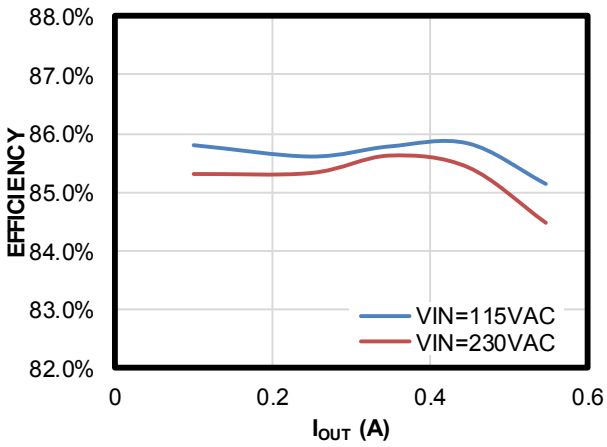
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested with the evaluation board in the Typical Application Circuits section. V_{IN} = 230VAC, V_{OUT} = 18V, I_{OUT} = 550mA, T_A = 25°C, unless otherwise noted.

No-Load Consumption



Efficiency



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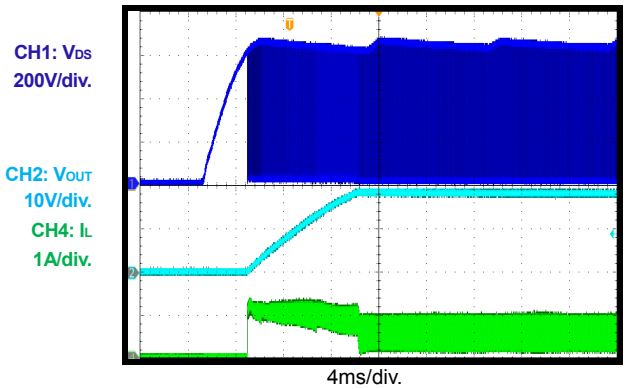
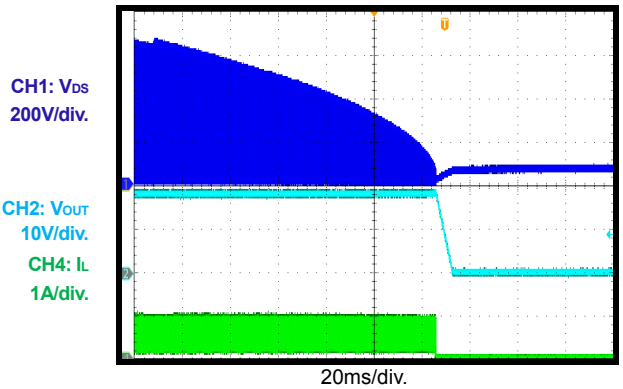
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested with the evaluation board in the Typical Application Circuits section. V_{IN} = 230VAC, V_{OUT} = 18V, I_{OUT} = 550mA, T_A = 25°C, unless otherwise noted.

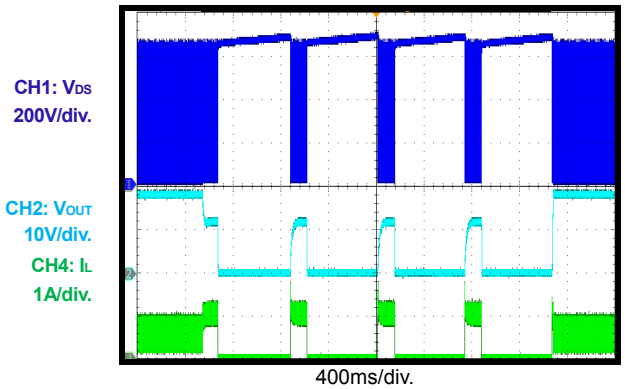
Power On



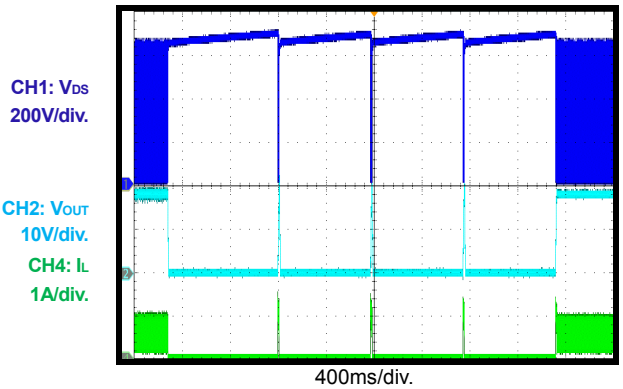
Power Off



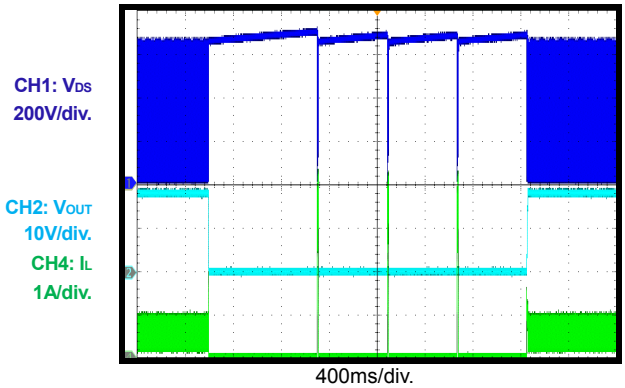
OLP entry and recovery



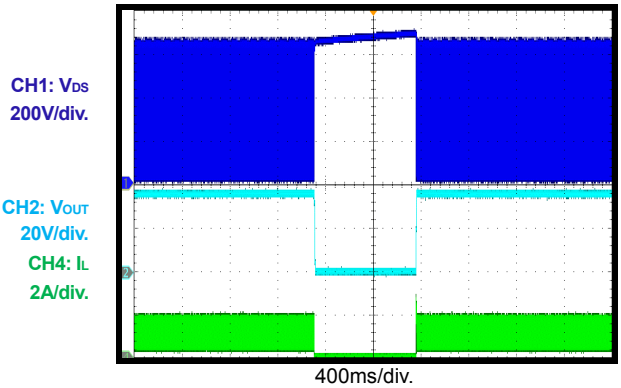
Open loop entry and recovery



SCP entry and recovery



OTP entry and recovery



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BLOCK DIAGRAM

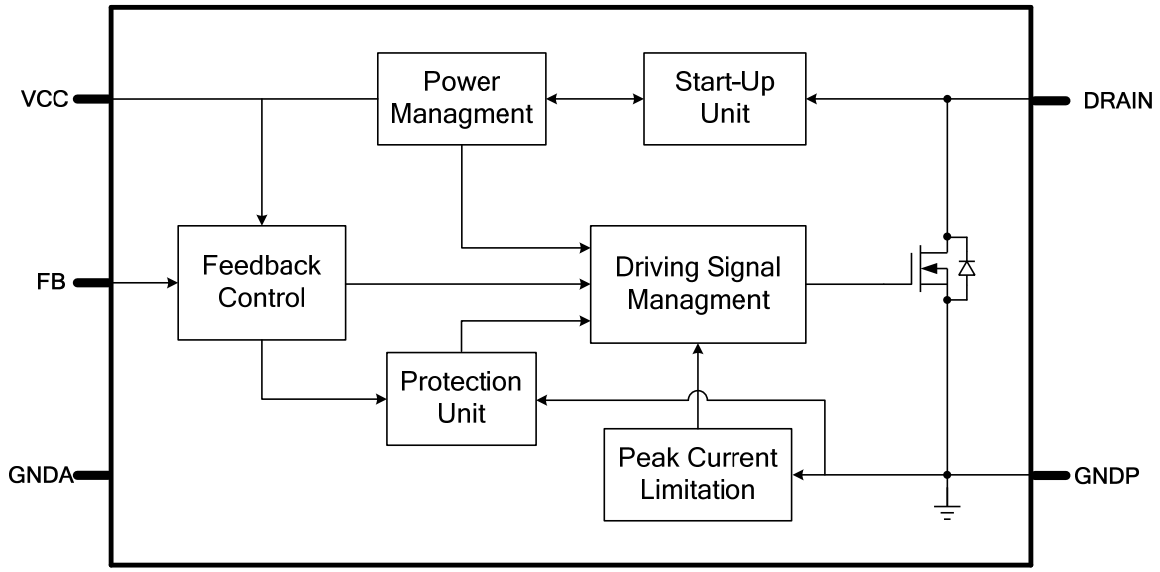

Figure 1: Functional Block Diagram

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OPERATION

The MP175 is a green-mode-operation regulator. The peak current limit and the switching frequency both decrease as the load decreases. As a result, the MP175 offers excellent light-load efficiency and improves average efficiency. The typical application diagram on page 1 shows that the regulator operates with a minimal number of external components. The MP175 incorporates multiple features described below.

Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage (HV) current-source regulator supplies the VCC from DRAIN. When VCC is charged to V_{HVoff}, the internal HV regulator is turned off, and the IC starts switching. If the VCC falls below V_{HVon}, the internal HV regulator turns on to charge the external VCC capacitor. This way, the MP175 is able to work with a very small VCC capacitor (in the low µF range).

Under-voltage lockout (UVLO), which stops switching when VCC is lower than V_{CCL}, prevents misbehaviors caused by insufficient supply voltage. The IC remains in shutdown mode until VCC is charged to V_{HVoff} again (see Figure 2).

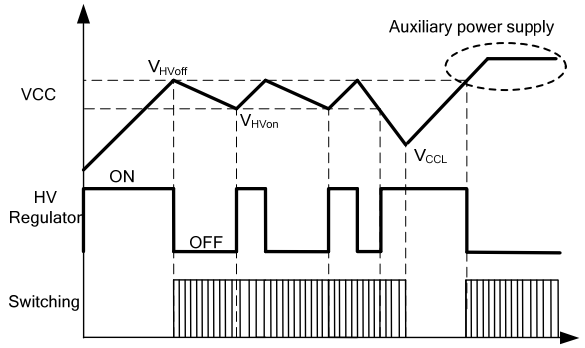

Figure 2: Start-Up and UVLO operation

Soft Start (SS)

A soft-start period occurs whenever the chip begins switching. This prevents the inductor current from overshooting.

The MP175 implements a soft start by decreasing the minimal off time gradually in eight steps. The sequence pattern in the soft-start phase is shown in Table 1.

During soft start, short-circuit protection (SCP), overload protection (OLP), open-loop detection (OLD), and brown-out protection (BOP) are disabled.

Table 1: Soft-Start Pattern

Step	Min off time (µs)	Cycles
#1	36	16
#2	36	16
#3	20	32
#4	20	64
#5	18	128
#6	14	128
#7	14	128
#8	13	128

Constant-Voltage (CV) Operation

The MP175 is designed to be a constant-voltage (CV) regulator, which regulates the output voltage by the feedback of either VCC or FB, depending on the external set-up.

The regulator operates as a fixed output by the internal feedback on VCC when FB is not connected to the external resistor divider.

The lower resistor of the internal feedback divider is 500kΩ, typically. As a result, when a feedback divider is connected to FB externally with a much smaller resistance, the internal feedback is overridden, so the MP175 output voltage is externally adjusted (see Figure 3).

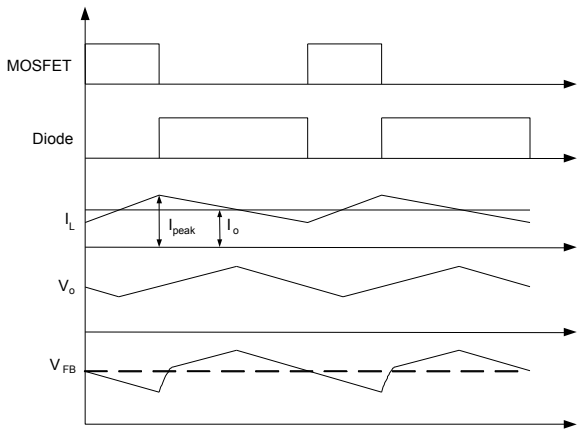

Figure 3: Constant-Voltage Regulation

As shown in Figure 3, the internal MOSFET is turned on when the feedback (FB) voltage is lower than the MOSFET turn-on threshold (V_{FB}) and is turned off based on the peak current limitation.

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V_{FB} is the reference voltage on FB. In this way, the feedback voltage is regulated at the reference voltage. The output voltage can be determined by Equation (1):

$$V_o = V_{FB} \times \frac{R_{up} + R_{low}}{R_{low}} \quad (1)$$

Frequency Foldback and Peak-Current Compression

Due to the constant voltage regulation scheme adopted by the MP175, the switching frequency of the HV regulator is decreased as the load reduces. As a result, the MP175 can achieve excellent efficiency at light-load conditions.

The switching frequency can be calculated approximately with Equation (2) for continuous conduction mode (CCM) and Equation (3) for discontinuous conduction mode (DCM):

$$f_s = \frac{(V_{in} - V_o)}{2L \times (I_{peak} - I_o)} \times \frac{V_o}{V_{in}} \quad (2)$$

$$f_s = \frac{2(V_{in} - V_O)}{L \times I^2_{peak}} \times \frac{I_o \times V_o}{V_{in}} \quad (3)$$

As the switching frequency decreases, the peak current limit is also reduced to minimize audible noise when the frequency drops down to the audible range. The peak current limit can be estimated with Equation (4):

$$I_{peak} = I_{limit} - (40mA/\mu s) \times (t_{off} - t_{off\,min}) \quad (4)$$

The minimum value of I_{peak} is limited internally.

Overload Protection (OLP)

The maximum output power of the MP175 is limited by the minimum off time and peak current limit. The MP175 is considered to be in an overload condition (OLP) when working under a minimum off time, which indicates a maximum switching frequency.

When the MP175 works at a minimum off time, the OLP counter begins counting the switching cycle. If the counter reaches 8192, OLP is triggered. This OLP counter duration helps prevent OLP from triggering falsely during start-up or during load transition.

The overload state is also affected by external setting, such as output voltage and inductor value, etc. Although this is not a very precise approach, it can act as a function to avoid overstress operation of the system. In order to improve robustness, it is recommended to apply MP175 in a scenario with Vo higher than 10V, in which case VCC can be supplied from output as well.

Short-Circuit Protection (SCP)

The MP175 monitors the peak current and shuts down when the peak-current rises above the SCP threshold. The power supply resumes normal operation when the fault condition is removed.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is triggered when the junction temperature exceeds the thermal shutdown threshold to prevent any thermal-induced damage.

Brown-Out Protection (BOP)

If the turn-on time reaches the maximum limitation for four consecutive cycles, BOP is triggered. BOP can prevent the MP175 from working under extremely low input voltages.

Open-Loop Detection (OLD)

If V_{FB} is lower than V_{OLD}, the IC stops switching, and a restart cycle begins. During soft start, OLD is blanked.

To use OLD, the feedback capacitor should be separated from the VCC capacitor. For circuit design recommendations, please refer to the feedback set-ups shown in the Application Information section on page 15.

OLD is disabled when the VCC capacitor acts as a feedback capacitor.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit prevents premature switching pulse termination due to a turn-on spike. Turn-on spikes are caused by parasitic capacitance and reverse-recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the internal MOSFET (see Figure 4).

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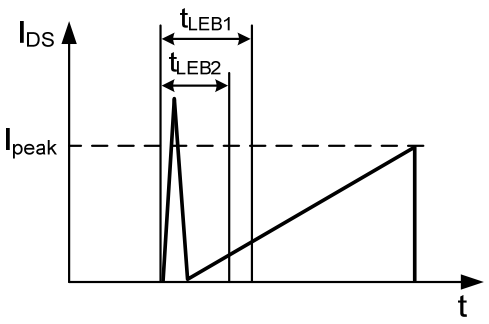

Figure 4: Leading-Edge Blanking

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 5 shows the typical DC bus voltage waveform of a half-wave rectifier and full-wave rectifier.

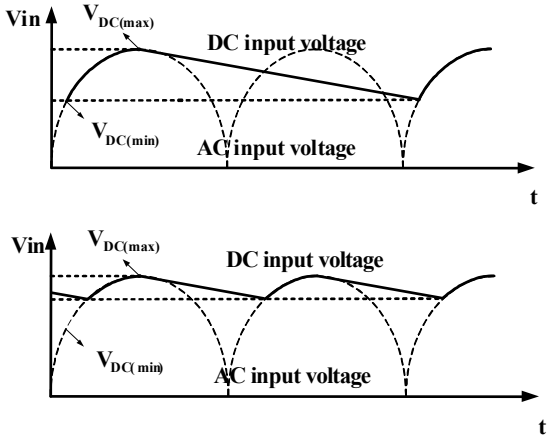

Figure 5: Input Voltage Waveform

Typically, the use of a half-wave rectifier requires an input capacitor rated at 3μF/W for the universal input condition. When using a full-wave rectifier, the input capacitor is chosen as 1.5 - 2μF/W for the universal input condition. A half-wave rectifier is recommended for <2W output applications. A full-wave rectifier is recommended for >2W output applications.

Avoid using an input capacitor that is too small, since it may not hold the DC voltage high long enough. A low DC input voltage can lead to bad thermal performance. If the input voltage is very low, the MOSFET on time may reach t_{maxon} and trigger BOP.

Selecting the Inductor

The MP175 has a minimum off-time limit that determines the maximum output power. Since the peak current limit is fixed, the maximum power increases as the inductance of the power inductor increases. Using a small inductance may lead to insufficient output power, but a larger inductance results in an inappropriate OLP point.

It is recommended to select an inductor with the minimum inductance value to meet the overload requirement. Tolerance of the peak-current limit and minimum off time should also be considered for mass production. The OLP point can be estimated with Equation (5) for CCM or Equation (6) for DCM:

$$P_{omax} = V_o \times (I_{Limit} - \frac{V_o \times t_{minoff}}{2L}) \quad (5)$$

$$P_{omax} = \frac{1}{2} L \times I_{Limit}^2 \times \frac{1}{t_{minoff}} \quad (6)$$

To reduce costs, use a standard, off-the-shelf inductor no less than the calculated value.

Freewheeling Diode

The diode should be selected based on the maximum input voltage and peak current.

Since the freewheeling diode's reverse recovery can affect efficiency and circuit operation in CCM, use an ultra-fast reverse recovery diode, such as the STTH2R06.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation (7) for CCM or Equation (8) for DCM:

$$V_{OUT\_ripple} = \frac{\Delta i}{8 f_s \times C_o} + \Delta i \times R_{ESR} \quad (7)$$

$$V_{OUT\_ripple} = \frac{I_o}{f_s \times C_o} \left(\frac{I_{peak} - I_o}{I_{peak}} \right)^2 + I_{peak} \times R_{ESR} \quad (8)$$

It is recommended to use low ESR electrolytic or ceramic capacitors to reduce the output voltage ripple, if necessary.

Feedback Set-Up

There are three kinds of feedback set-ups recommended for the MP175. Each set-up can be chosen according to cost and performance requirements. These feedback set-ups are shown in Figure 6, Figure 7, and Figure 8.

Figure 6 shows the typical external feedback circuit with the OLD function enabled. C1 is a dedicated feedback capacitor isolated from VCC by D2. In this way, the VCC operation will not interfere with the feedback operation. Both the VCC capacitor and feedback loop can be adjusted.

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The set-up shown in Figure 6 is recommended for most applications due to its high reliability and good performance.

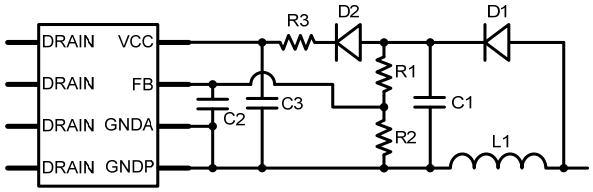

Figure 6: External Feedback Circuit with Dedicated Feedback Circuit

Figure 7 shows a typical external feedback circuit using the VCC capacitor for output voltage sampling. R1 and R2 compose a resistor divider for adjustable output voltage.

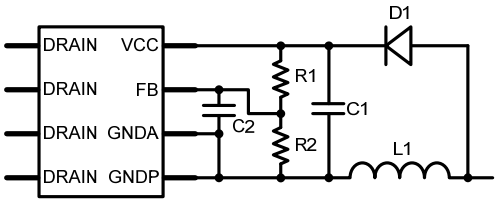

Figure 7: External Feedback Circuit

Figure 8 shows the typical internal feedback circuit. C1 is the VCC capacitor and is also used as a feedback capacitor. C2 and C3 are two small capacitors, which are used to achieve stable operation.

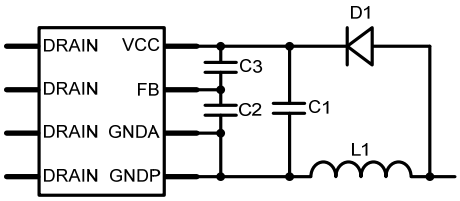

Figure 8: Internal Feedback Circuit

OLD is disabled in the set-ups shown in Figure 7 and Figure 8. After power-on, VCC is always above V_{CCL}, and V_{FB} is proportional to VCC due to the presence of an internal feedback resistor divider and cannot drop to V_{OLD}. However, the MP175 hiccups when the feedback circuit is open because OLP is triggered.

External Feedback Resistors

For adjustable output configurations, the divider's lower resistor value should not exceed 1/20 of the internal resistor divider's lower resistor. If large external resistors are preferred, the external resistor value should be adjusted to meet the output voltage target.

Feedback Capacitor

The feedback capacitor provides a sample-and-hold function for the output voltage regulation. In Figure 6, C1 is the dedicated feedback capacitor. The VCC capacitor is used as the feedback capacitor in Figure 7 and Figure 8.

Usually, a large feedback capacitor (a few μF in value) is preferred because it helps reduce no-load consumption and achieves good light-load regulation. However, stability may be affected when the feedback capacitor is too large.

For the set-ups shown in Figure 7 and Figure 8, a large feedback (VCC) capacitor can help increase the hiccup interval under protections, which reduces the input power under SCP and reduces the output voltage under open-loop condition.

Control Loop Robustness Optimization

The MP175 requires a small capacitor connected between FB and GND to achieve stable operation (around 1nF, which may vary in different applications). This small capacitor bypasses the noises that interfere with FB sampling.

When an internal feedback is adopted, another small feed-forward capacitor (tens of pF in value) should be used between FB and VCC to eliminate control loop oscillation. The potential oscillation is due to the delay of the R-C network, which is introduced by the large internal feedback resistor and the FB to GND capacitor discussed above.

Dummy Load

The MP175 switches at a minimum switching frequency and delivers a certain amount of power under no-load condition. This minimum switching frequency is determined by the feedback R-C discharge rate. A dummy load is required to dissipate this power and keep the output voltage regulated.

A large dummy load current leads to better regulation but larger no-load consumption. This is a compromise between small no-load consumption and good no-load regulation.

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Surge Performance

The input capacitor and filter can also be used for surge suppression. If an appropriate input circuit is chosen, the MP175 may pass the low-level surge test without any other surge suppression components. Figure 9 shows the typical half-wave rectifier used in low-power offline applications. Table 2 shows the capacitance that the MP175 requires under normal conditions for different surge levels. FR1 is a 20Ω/2W fused resistor, and L1 is 1mH for this recommendation.

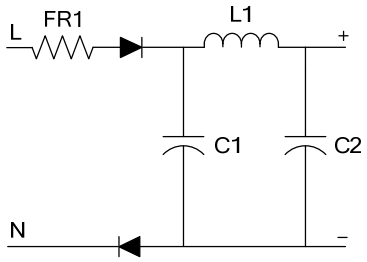


Figure 9: Half-Wave Rectifier

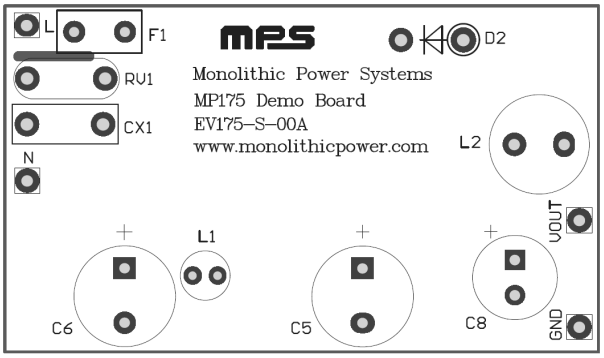
Table 2: Recommended Capacitance

Surge Voltage	500V	1000V	2000V
C1	1μF	2.2μF	3.3μF
C2	1μF	2.2μF	3.3μF

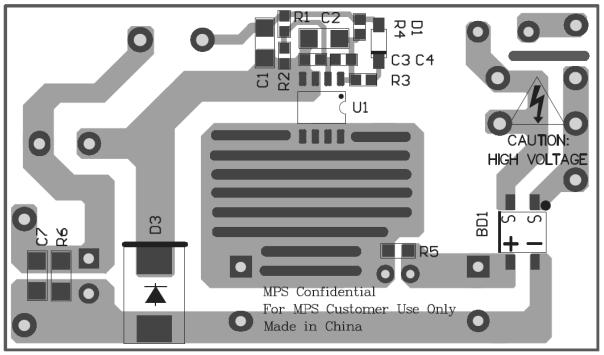
PCB Layout Guidelines

PCB layout is critical for reliable operation, good EMI, and thermal performance. For the best performance, refer to Figure 10 and follow the guidelines below.

1) Minimize the loop area formed by the input capacitor, MP175 internal MOSFET, freewheeling diode, inductor, and output capacitor.
2) Place the power inductor far away from the input filter while keeping the loop area small.
3) Keep the AC input loop as small as possible to prevent noise coupling.
4) Place a bypass capacitor (around 1nF) between FB and GND as close to the IC as possible.
5) Connect a large copper area to DRAIN for better thermal performance.



Top



Bottom

Figure 10: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

Figure 11 shows a typical application example of an 18V/550mA, non-isolated power supply using the MP175GS.

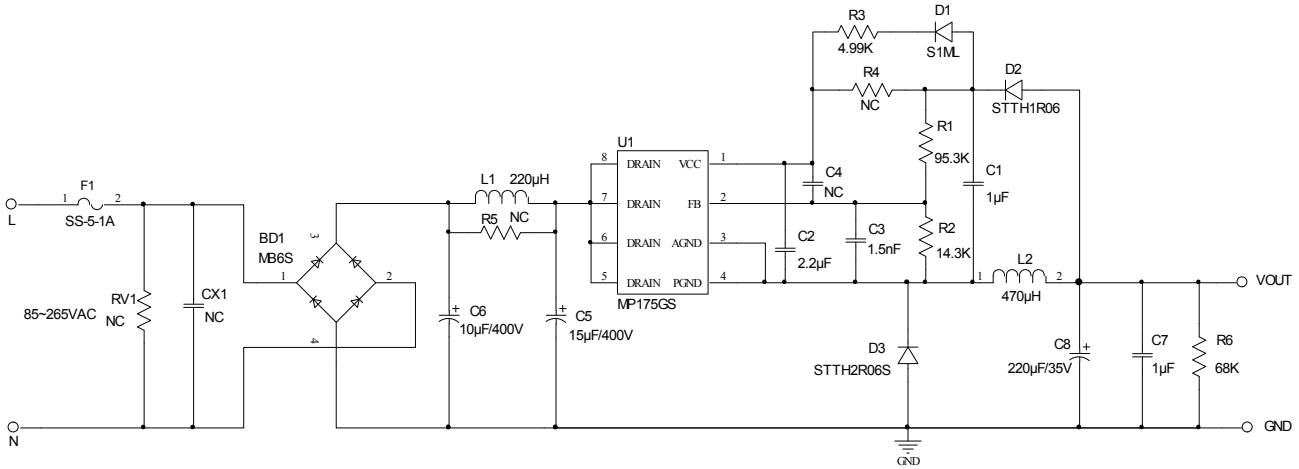

Figure 11: Typical Application with Universal Input and 18V/550mA Output

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PACKAGE INFORMATION

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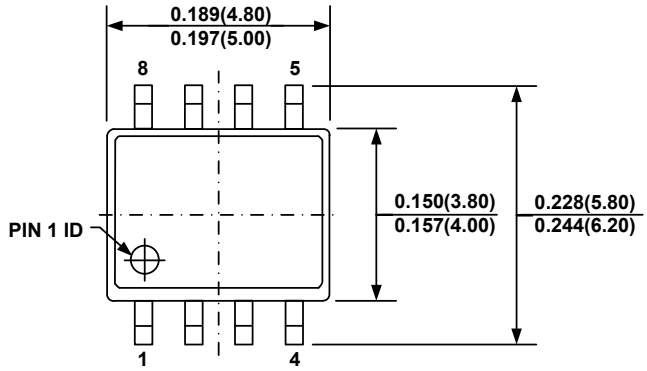
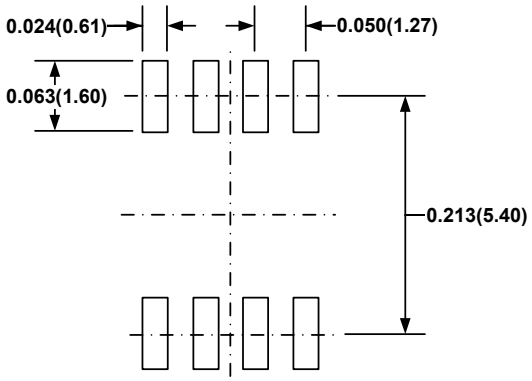
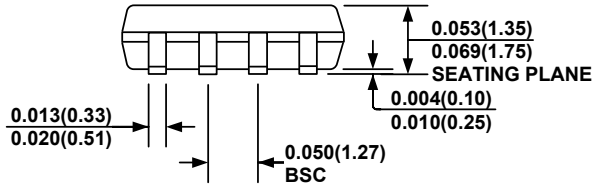


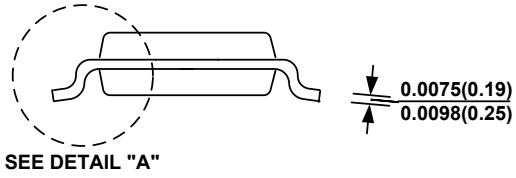
TOP VIEW



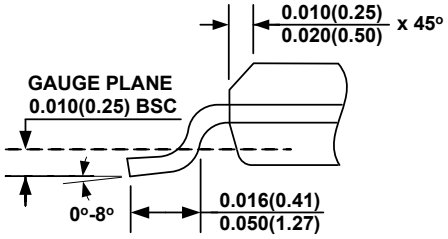
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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