MC5480 · MC7480
MC9380 · MC8380

ISSUE A

ORIG

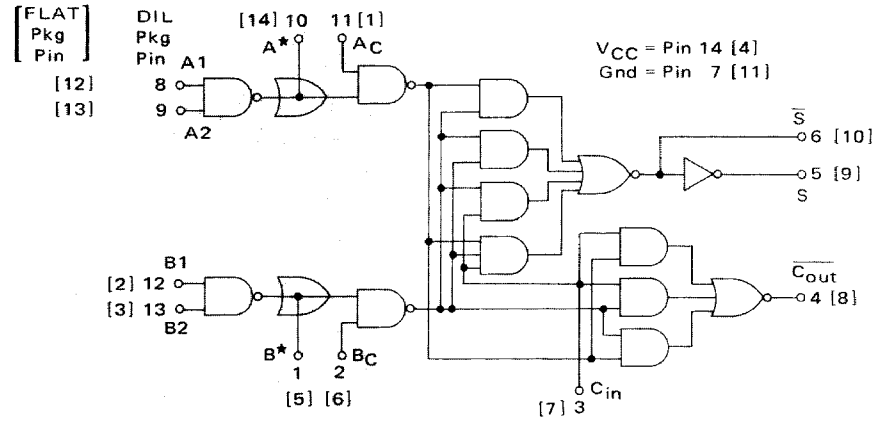
004477

4477

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 646) MC7480, MC8380.

These devices are one-bit binary full adders with grated complementary inputs, complementary Sum and $\overline{\text{Sum}}$ outputs, and an inverted Carry output. The circuit uses DTL inputs and a high-speed, high-fan-out, TTL "totem pole" configuration for the Sum, $\overline{\text{Sum}}$, and Carry outputs. The design of the high-speed carry circuitry reduces the need for external "look ahead carry" cascading in system designs. The use of low-level, low-power gates in a monolithic design provides significantly lower power dissipation than equivalent adders built from standard integrated circuits.

This full adder provides a basic building block for medium and high-speed, multiple-bit, parallel-add/serial-carry subsystems.



TRUTH TABLE

C_{in}	B	A	$\overline{C_{out}}$	$\bar{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

1. $A = \overline{A^{\bigstar} \cdot A_C}$, $B = \overline{B^{\bigstar} \cdot B_C}$

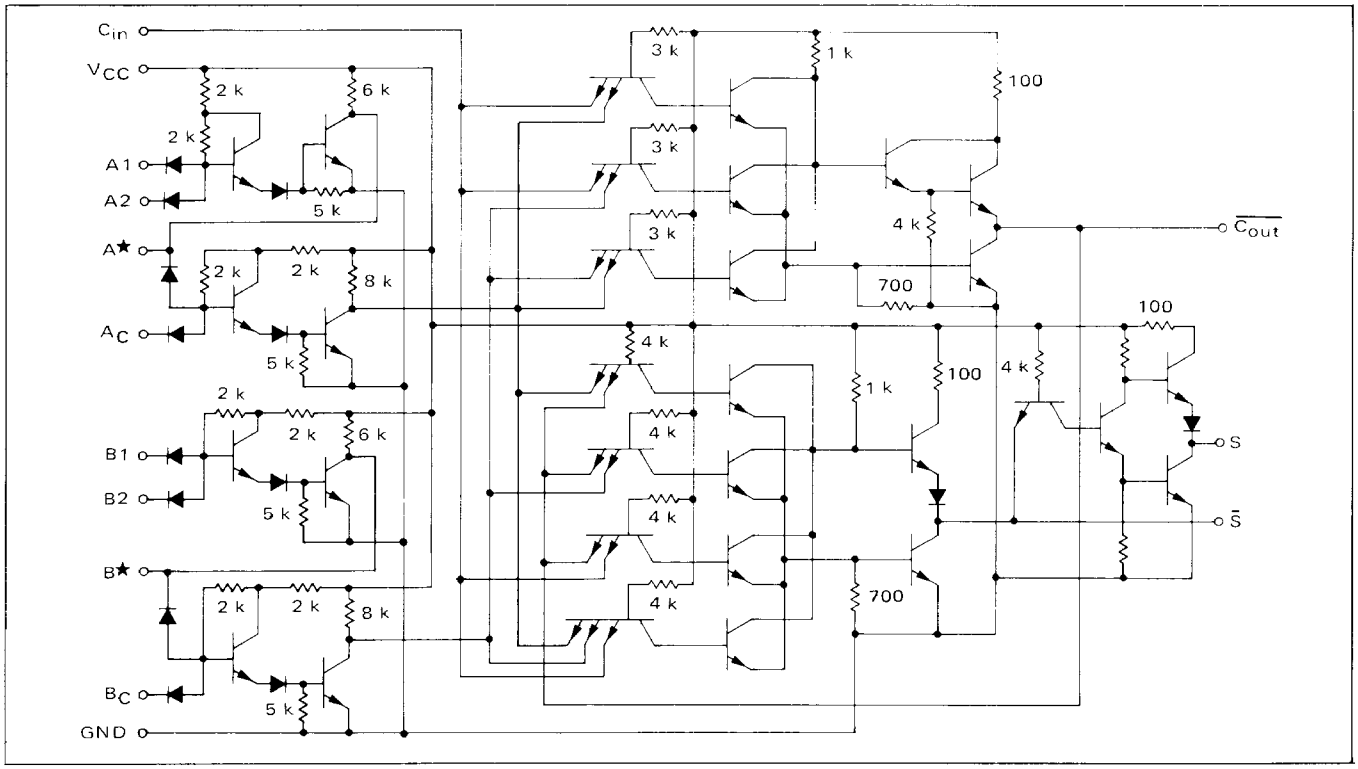
   where $A^{\bigstar} = \overline{A_1 \cdot A_2}$

   $B^{\bigstar} = \overline{B_1 \cdot B_2}$
2. When $A^{\bigstar}$ (or $B^{\bigstar}$) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
3. When A1 and A2 (or B1 and B2) are used as inputs, $A^{\bigstar}$ (or $B^{\bigstar}$) must be open, or used to perform wired-OR logic.

Input Loading Factor:
A1, A2, A_C, B1, B2, B_C = 1
$A^{\bigstar}$, $B^{\bigstar}$ = 1.625
C_{in} = 5

Output Loading Factor:
$\overline{C_{out}}$ = 5
S, $\bar{S}$ = 10
$A^{\bigstar}$, $B^{\bigstar}$ = 3

Total Power Dissipation = 105 mW typ/pkg



ELECTRICAL CHARACTERISTICS

Output voltage (logic level) tests are shown only for each output. The complete circuit can be tested by following the truth table.

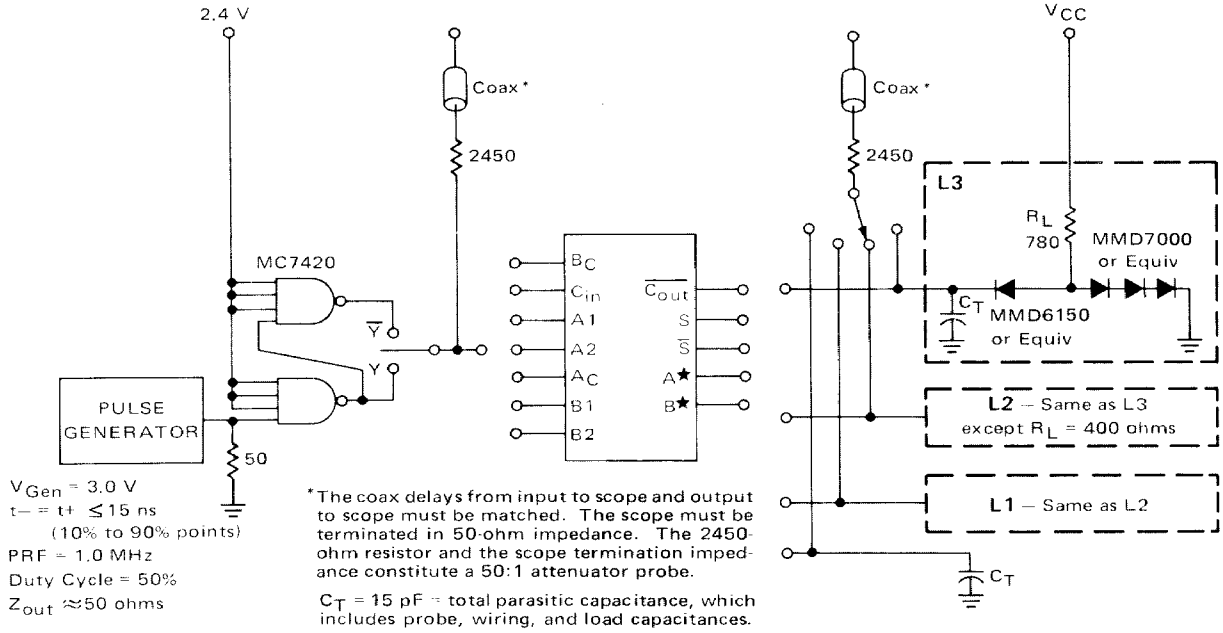
V = V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

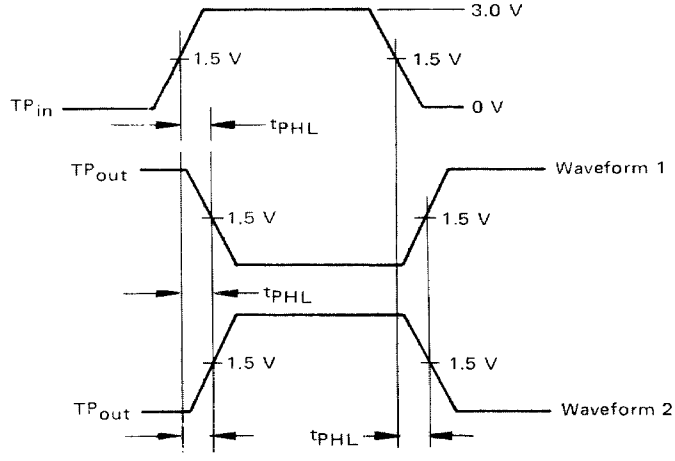
									TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
									mA						Volts							
									I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}
								MC5480, MC9380	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	0.8	2.0	4.5	5.5
								MC7480, MC8380	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	0.8	2.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5480/MC9380 Test Limits -55 to +125°C Min	Max	Unit	MC7480/MC8380 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below. Gnd
Input																							
Forward Current	I_{IL}	B*	–	-2.6	mAdc		-2.6	mAdc							B*			B_C				V	B1,B2
		B_C		-1.6		–	-1.6				–			–	B_C								B1,B2
		C_{in}	–	-8.0			-8.0								C_{in}								
		A1	–	-1.6		–	-1.6								A1			A2			B1,B2,A1,A2		
		A2	–	-1.6			-1.6								A2	–		A1					B_C,A_C
		A*	–	-2.6		–	-1.6				–			–	A*			A_C					
		A_C		-1.6		–	-1.6				–			–	A_C								A1,A2
		B1	–											–	B1			B2					A1,A2
		B2				–					–				B2			B1					
Leakage Current	I_{IH}	B_C	–	15	µAdc		15	µAdc				–				B_C						V	B*
		C_{in}		200		–	200									C_{in}							A1,A2,B1,B2
		A1	–	15			15							–		A1					B_C,A_C		A2
		A2				–					–		–			A2	–						A1
		A_C	–								–					A_C							A*
		B1														B1	–						B2
		B2	–								–					B2							B1
	I_{IHH}	B_C	–	1.0	mAdc	–	1.0	mAdc				–			–		B_C					V	B*
		C_{in}				–						–	–				C_{in}						A1,A2,B1,B2
		A1				–						–	–				A1	–			B_C,A_C		A2
		A2				–					–						A2						A1
		A_C	–								–			–			A_C						A*
		B1	–									–					B1						B2
		B2				–			–				–				B2						B1
Output																							
Output Voltage	V_{OL}	B*		0.4	Vdc	–	0.4	Vdc	B*		–			–	–		–			B1,B2		V	
		$\overline{C_{out}}$	–							$\overline{C_{out}}$		–		–					B_C,C_{in},A2	A1,B1			
																			A_C,B2				
		S	–						–		S	–							C_{in},A1,A2, B1,B2	B_C,A_C			
		$\overline{S}$							–		S	–			–		–		A2,B2				
		A*	–			–			A*			–		–	–		–			B_C,C_{in},A1,A_C,B1				
															–		–			A1,A2			
	V_{OH}	A*	2.4	–	Vdc	2.4		Vdc	–		–	B*		–						B1,B2		V	
		$\overline{C_{out}}$									–		$\overline{C_{out}}$	–						C_{in},A1,A2	B_C,A_C		
																				B1,B2			
		S		–					–		–		–	S			–			C_{in},A1,A_C	B_C,A2,B2		
		$\overline{S}$									–			$\overline{S}$						B1			
		B*		–					–	–	–	A*	–	–			–			A1,A2,B1,B2,B*,B_C	C_{in} A* A_C		
																				A1,A2			
Short-Circuit Current	I_{OS}†	$\overline{C_{out}}$	-20	-70	mAdc	-18	-70	mAdc	–					–			–		B_C,C_{in},A1, A_C,B1				
		S		-57			-57		–					–			–		B_C,A2,B2			V	C_{out},A2,B2
		$\overline{S}$		-57			-57			–				–					C_{in} A* ,B2				C_{in},S,A1,A_C,B1
																							B*,B_C,S,A1,A2,B1,B2
Power Requirements																							
Power Supply Drain	I_{CC}	V		31	mAdc		35	mAdc														V	

†Only one output should be shorted at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





TEST PROCEDURES (T_A = 25°C)

TEST	PIN UNDER TEST	INPUT B_C Pin 2 [6]	C_{in} Pin 3 [7]	A1 Pin 8 [12]	A2 Pin 9 [13]	A_C Pin 11 [1]	B1 Pin 12 [2]	B2 Pin 13 [3]	OUTPUT C_{out} Pin 4 [8]	S Pin 5 [9]	$\overline{S}$ Pin 6 [10]	A★ Pin 10 [14]	B★ Pin 1 [5]	MAX LIMIT	WAVE-FORM
t_{PLH} C_{out}	4 [8]		Y				Gnd		L3					17 ns	1
t_{PHL} C_{out}			Y				Gnd		L3					12 ns	1
t_{PLH} C_{out}		Y	2.4 V	Gnd			Gnd		L3					25 ns	2
t_{PHL} C_{out}		Y	2.4 V	Gnd			Gnd		L3					55 ns	2
t_{PLH} S	5 [9]		2.4 V	Gnd		Y	Gnd		L3	L1	L2			70 ns	2
t_{PHL} S	5 [9]		2.4 V	Gnd		Y	Gnd		L3	L1	L2			80 ns	2
t_{PLH} S	6 [10]	Y	2.4 V				Gnd				L2			55 ns	2
t_{PHL} S	6 [10]	Y	2.4 V				Gnd				L2			75 ns	2
t_{PLH} A★	10 [14]			Y	2.4 V		--					C_T		65 ns	1
t_{PHL} A★	10 [14]			Y	2.4 V						--	C_T		25 ns	1
t_{PLH} B★	1 [5]						Y	2.4 V					C–	65 ns	1
t_{PHL} B★	1 [5]						Y	2.4 V					C–	25 ns	1