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NTE4016B & NTE4016BT Integrated Circuit CMOS, Quad Analog Switch/Quad Multiplexer

Description:

The NTE4016B (14-Lead DIP) and NTE4016BT (SOIC-14) quad bilateral switches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each device consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator demodulator and CMOS logic implementation.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18Vdc
- Linearized Transfer Characteristics
- Low Noise – $12\text{nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0\text{kHz}$ typical
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	–0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}	–0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}	–0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}	$\pm 10\text{mA}$
Switch Through Current, I_{SW}	$\pm 25\text{mA}$
Power Dissipation (Per Package), P_D	500mW
Temperature Derating (from +65° to +125°C)	–7.0mW/°C
Ambient Temperature Range, T_A	–55° to +125°C
Storage Temperature Range, T_{stg}	–65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L	+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2, Note 3)

Parameter	Symbol	V _{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Voltage	V _{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
		10	–	–	–	1.5	0.9	–	–	Vdc
		15	–	–	–	1.5	0.9	–	–	Vdc
	V _{IH}	5.0	–	–	3.0	2.0	–	–	–	Vdc
		10	–	–	8.0	6.0	–	–	–	Vdc
		15	–	–	13.0	11.0	–	–	–	Vdc
Input Control Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance Control	C _{in}	–	–	–	–	5.0	–	–	–	pF
Switch Input		–	–	–	–	5.0	–	–	–	pF
Switch Output		–	–	–	–	5.0	–	–	–	pF
Feed Through		–	–	–	–	0.2	–	–	–	pF
Quiescent Current (Per Package, Note 4)	I _{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.5	–	0.0010	0.5	–	15	μAdc
		15	–	1.0	–	0.0015	1.0	–	30	μAdc
“ON” Resistance (V _C = V _{DD} , R _L = 10kΩ) (V _{in} = +5.0Vdc) (V _{in} = –5.0Vdc) V _{SS} = –5.0Vdc (V _{in} = ±5.0Vdc)	R _{ON}	5.0	–	600	–	300	660	–	840	Ohms
		5.0	–	600	–	300	660	–	840	Ohms
		5.0	–	600	–	280	660	–	840	Ohms
		(V _{in} = +7.5Vdc)	7.5	–	360	–	240	400	–	520
(V _{in} = –7.5Vdc) V _{SS} = –7.5Vdc (V _{in} = ±0.25Vdc)		7.5	–	360	–	240	400	–	520	Ohms
7.5		–	360	–	180	400	–	520	Ohms	
(V _{in} = +10Vdc)		10	–	600	–	260	660	–	840	Ohms
(V _{in} = +0.25Vdc) V _{SS} = 0Vdc (V _{in} = +5.6Vdc)		10	–	600	–	310	660	–	840	Ohms
10		–	600	–	310	660	–	840	Ohms	
(V _{in} = +15Vdc)		15	–	360	–	260	400	–	520	Ohms
(V _{in} = +0.25Vdc) V _{SS} = 0Vdc (V _{in} = +9.3Vdc)		15	–	360	–	260	400	–	520	Ohms
15		–	360	–	300	400	–	520	Ohms	
Δ“ON” Resistance Between any 2 circuits in a common package (V _C = V _{DD}) (V _{in} = ±5.0Vdc, V _{SS} = –5.0Vdc) (V _{in} = ±7.5.Vdc, V _{SS} = –7.5Vdc)	ΔR _{ON}	5.0	–	–	–	15	–	–	–	Ohms
		7.5	–	–	–	10	–	–	–	Ohms
Input/Output Leakage Current (V _C = V _{SS}) (V _{in} = +7.5Vdc, V _{out} = –7.5Vdc) (V _{in} = –7.5Vdc, V _{out} = +7.5Vdc)	–	7.5	–	±0.1	–	±0.0015	±0.1	–	±0.1	μAdc
		7.5	–	±0.1	–	±0.0015	±0.1	–	±0.1	μAdc

Note 2. All unused inputs must be returned to V_{DD} or V_{SS} .

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 4. For voltage drops across the switch (ΔV_{switch}) > 600mV (> 300mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded (See first page of this data sheet.).

Electrical Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 3, Note 5)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Time ($V_{SS} = 0\text{Vdc}$) V_{in} to V_{out} ($V_C = V_{DD}$, $R_L = 10\text{k}\Omega$)	t_{PLH} , t_{PHL}	5.0	–	15	45	ns
		10	–	7.0	15	ns
		15	–	6.0	12	ns
Control to Output $V_{in} \leq 10\text{Vdc}$, $R_L = 10\text{k}\Omega$)	t_{PHZ} , T_{PLZ} , t_{PZH} , t_{PZL}	5.0	–	34	90	ns
		10	–	20	45	ns
		15	–	15	35	ns
Crosstalk, Control to Output ($V_{SS} = 0\text{Vdc}$) ($V_C = V_{DD}$, $R_{in} = 10\text{k}\Omega$, $R_{out} = 10\text{k}\Omega$, $f = 1.0\text{kHz}$)	–	5.0	–	30	–	mV
		10	–	50	–	mV
		15	–	100	–	mV
Crosstalk Between any Two Switches ($V_{SS} = 0\text{Vdc}$) ($R_L = 1.0\text{k}\Omega$, $f = 1.0\text{kHz}$, Crosstalk = $20\log_{10} \frac{V_{out1}}{V_{out2}}$)	–	5.0	–	–80	–	dB
Noise Voltage ($V_{SS} = 0\text{Vdc}$) ($V_C = V_{DD}$, $f = 100\text{Hz}$) ($V_C = V_{DD}$, $f = 100\text{kHz}$)		5.0	–	24	–	$\text{nV}/\sqrt{\text{Cycle}}$
		10	–	25	–	$\text{nV}/\sqrt{\text{Cycle}}$
		15	–	30	–	$\text{nV}/\sqrt{\text{Cycle}}$
		5.0	–	12	–	$\text{nV}/\sqrt{\text{Cycle}}$
		10	–	12	–	$\text{nV}/\sqrt{\text{Cycle}}$
		15	–	15	–	$\text{nV}/\sqrt{\text{Cycle}}$
Second Harmonic Distortion ($V_{SS} = -5.0\text{Vdc}$) ($V_{in} = 1.77\text{Vdc}$, RMS Centered Q 0.0Vdc , $R_L = 10\text{k}\Omega$, $f = 1.0\text{kHz}$)	–	5.0	–	0.16	–	%
Insertion Loss ($V_C = V_{DD}$, $V_{in} = 1.77\text{Vdc}$, $V_{SS} = -5.0\text{Vdc}$, (RMS centered = 0.0Vdc , $f = 1.0\text{MHz}$) $I_{loss} = 20\log_{10} \frac{V_{out1}}{V_{out2}}$ ($R_L = 1.0\text{k}\Omega$) ($R_L = 10\text{k}\Omega$) ($R_L = 100\text{k}\Omega$) ($R_L = 1.0\text{M}\Omega$)	–	5.0				
			–	2.3	–	dB
			–	0.2	–	dB
			–	0.1	–	dB
			–	0.05	–	dB
Bandwidth (-3.0dB) ($V_C = V_{DD}$, $V_{in} = 1.77\text{Vdc}$, $V_{SS} = -5.0\text{Vdc}$, (RMS centered = 0.0Vdc) ($R_L = 1.0\text{k}\Omega$) ($R_L = 10\text{k}\Omega$) ($R_L = 100\text{k}\Omega$) ($R_L = 1.0\text{M}\Omega$)	–	5.0				
			–	54	–	MHz
			–	40	–	MHz
			–	38	–	MHz
			–	37	–	MHz

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 5. The formulas given are for the typical characteristics only at $+25^\circ\text{C}$.

Electrical Characteristics (Cont'd): ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 3, Note 5)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
OFF Channel Feedthrough Attenuation ($V_{SS} = -5.0\text{Vdc}$) ($V_C = V_{SS}$, $20\log_{10} \frac{V_{out1}}{V_{out2}} = -50\text{dB}$) ($R_L = 1.0\text{k}\Omega$) ($R_L = 10\text{k}\Omega$) ($R_L = 100\text{k}\Omega$) ($R_L = 1.0\text{M}\Omega$)	–	5.0				
			–	1250	–	kHz
			–	140	–	kHz
			–	18	–	kHz
			–	2.0	–	kHz

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 5. The formulas given are for the typical characteristics only at $+25^\circ\text{C}$.

Pin Connection Diagram

In 1 **1** **14** V_{DD}
Out 1 **2** **13** Control 1
Out 2 **3** **12** Cont D
In 2 **4** **11** In/Out D
Control 2 **5** **10** Out/In D
Control 3 **6** **9** Out/In C
 V_{SS} **7** **8** In/Out C

Block Diagram

Control 1 **13**
In 1 **1** Out 1 **2**
Control 2 **5**
In 2 **4** Out 2 **3**
Control 3 **6**
In 3 **8** Out 3 **9**
Control 4 **12**
In 4 **11** Out 4 **10**

$V_{DD} = \text{Pin14}$
 $V_{SS} = \text{Pin7}$

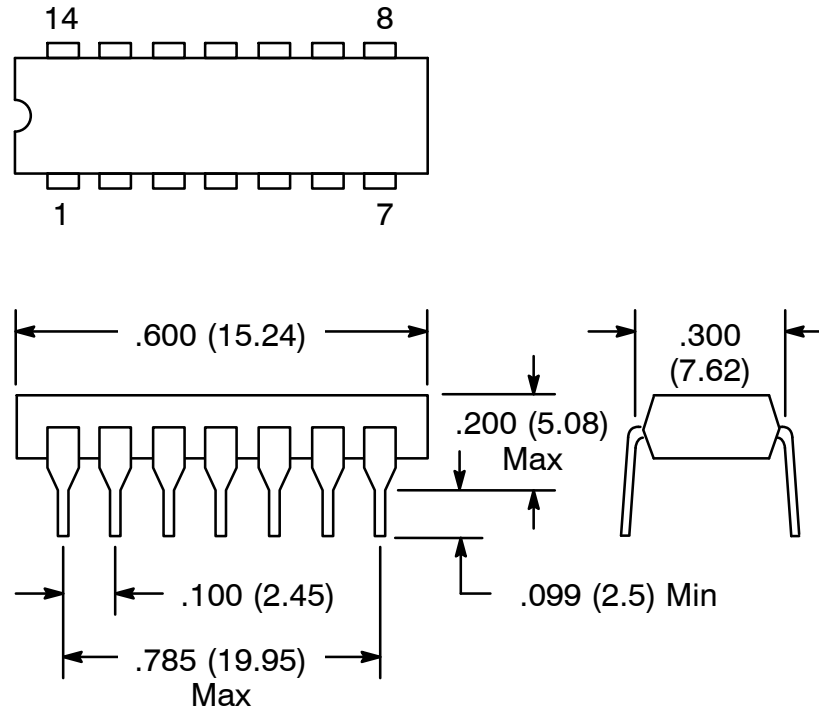
Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

Pin Connection Diagram
(1/4 of Device Shown)

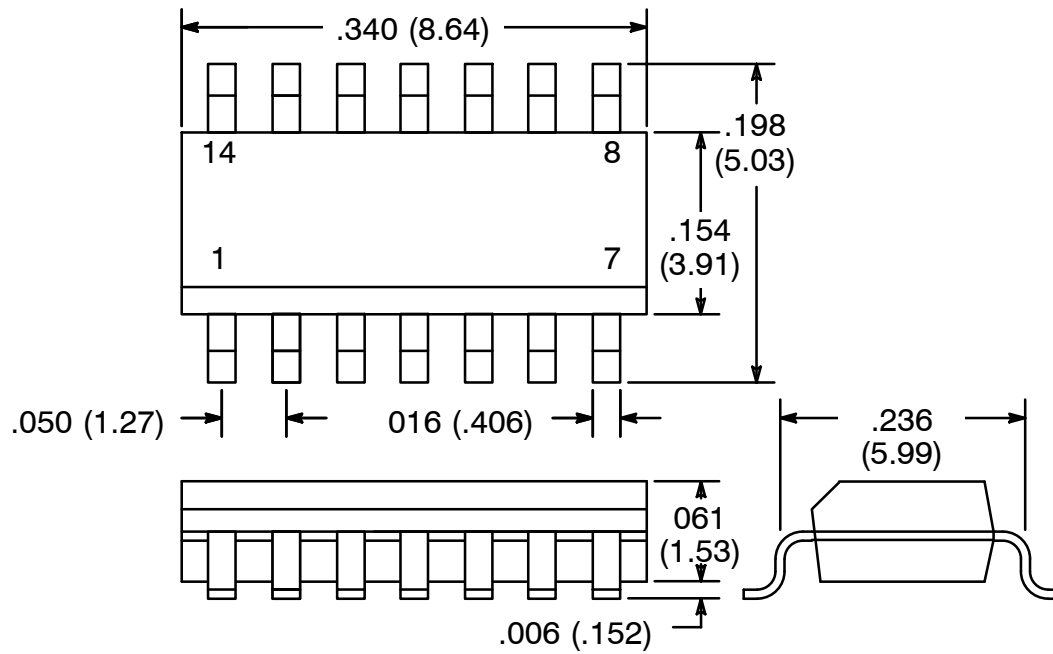
Control — [Inverter] — [Inverter] — [Switch] — Out
In — [Switch] — Out

Logic Diagram Restrictions
 $V_{SS} \leq V_{in} \leq V_{DD}$
 $V_{SS} \leq V_{out} \leq V_{DD}$

NTE4016B



NTE4016BT



NOTE: Pin1 on Beveled Edge