

54AC138 • 54ACT138

1-of-8 Decoder/Demultiplexer

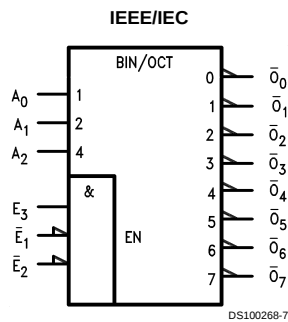
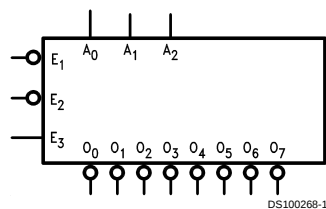
General Description

The 'AC/ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/ACT138 devices or a 1-of-32 decoder using four 'AC/ACT138 devices and one inverter.

Features

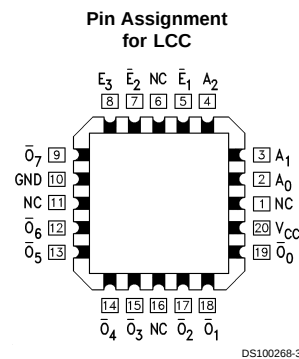
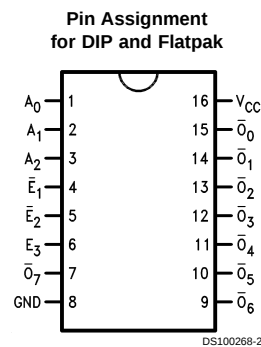
- I_{CC} reduced by 50%
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT138 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
 - 'AC138: 5962-87622
 - 'ACT138: 5962-87554

Logic Symbols



Pin Names	Description
A_0 – A_2	Address Inputs
$\bar{E}_1$ – $\bar{E}_2$	Enable Inputs
E_3	Enable Input
$\bar{O}_0$ – $\bar{O}_7$	Outputs

Connection Diagrams



Functional Description

The 'AC/ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$ – $\overline{O}_7$). The 'AC/ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel ex-

pansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/ACT138 devices and one inverter (see *Figure 1*). The 'AC/ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

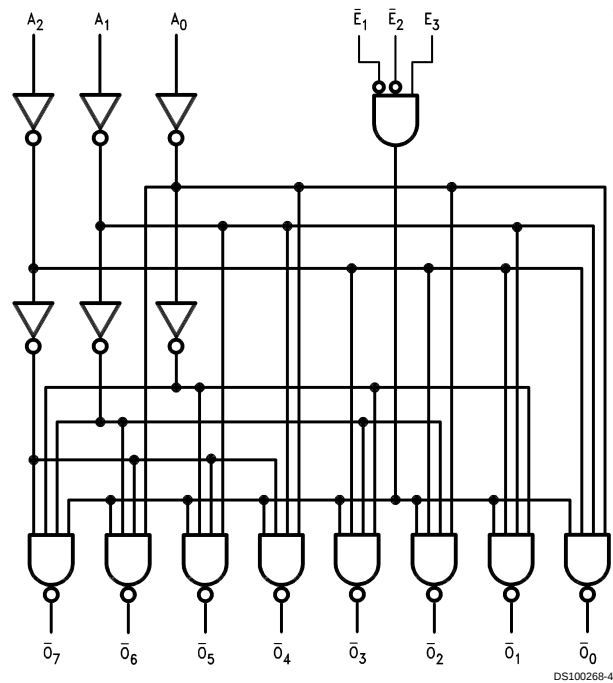
Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram (Continued)

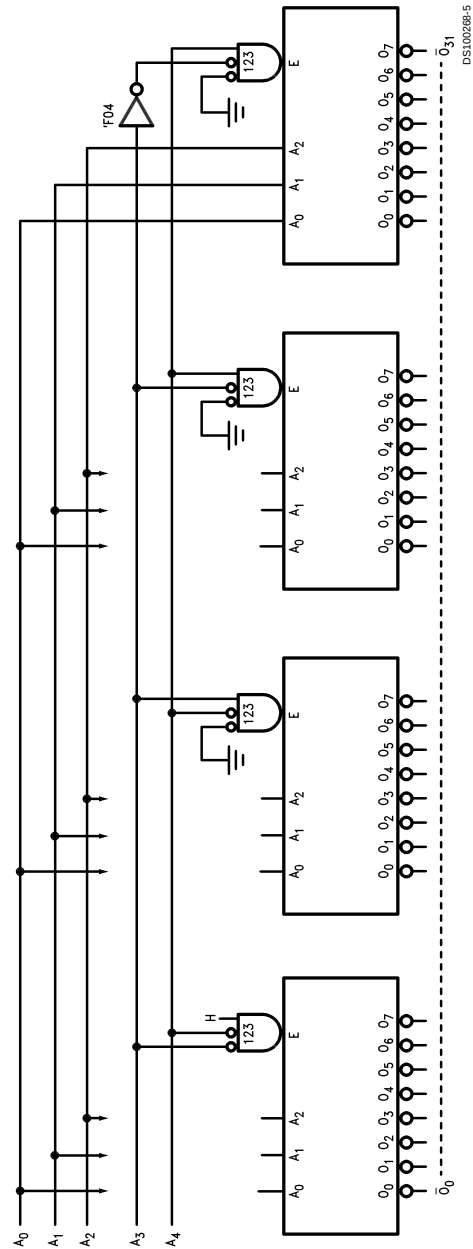


FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.4		
		5.5	5.4		
		3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
		4.5	3.7		
		5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.1		
		5.5	0.1		
		3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
		4.5	0.50		
		5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0	μA	$V_I = V_{CC}, GND$
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5	-50	mA	$V_{OHD} = 3.85V$ Min

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	54ACT	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I _{OUT} = –50 μA
		4.5 5.5	3.70 4.70	V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OH} –24 mA –24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5	0.50 0.50	V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OL} 24 mA 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} – 2.1V
I _{OLD}	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	–50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 8)	54AC		Units	Fig. No.
			T _A = −55°C to +125°C C _L = 50 pF			
			Min	Max		
t _{PLH}	Propagation Delay	3.3	1.0	16.0	ns	
	A _n to $\overline{O}_n$	5.0	1.5	12.0		
t _{PHL}	Propagation Delay	3.3	1.0	15.0	ns	
	A _n to $\overline{O}_n$	5.0	1.5	11.5		
t _{PLH}	Propagation Delay	3.3	1.0	16.5	ns	
	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	13.0		
t _{PHL}	Propagation Delay	3.3	1.0	15.5	ns	
	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	12.0		
t _{PLH}	Propagation Delay	3.3	1.0	17.0	ns	
	E ₃ to $\overline{O}_n$	5.0	1.5	13.5		
t _{PHL}	Propagation Delay	3.3	1.0	15.0	ns	
	E ₃ to $\overline{O}_n$	5.0	1.5	11.0		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

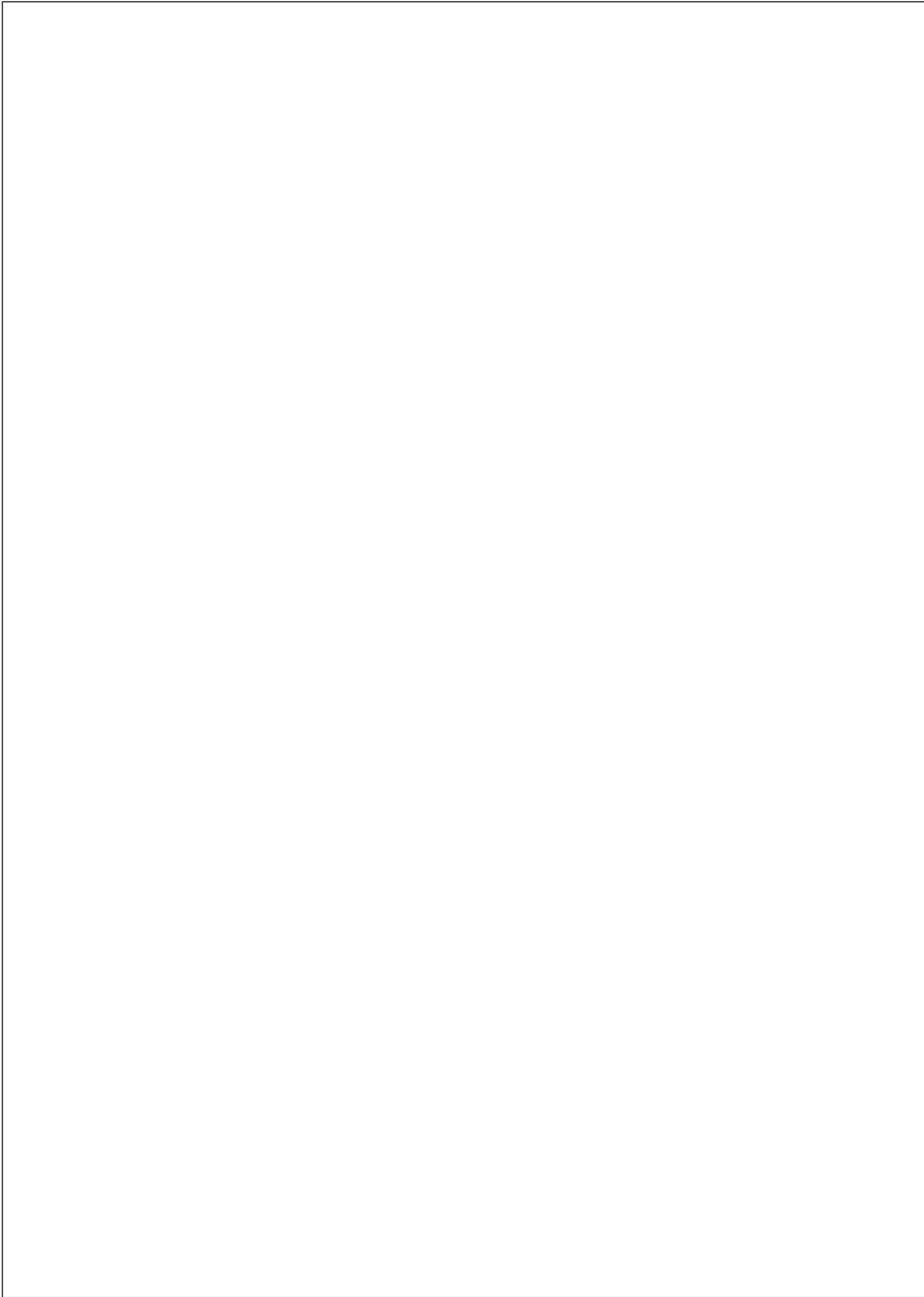
AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 9)	54ACT		Units	Fig. No.
			T _A = −55°C to +125°C C _L = 50 pF			
			Min	Max		
t _{PLH}	Propagation Delay A _n to $\overline{O}_n$	5.0	1.5	12.5	ns	
t _{PHL}	Propagation Delay A _n to $\overline{O}_n$	5.0	1.5	12.5	ns	
t _{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	13.5	ns	
t _{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	12.5	ns	
t _{PLH}	Propagation Delay E ₃ to $\overline{O}_n$	5.0	1.5	14.0	ns	
t _{PHL}	Propagation Delay E ₃ to $\overline{O}_n$	5.0	1.5	12.0	ns	

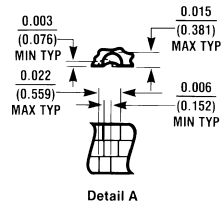
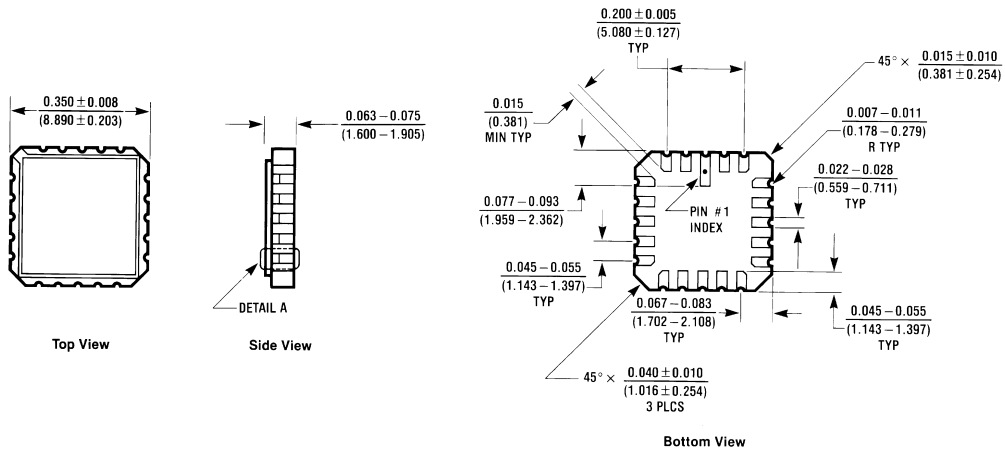
Note 9: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.0V

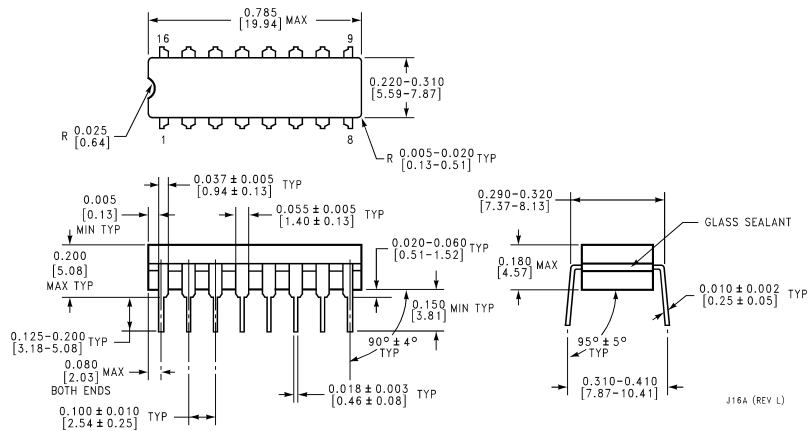


Physical Dimensions inches (millimeters) unless otherwise noted



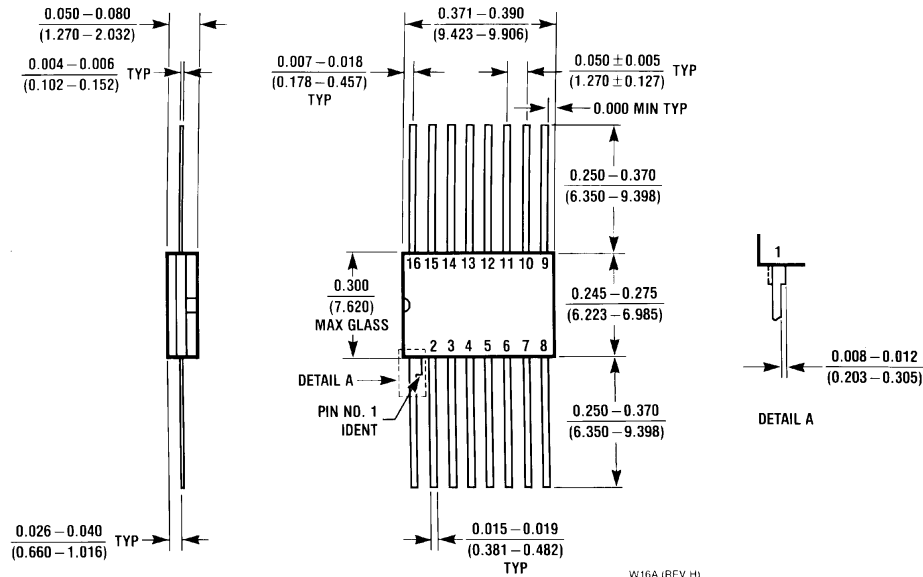
20 Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A

E20A (REV D)



16 Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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