

# Product Document

# AS3709

## Micro-PMIC with 5 DC/DCs and 2 LDOs

### General Description

The AS3709 is an ultra compact Micro-PMIC containing 5 high-efficiency, constant-frequency synchronous buck converters in addition with two universal IO LDOs are available for lower current power rails. The wide input voltage range (2.7V to 5.5V), automatic power-save mode and minimal external component requirements make the AS3709 perfect for any single Li-Ion battery-powered or fixed 3.3V/5V supply application. Typical supply current with no load is 110µA and decreases to  $\leq 7\mu\text{A}$  in shutdown mode. An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (2MHz, 3MHz or 4MHz) allows the use of small surface mount external components. Very low output voltages can be delivered with the internal 0.6V feedback reference voltage. The AS3709 is available in a 32-pin QFN 4x4mm package and in a very compact WL-CSP36 with 0.4mm pitch.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of AS3709, Micro-PMIC with 5 DC/DCs and 2 LDOs are listed below:

**Figure 1:**  
**Added Value of Using AS3709**

| Benefits                                                                                                                                               | Features                                                                                                                                                                                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Compact design due to small coils for IO and memory voltage generation</li> </ul>                             | <ul style="list-style-type: none"> <li>• 5 DC/DC step down regulators (2-4MHz)</li> </ul>                                                                                                    |
| <ul style="list-style-type: none"> <li>• Independent voltage rails for general purpose IO supplies</li> </ul>                                          | <ul style="list-style-type: none"> <li>• 2 universal IO LDOs</li> </ul>                                                                                                                      |
| <ul style="list-style-type: none"> <li>• Flexible and fast adaptation to different processors/applications</li> </ul>                                  | <ul style="list-style-type: none"> <li>• OTP programmable boot sequence</li> </ul>                                                                                                           |
| <ul style="list-style-type: none"> <li>• Power saving control according to the processor's needs.</li> </ul>                                           | <ul style="list-style-type: none"> <li>• Stand-by function with selectable rails and programmable voltages</li> </ul>                                                                        |
| <ul style="list-style-type: none"> <li>• Self-contained start-up and control for single-cell battery applications. Safety shutdown feature.</li> </ul> | <ul style="list-style-type: none"> <li>• Control Interface</li> <li>• I<sup>2</sup>C control lines</li> <li>• ON key with 4s/8s emergency shut-down</li> <li>• POR with RESET I/O</li> </ul> |
| <ul style="list-style-type: none"> <li>• Dedicated packages for specific applications. Optimization for PCB cost or size.</li> </ul>                   | <ul style="list-style-type: none"> <li>• 32-pin QFN (4mmx4mm), 0.4mm pitch</li> <li>• 36-ball WL-CSP 0.4mm pitch</li> </ul>                                                                  |

## Applications

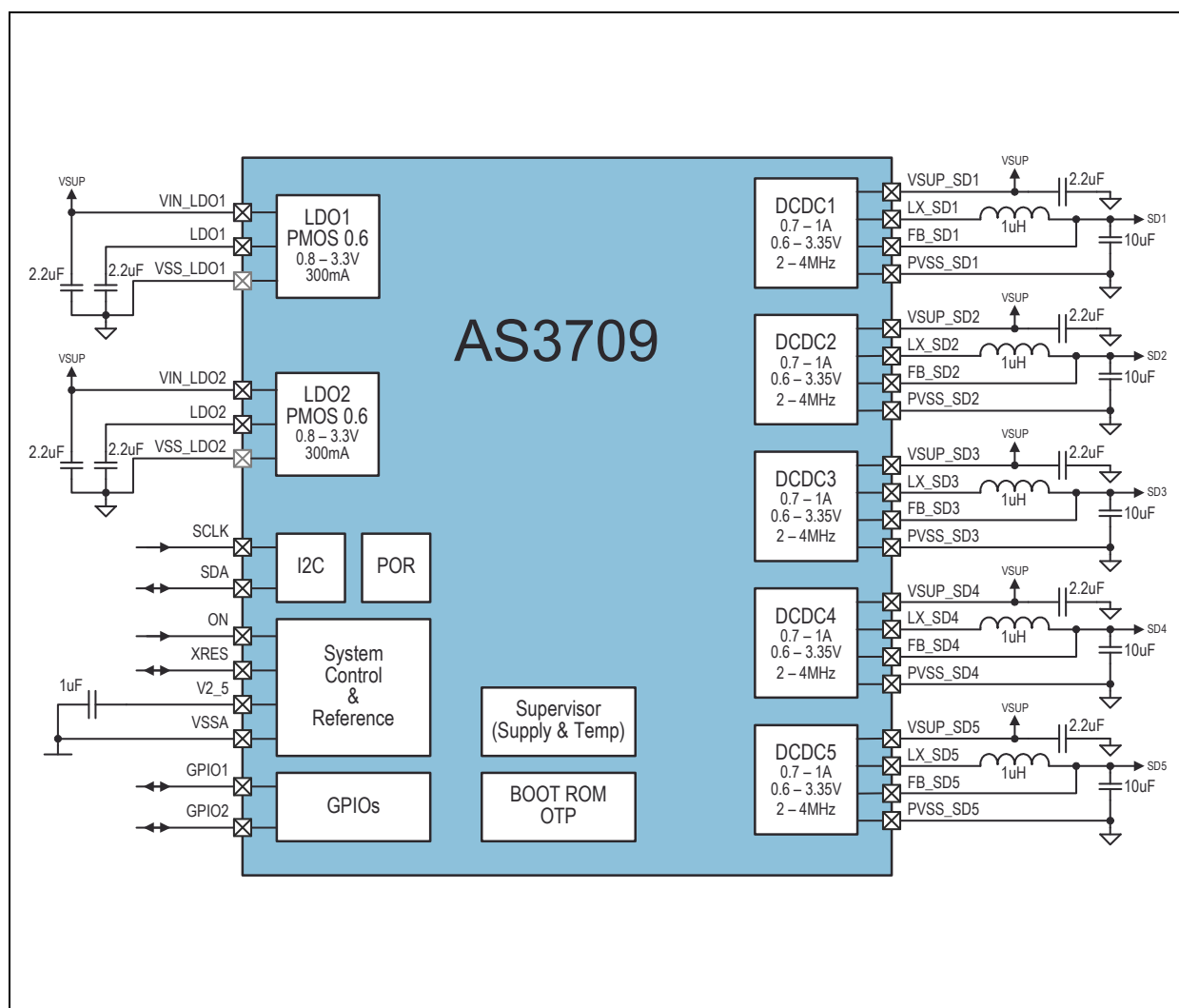
The device is ideal for:

- SSDs, mobile communication devices
- Laptops and PDAs
- Ultra-low-power systems
- Medical instruments or any other space-limited application with low power-consumption requirements.

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**  
**AS3709 Block Diagram**

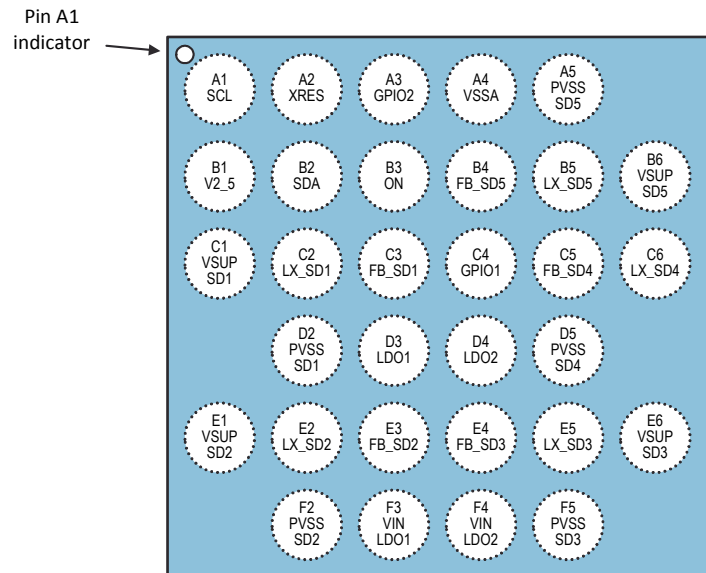


## Pin Assignments

The AS3709 pin assignments are described below.

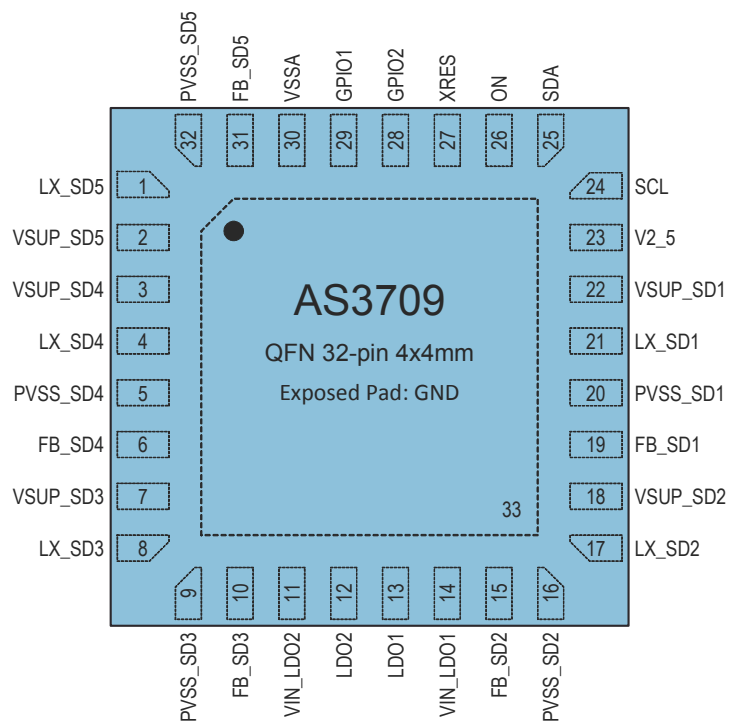
**Figure 3:**  
**36 Balls WL-CSP with 0.4mm Pitch**

**Ball Assignments:** Shows the top view ball assignment of the AS3709 WL-CSP.



**Figure 4:**  
**32 Pins QFN 4x4 with 0.4mm Pitch**

**Pin Assignment:** Shows the top view pin assignment of the AS3709 QFN package.



**Figure 5:**  
**Pin Description**

| Pin Number |        | Pin Name | Pin Type | Description                                | If Not Used     |
|------------|--------|----------|----------|--------------------------------------------|-----------------|
| QFN        | WL-CSP |          |          |                                            |                 |
| 1          | B5     | LX_SD5   | DIG OUT  | DC/DC SD5 switch output to coil            | Open            |
| 2          | B6     | VSUP_SD5 | SUP IN   | DC/DC SD5 pos supply terminal              | Always needed   |
| 3          | B6     | VSUP_SD4 | SUP IN   | DC/DC SD4 pos supply terminal              | Always needed   |
| 4          | C6     | LX_SD4   | DIG OUT  | DC/DC SD4 switch output to coil            | Open            |
| 5          | D5     | PVSS_SD4 | GND      | DC/DC SD4 neg supply terminal              | Always needed   |
| 6          | C5     | FB_SD4   | ANA IN   | DC/DC SD4 Feedback pin                     | Open            |
| 7          | E6     | VSUP_SD3 | SUP IN   | DC/DC SD3 pos supply terminal              | Always needed   |
| 8          | E5     | LX_SD3   | DIG OUT  | DC/DC SD3 switch output to coil            | Open            |
| 9          | F5     | PVSS_SD3 | GND      | DC/DC SD3 neg supply terminal              | Always needed   |
| 10         | E4     | FB_SD3   | ANA IN   | DC/DC SD3 Feedback pin                     | Open            |
| 11         | F4     | VIN_LDO2 | SUP IN   | Supply pin for LDO2                        | Always needed   |
| 12         | D4     | LDO2     | ANA OUT  | Output Voltage of LDO2                     | Open            |
| 13         | D3     | LDO1     | ANA OUT  | Output Voltage of LDO1                     | Open            |
| 14         | F3     | VIN_LDO1 | SUP IN   | Supply pin for LDO1                        | Always needed   |
| 15         | E3     | FB_SD2   | ANA IN   | DC/DC SD2 Feedback pin                     | Open            |
| 16         | F2     | PVSS_SD2 | GND      | DC/DC SD2 neg supply terminal              | Always needed   |
| 17         | E2     | LX_SD2   | DIG OUT  | DC/DC SD2 switch output to coil            | Open            |
| 18         | E1     | VSUP_SD2 | SUP IN   | DC/DC SD2 pos supply terminal              | Always needed   |
| 19         | C3     | FB_SD1   | ANA IN   | DC/DC SD1 Feedback pin                     | Open            |
| 20         | D2     | PVSS_SD1 | GND      | DC/DC SD1 neg supply terminal              | Always needed   |
| 21         | C2     | LX_SD1   | DIG OUT  | DC/DC SD1 switch output to coil            | Open            |
| 22         | C1     | VSUP_SD1 | SUP IN   | DC/DC SD1 pos supply terminal              | Always needed   |
| 23         | B1     | V2_5     | ANA OUT  | Internal 2.5V regulator output             | Always needed   |
| 24         | A1     | SCL      | DIG IN   | 2-wire Serial IF Clock Input               | Pull-up to V2_5 |
| 25         | B2     | SDA      | DIG IO   | 2-wire Serial IF Data IO                   | Pull-up to V2_5 |
| 26         | B3     | ON       | DIG IN   | Power Up Input                             | Open            |
| 27         | A2     | XRES     | DIG IO   | Reset IO, external pull-up resistor needed | Always needed   |

| Pin Number |        | Pin Name | Pin Type | Description                     | If Not Used   |
|------------|--------|----------|----------|---------------------------------|---------------|
| QFN        | WL-CSP |          |          |                                 |               |
| 28         | A3     | GPIO2    | ANA IO   | General Purpose IO 2            | Open          |
| 29         | C4     | GPIO1    | ANA IO   | General Purpose IO 1            | Open          |
| 30         | A4     | VSSA     | GND      | GND Reference for analog blocks | Always needed |
| 31         | B4     | FB_SD5   | ANA IN   | DC/DC SD5 Feedback pin          | Open          |
| 32         | A5     | PVSS_SD5 | GND      | DC/DC SD5 neg supply terminal   | Always needed |
| 33         |        | VSS      | GND      | Exposed Pad                     | Always needed |

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 6:**  
**Absolute Maximum Ratings**

| Symbol                                               | Parameter                                   | Min  | Max | Units | Comments                                                                       |
|------------------------------------------------------|---------------------------------------------|------|-----|-------|--------------------------------------------------------------------------------|
| Electrical Parameters                                |                                             |      |     |       |                                                                                |
|                                                      | Supply Voltage to Ground 5V Pins            | -0.5 | 7.0 | V     | Applicable for pins: VSUP_SDx, VIN_LDOx, SCLK, SDA, ON, XRES, GPIOx, LX_SDx    |
|                                                      | Supply Voltage to Ground 3V Pins            | -0.5 | 5.0 | V     | Applicable for pins: V2_5, LDOx, FB_SDx                                        |
|                                                      | Voltage Difference between Ground Terminals | -0.3 | 0.3 | V     | Applicable for pins: VSSA, PVSS_SDx, Exposed Pad                               |
|                                                      | Input Current (latch-up immunity)           | -100 | 100 | mA    | JEDEC JESD78                                                                   |
| Continuous Power Dissipation (T <sub>A</sub> = 70°C) |                                             |      |     |       |                                                                                |
| P <sub>T</sub>                                       | Continuous Power Dissipation                |      | 1.2 | W     | P <sub>T</sub> <sup>(1)</sup> for QFN32 package (R <sub>THJA</sub> ~ 45K/W)    |
|                                                      |                                             |      | 1.1 | W     | P <sub>T</sub> <sup>(1)</sup> for WL-CSP36 package (R <sub>THJA</sub> ~ 50K/W) |
| Electrostatic Discharge                              |                                             |      |     |       |                                                                                |
| ESD <sub>HBM</sub>                                   | Electrostatic Discharge HBM                 | ±2   |     | kV    | JEDEC JESD22-A114F                                                             |
| Temperature Ranges and Storage Conditions            |                                             |      |     |       |                                                                                |
| T <sub>A</sub>                                       | Operating Temperature                       | -40  | 85  | °C    |                                                                                |
| T <sub>J</sub>                                       | Junction Temperature                        |      | 125 | °C    |                                                                                |
| T <sub>STRG</sub>                                    | Storage Temperature Range                   | -55  | 150 | °C    | QFN                                                                            |
|                                                      |                                             | -55  | 125 | °C    | WL-CSP                                                                         |
| RH <sub>NC</sub>                                     | Relative Humidity (non-condensing)          | 5    | 85  | %     |                                                                                |



| Symbol                         | Parameter                  | Min | Max | Units | Comments                                                                                                                     |
|--------------------------------|----------------------------|-----|-----|-------|------------------------------------------------------------------------------------------------------------------------------|
| <b>Temperature (Soldering)</b> |                            |     |     |       |                                                                                                                              |
| T <sub>BODY</sub>              | Package Body Temperature   |     | 260 | °C    | 32-pin QFN:<br>Norm IPC/JEDEC J-STD-020 <sup>(2)</sup><br>The lead finish for Pb-free leaded packages is matte tin (100% Sn) |
|                                |                            |     | 260 | °C    | 36-ball WL-CSP:<br>Norm IPC/JEDEC J-STD-020 <sup>(2)</sup>                                                                   |
| MSL                            | Moisture Sensitivity Level | 3   |     |       | Represents a maximum floor life time of 168h (QFN)                                                                           |
|                                |                            | 1   |     |       | Represents an unlimited floor life time (WL-CSP)                                                                             |

**Note(s):**

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices"



## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 7:**  
Electrical Characteristics

| Symbol         | Parameter                   | Conditions                                                                                         | Min | Typ | Max | Unit    |
|----------------|-----------------------------|----------------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| $V_{IN}$       | Input Voltage Range         | Pin $V_{SUP}$                                                                                      | 2.7 |     | 5.5 | V       |
| $I_Q$          | Quiescent Current           | Normal operating current. With bit Low_power_on = 0; only V2_5 active                              |     | 155 | 200 | $\mu A$ |
| $I_{LOWPOWER}$ | Low-Power Quiescent Current | Normal operating current. With bit Low_power_on = 1; only V2_5 active                              |     | 110 |     |         |
| $I_{POWEROFF}$ | Shutdown Current            | With bit power_off = 1; only V2_5 is active in power OFF mode.<br>Not tested, guaranteed by design |     | 7   | 20  |         |

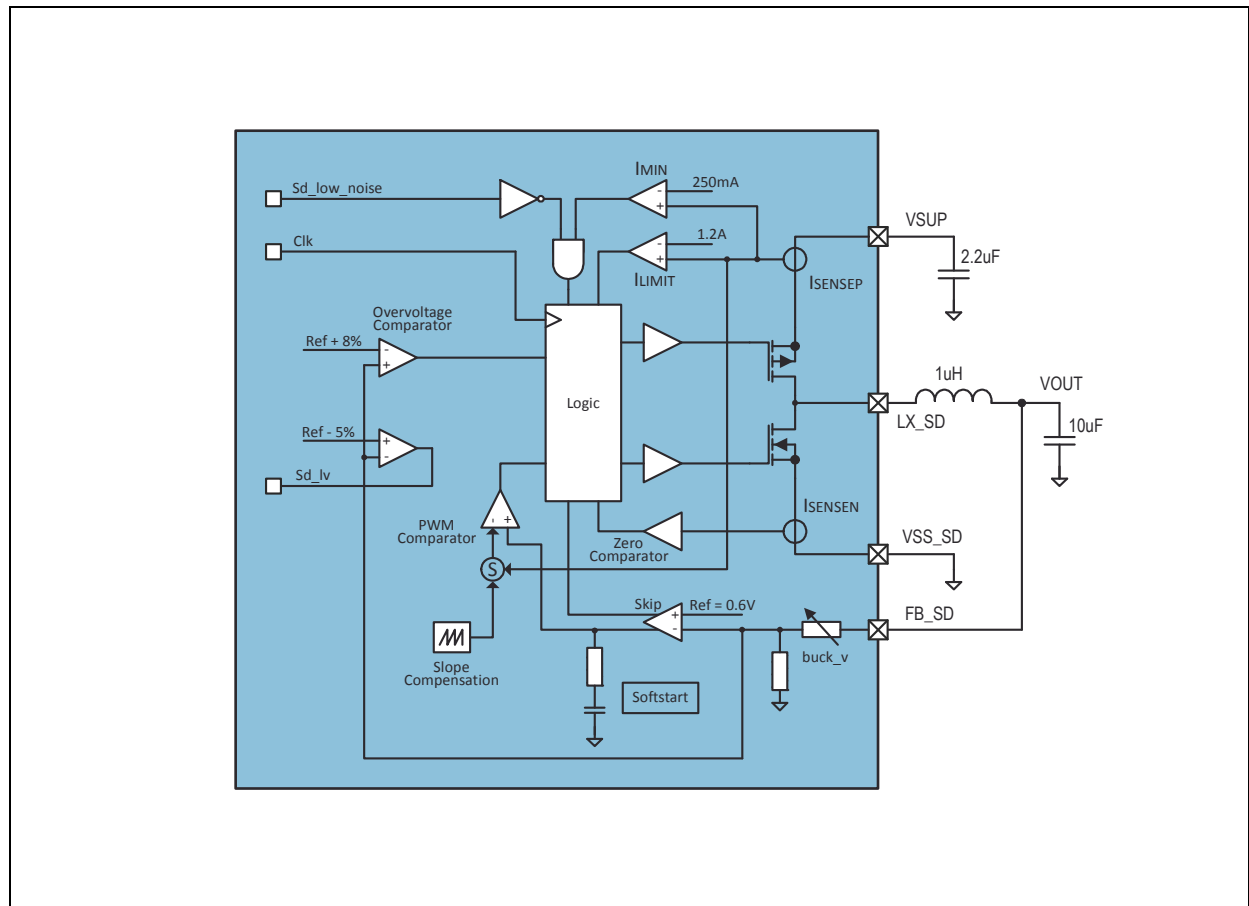
**Electrical Characteristics:**  $V_{SUP} = 3.7V$ ,  $V_{OUT} < V_{IN} - 0.5V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , typ. values @  $T_A = 25^{\circ}C$  (unless otherwise specified)

## Detailed Description - Power Management Functions

### Step Down DC/DC Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A, with an output capacitor of only 10 $\mu$ F. The implemented current limitation protects the DC/DC Converter and the coil during overload condition.

**Figure 8:**  
**Step Down DC/DC Converter Block Diagram**



## Mode Settings

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

### Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting bit *sd\_low\_noise* = 1.

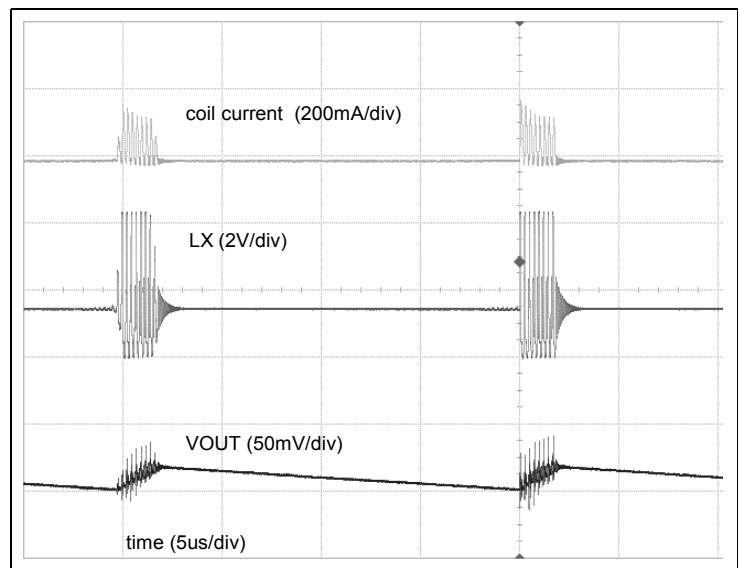
In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current, the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. Resultant the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to  $t_{\text{MIN\_ON}}$  to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small, that less than the minimum on time of the PMOS would be needed to keep the loop in regulation, the regulator will enter low power mode operation.

The crossover point is about 15mA for  $V_{\text{IN}} = 3\text{V}$ ,  $V_{\text{OUT}} = 1.2\text{V}$ ,  $1\mu\text{H}$ , 4MHz.

**Figure 9:**  
DC/DC Buck Low Noise Mode

**DC/DC Buck Low Noise Mode:** Shows the DC/DC switching waveforms for low noise operation.



**High-Efficiency Operation (Default Setting)**

High-efficiency operation is enabled by setting bit *sd\_low\_noise* = 0.

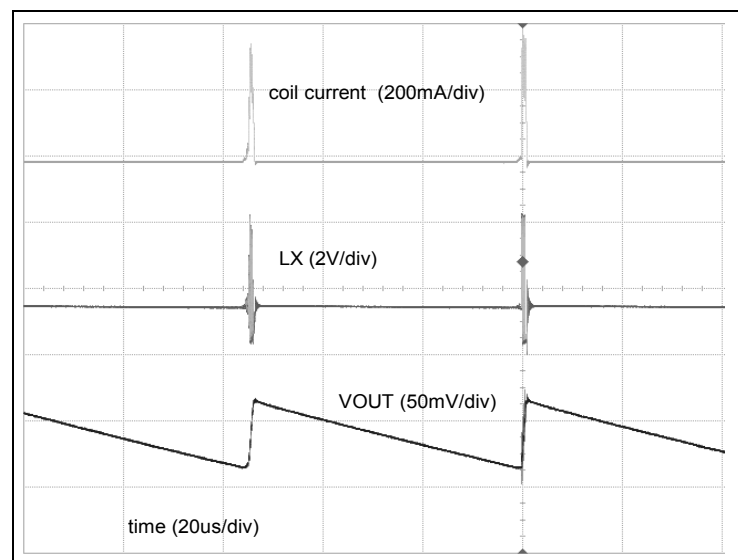
In this mode there is a minimum coil current necessary before switching OFF the PMOS. Resultant there are less pulses necessary at low output loads, and therefore the efficiency increases. As drawback, this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for  $V_{IN} = 3V$ ,  $V_{OUT} = 1.2V$ ,  $1\mu H$ , 4MHz)

**Figure 10:**  
**DC/DC Buck High Efficiency Mode**

**DC/DC Buck High Efficiency Mode:**

Shows the DC/DC switching waveforms for high efficiency operation

**Low Power Mode Operation (Automatically Controlled)**

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two additional guard bands, based on comparators, are set at  $\pm 5\%$  of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

### ***DVM (Dynamic Voltage Management)***

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see *sd\_dvm\_select* and *dvm\_time* description)

### ***Fast Regulation Mode***

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a 22µF output capacitor instead the 10µF one to guarantee the stability of the regulator.

The mode is enabled by setting *sd\_fast* = 1.

### ***Selectable Frequency Operation***

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency can be set to 2, 3 or 4MHz and this mode is selected by setting *sd\_freq* and *sd\_fsel* to the appropriate values.

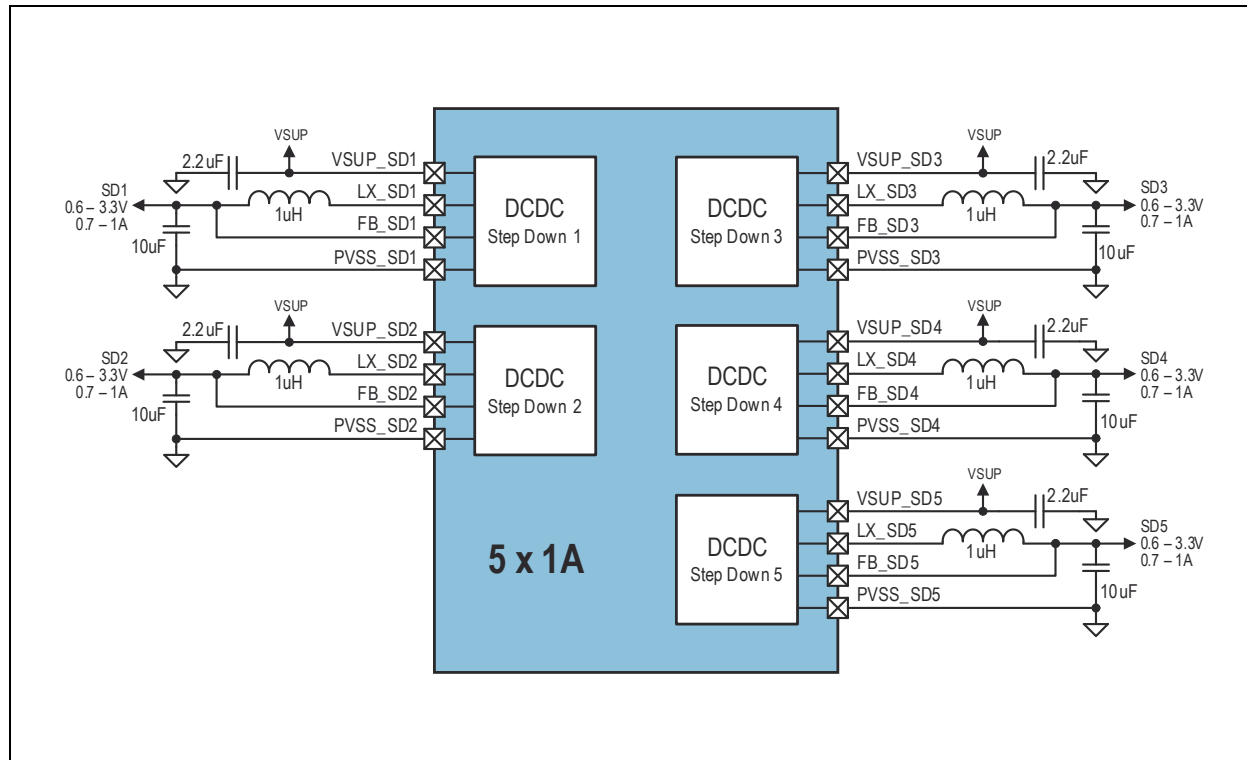
### ***100% PMOS ON Mode for Low Dropout Regulation***

For low input to output voltage difference the DC/DC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

### Step Down Converter Configuration Modes

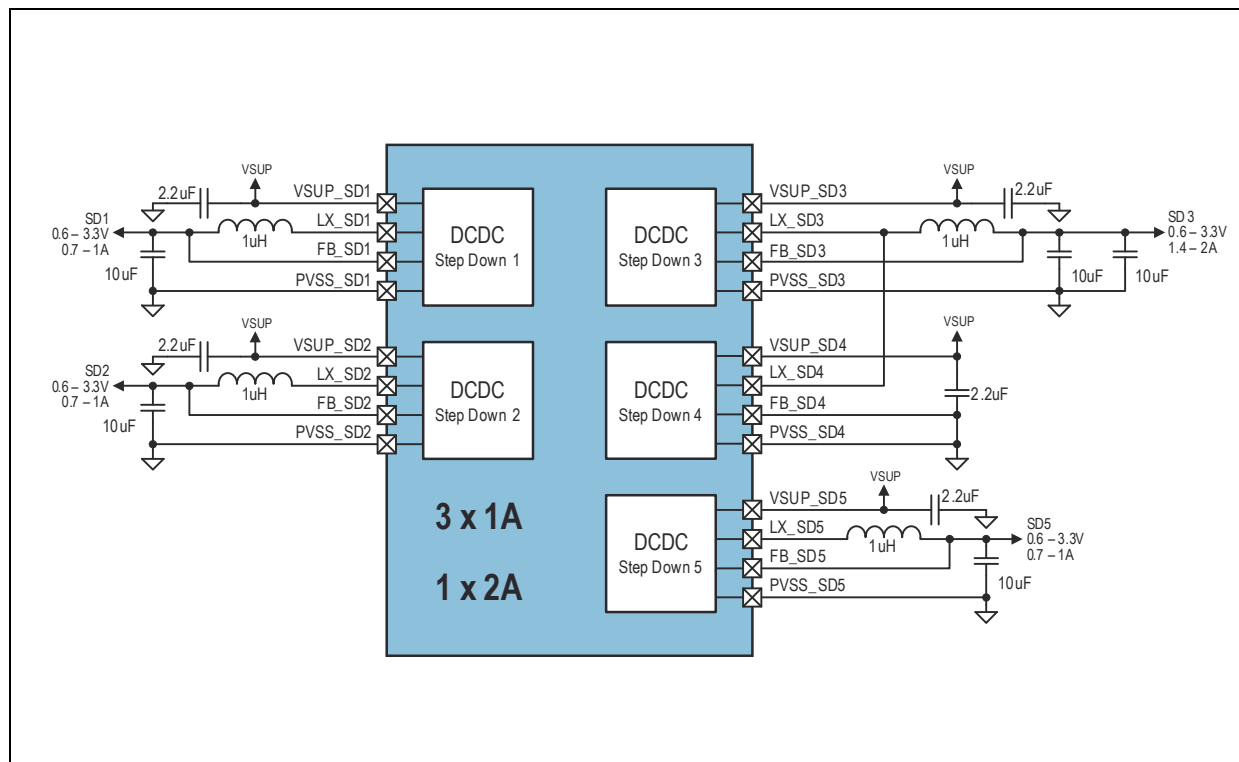
The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd2\_slave*, *sd4\_slave* and *sd5\_slave* (the default is set by the Boot-OTP).

**Figure 11:**  
**DC/DC Step Down Normal Operating Mode**



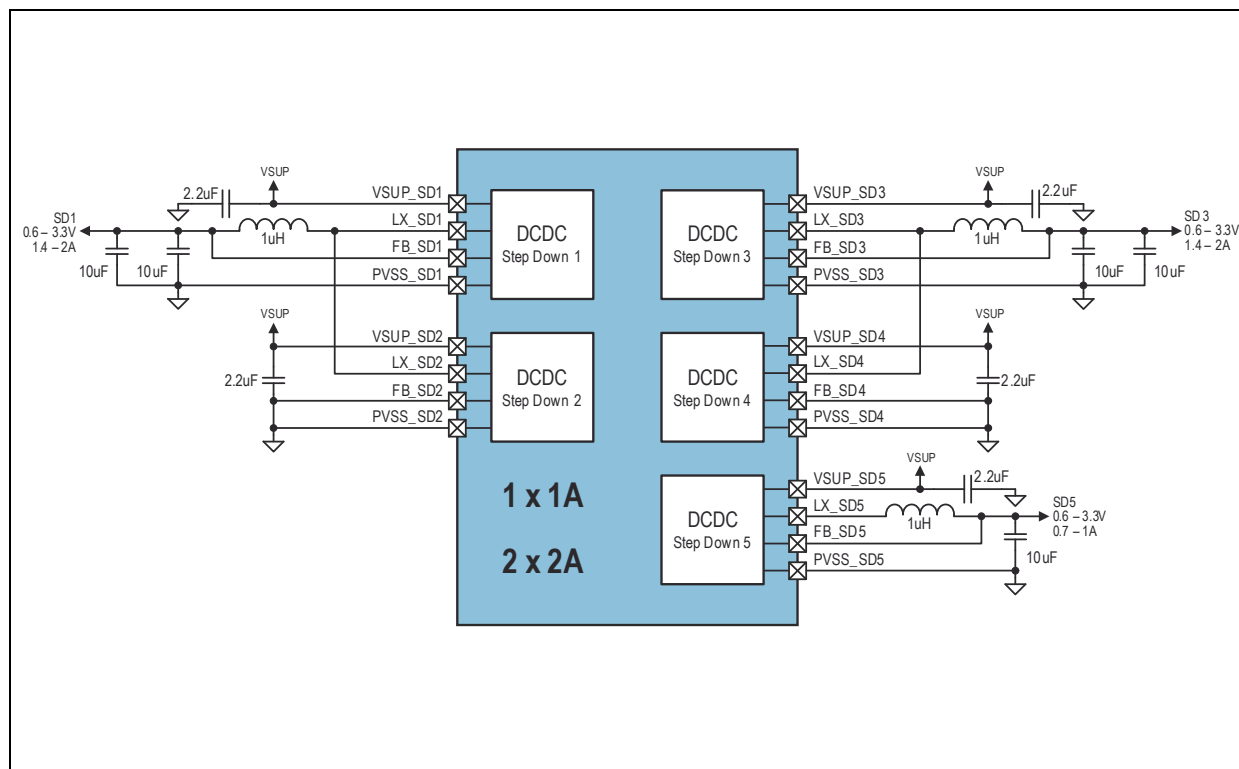
**Normal Operating Mode:** *sd2\_slave* = 0, *sd4\_slave* = 0, *sd5\_slave* = 0

**Figure 12:**  
**DC/DC Step Down SD3/SD4 Operating Mode**



**SD3/SD4 Operating Mode:** sd2\_slave = 0, sd4\_slave = 1, sd5\_slave = 0

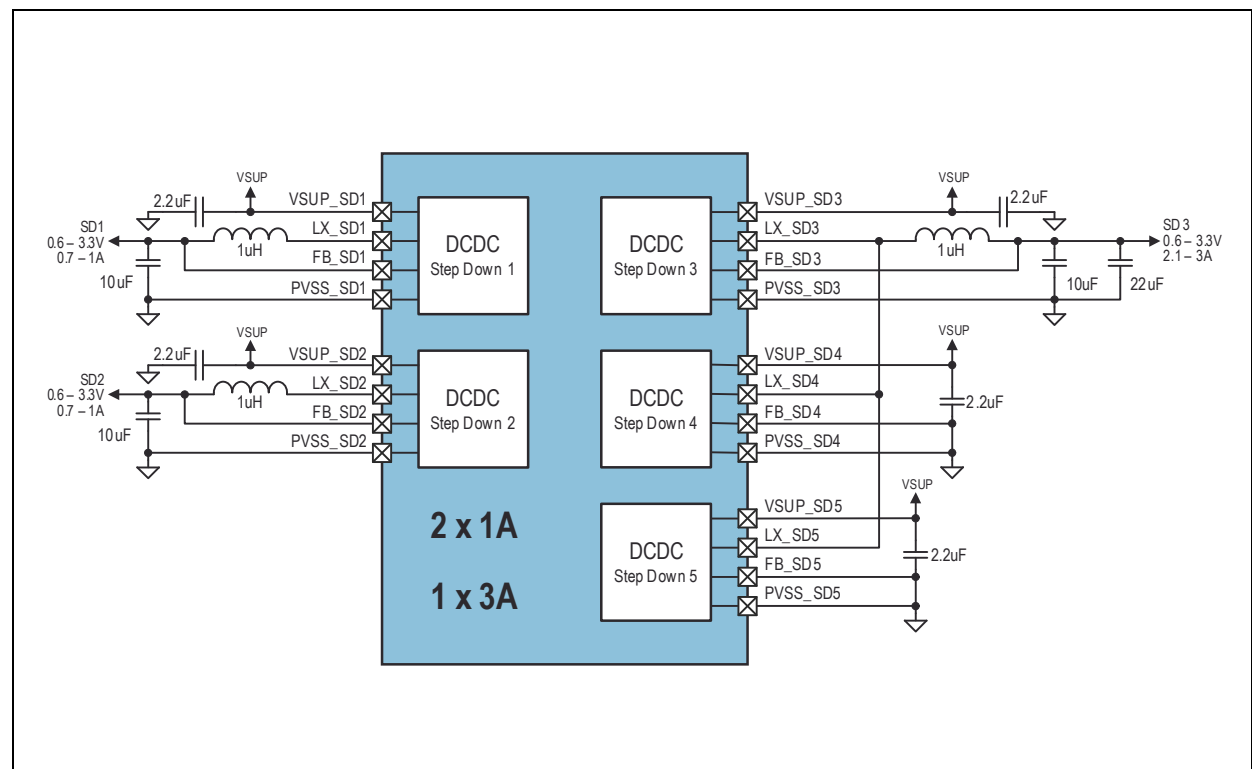
**Figure 13:**  
**DC/DC Step Down SD1/SD2 & SD3/SD4 Operating Mode**



**SD3/SD4 & SD4/SD5 Operating Mode:** sd2\_slave = 1, sd4\_slave = 1, sd5\_slave = 0

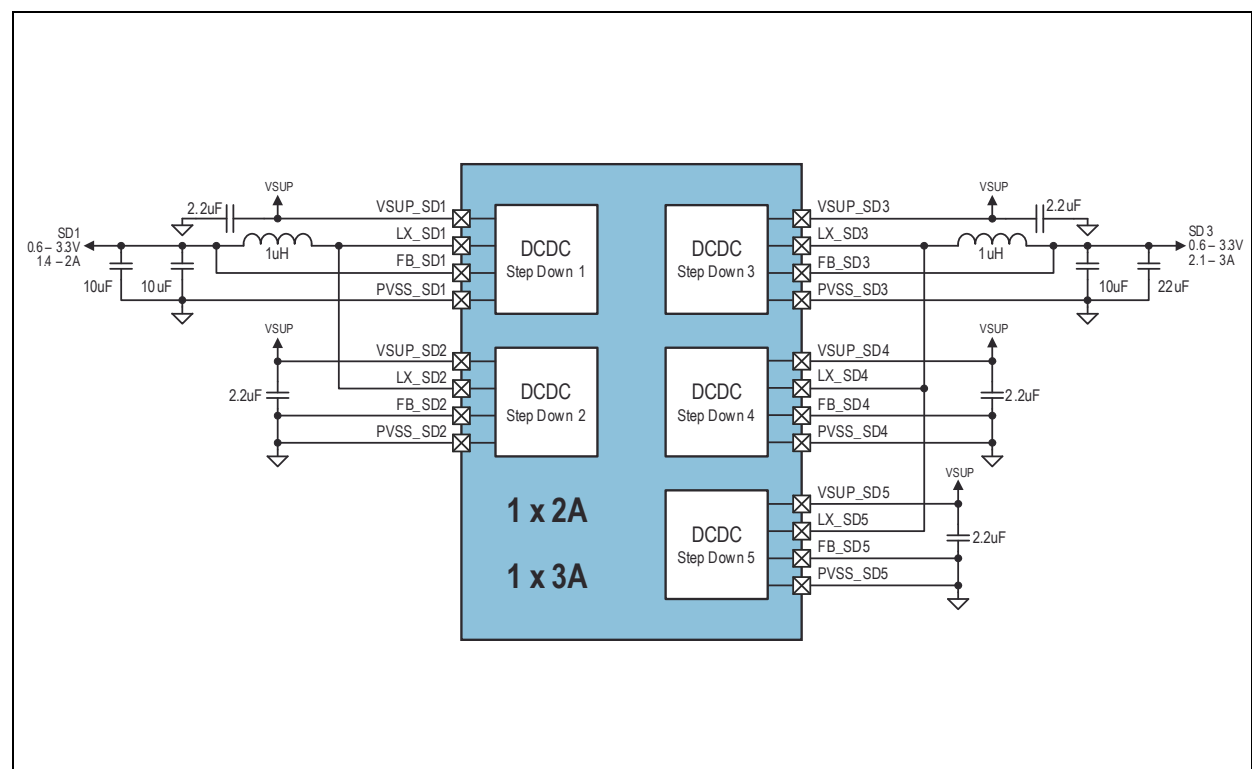


### Figure 14: DC/DC Step Down SD3/SD4/SD5 Operating Mode



**SD3/SD4/SD5 Operating Mode:** sd2\_slave = 0, sd4\_slave = 1, sd5\_slave = 1

**Figure 15:**  
**DC/DC Step Down SD1/SD2 & SD3/SD4/SD5 Operating**



**SD1/SD2 & SD3/SD4/SD5 Operating Mode:** sd2\_slave = 1, sd4\_slave = 1, sd5\_slave = 1

## Parameters

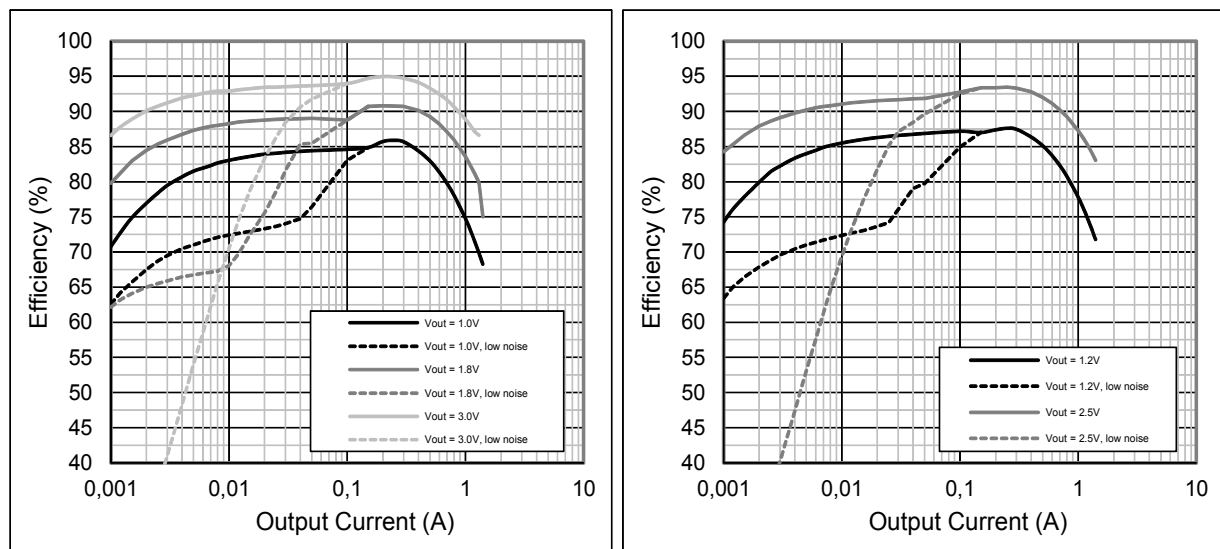
**Figure 16:**  
**Step Down DC/DC Converter Electrical Characteristics**

| Symbol           | Parameter                | Conditions                                                | Min    | Typ  | Max  | Unit     |
|------------------|--------------------------|-----------------------------------------------------------|--------|------|------|----------|
| $V_{IN}$         | Input Voltage            | Pin $V_{SUP}$                                             | 2.7    |      | 5.5  | V        |
| $V_{OUT}$        | Regulated Output Voltage |                                                           | 0.6125 |      | 3.35 | V        |
| $V_{OUT\_TOL}$   | Output Voltage Tolerance | min. 40mV                                                 | -3     |      | +3   | %        |
| $I_{LIMIT}$      | Current Limit            |                                                           |        | 1.2  |      | A        |
| $R_{PMOS}$       | P-Switch ON Resistance   |                                                           |        | 0.25 | 0.5  | $\Omega$ |
| $R_{NMOS}$       | N-Switch ON Resistance   |                                                           |        | 0.25 | 0.5  | $\Omega$ |
| $f_{SW}$         | Switching Frequency      | $sdX\_frequ = 1$<br>$sdX\_fsel = 1$<br>$fclk\_int = 4MHz$ |        | 4    |      | MHz      |
|                  |                          | $sdX\_frequ = 1$<br>$sdX\_fsel = 0$<br>$fclk\_int = 4MHz$ |        | 3    |      | MHz      |
|                  |                          | $sdX\_frequ = 0$<br>$sdX\_fsel = 0$<br>$fclk\_int = 4MHz$ |        | 2    |      | MHz      |
| $I_{LOAD}$       | Load Current             | $V_{OUT} \leq 1.8V$                                       | 0      |      | 1    | A        |
|                  |                          | $V_{OUT} > 1.8V$                                          | 0      |      | 0.7  |          |
| $I_{SUP\_DC/DC}$ | Current Consumption      | Operating current without load                            |        | 60   |      | $\mu A$  |
|                  |                          | Shutdown current                                          |        | 0.1  |      |          |
| $t_{MIN\_ON}$    | Minimum ON Time          |                                                           |        | 40   |      | ns       |
| $\eta_{EFF}$     | Efficiency               | See figures below                                         |        |      |      | %        |

**Figure 17:**  
**Step Down DC/DC External Components**

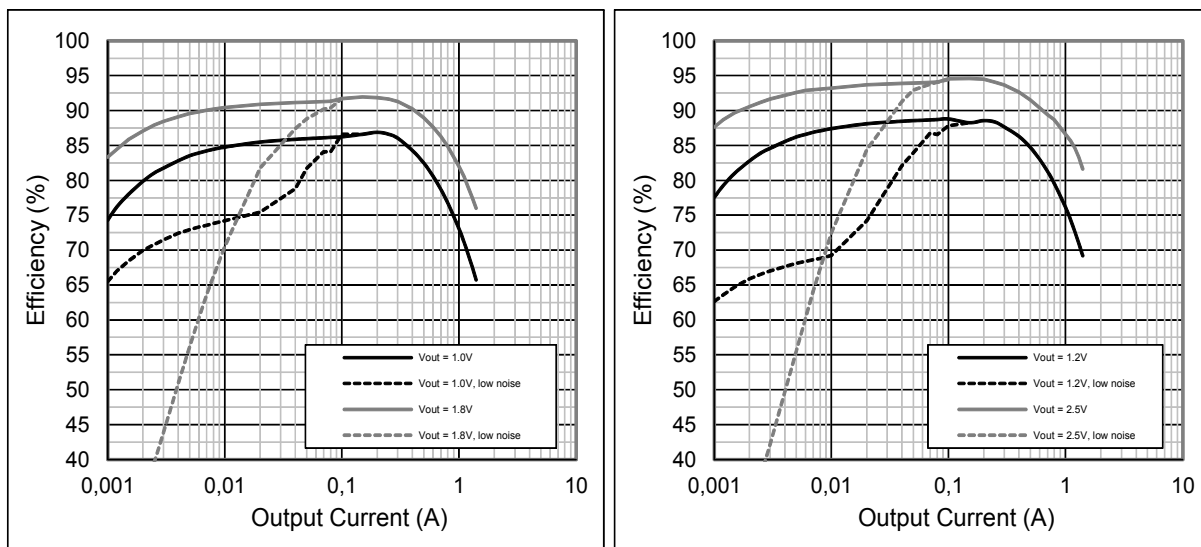
| Symbol          | Parameter        | Conditions         | Min | Typ | Max | Unit    |
|-----------------|------------------|--------------------|-----|-----|-----|---------|
| $C_{FB\_SDx}$   | Output Capacitor | Ceramic X5R or X7R | 8   | 10  |     | $\mu F$ |
| $C_{VSUP\_SDx}$ | Input Capacitor  | Ceramic X5R or X7R |     | 2.2 |     | $\mu F$ |
| $L_{SDx}$       | Inductor         | 4MHz operation     |     | 1   |     | $\mu H$ |
|                 |                  | 3MHz operation     |     | 1   |     |         |
|                 |                  | 2MHz operation     |     | 2.2 |     |         |

**Figure 18:**  
**DC/DC SD1 Efficiency vs. Output Current**



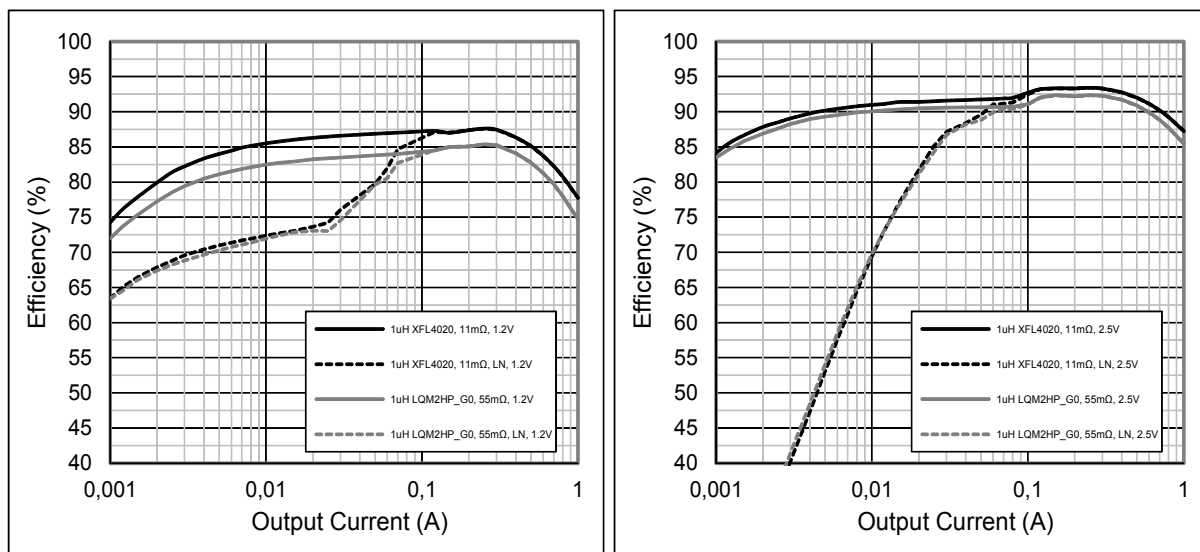
**SD1 Efficiency vs. Output Current:**  $V_{IN} = 3.7V$ , 3MHz operation, XFL4020  $1\mu H$  coil,  $T_A = 25^\circ C$

**Figure 19:**  
DC/DC SD1 Efficiency vs. Output Current



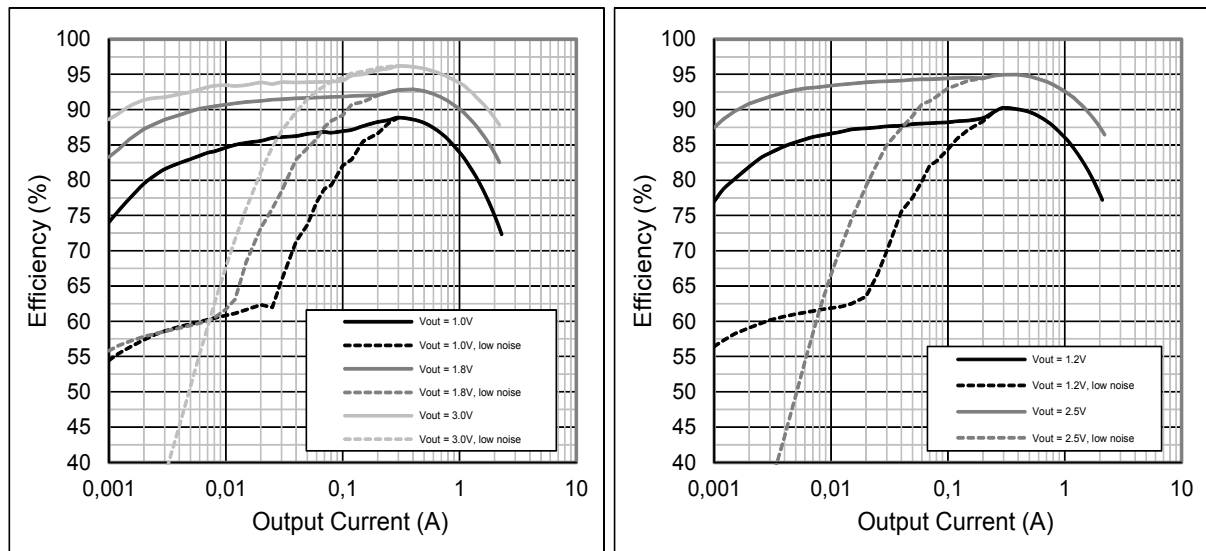
SD1 Efficiency vs. Output Current:  $V_{IN} = 3.0V$ , 3MHz operation, XFL4020 1 $\mu$ H coil,  $T_A = 25^\circ C$

**Figure 20:**  
DC/DC SD1 Efficiency vs. Output Current



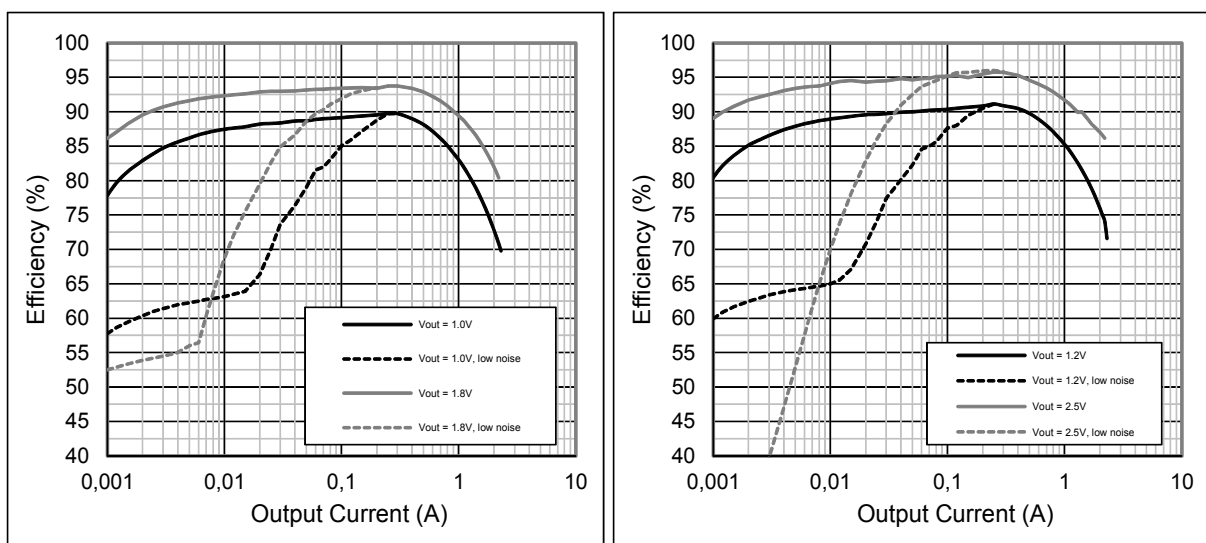
SD1 Efficiency vs. Output Current:  $V_{IN} = 3.7V$ ,  $V_{OUT} = 1.2V/2.5V$ , 3MHz operation,  $T_A = 25^\circ C$

**Figure 21:**  
DC/DC SD1 + SD2 Efficiency vs. Output Current



SD1 + SD2 Efficiency vs. Output Current:  $V_{IN} = 3.7V$ , 3MHz operation, XFL4020 1 $\mu H$  coil,  $T_A = 25^\circ C$

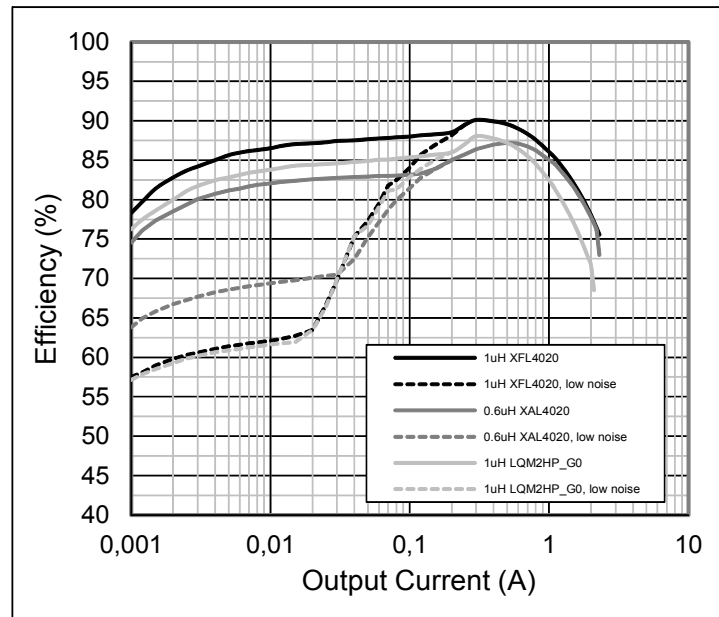
**Figure 22:**  
DC/DC SD1 + SD2 Efficiency vs. Output Current



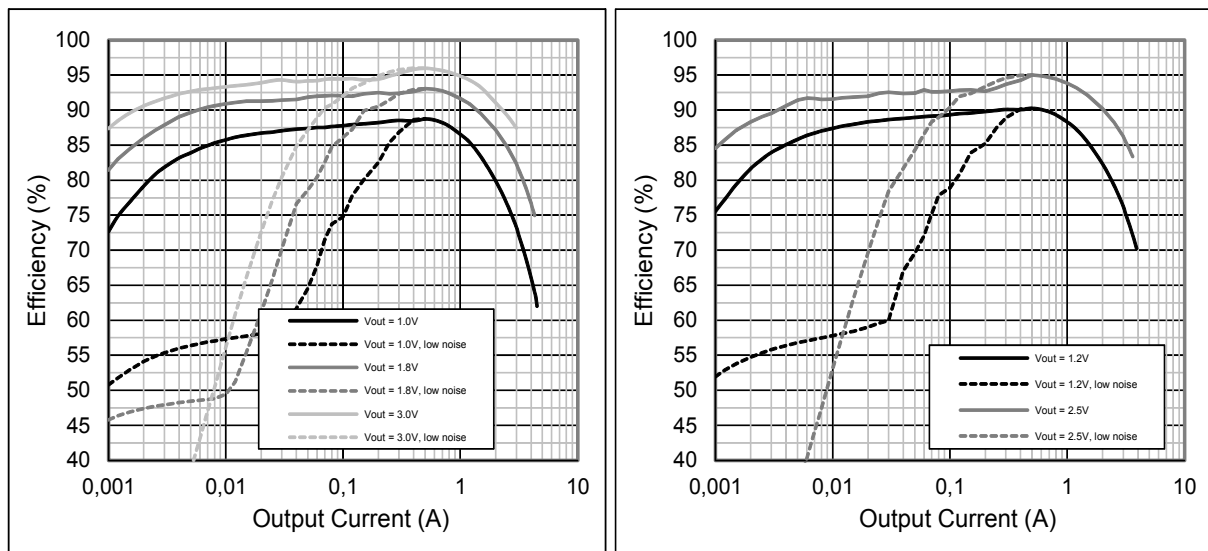
SD1 + SD2 Efficiency vs. Output Current:  $V_{IN} = 3.0V$ , 3MHz operation, XFL4020 1 $\mu H$  coil,  $T_A = 25^\circ C$

**Figure 23:**  
DC/DC SD1 + SD2 Efficiency vs. Output Current

**SD1 + SD2 Efficiency vs. Output Current:**  $V_{IN} = 3.7V$ ,  $V_{OUT} = 1.2V$ , 3MHz operation,  $T_A = 25^\circ C$

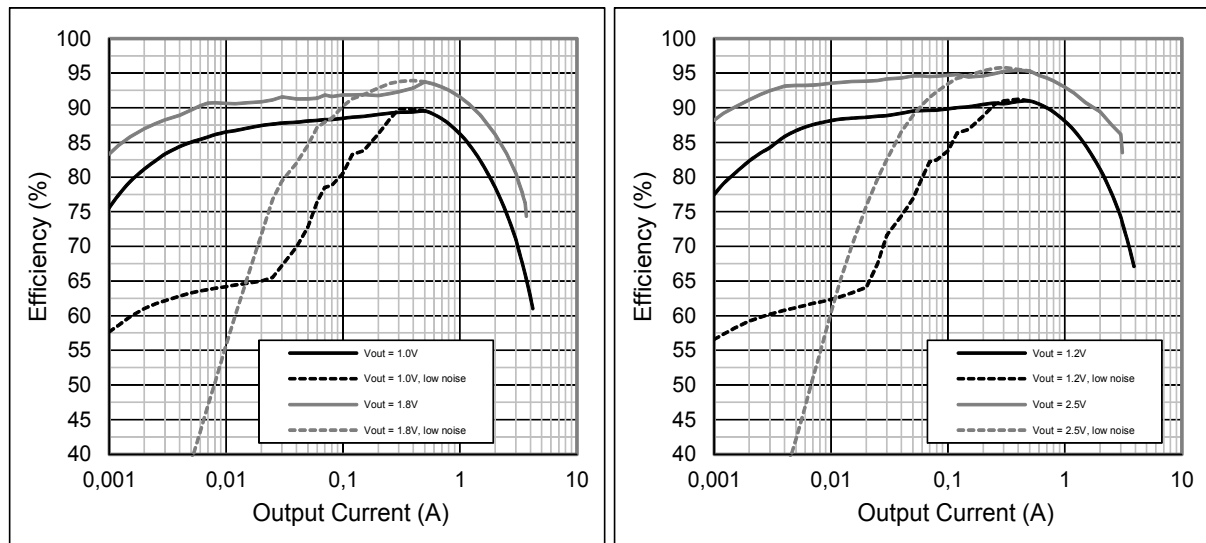


**Figure 24:**  
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current



**SD3 + SD4 + SD5 Efficiency vs. Output Current:**  $V_{IN} = 3.7V$ , 3MHz operation, XFL4020 1μH coil,  $T_A = 25^\circ C$

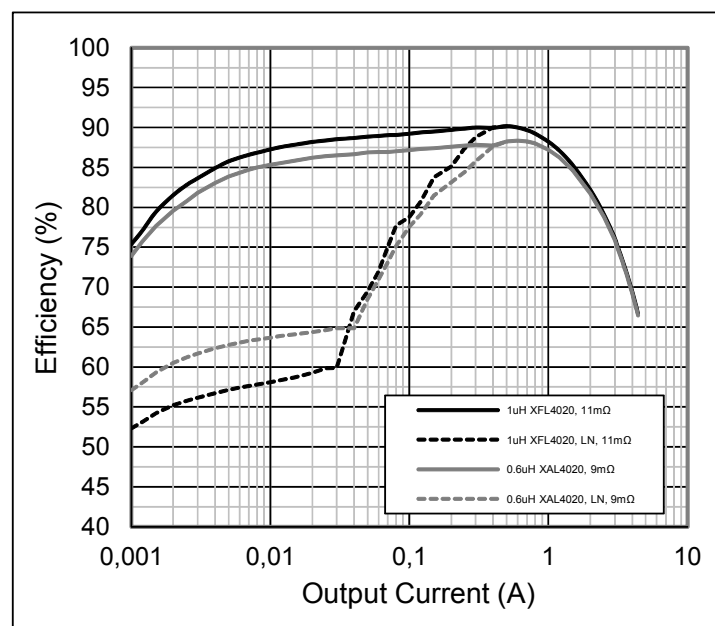
**Figure 25:**  
**DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current**



**SD3 + SD4 + SD5 Efficiency vs. Output Current:**  $V_{IN} = 3.0V$ , 3MHz operation, XFL4020 1 $\mu$ H coil,  $T_A = 25^\circ C$

**Figure 26:**  
**DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current**

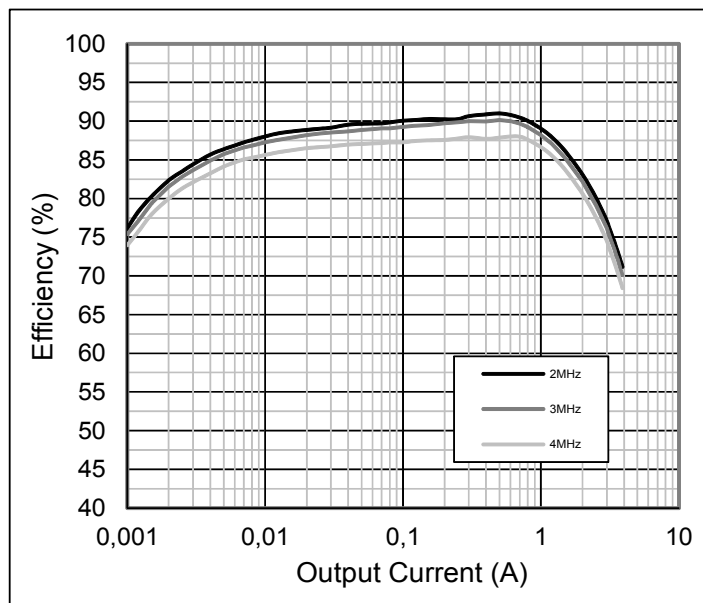
**SD3 + SD4 + SD5 Efficiency vs. Output Current:**  $V_{IN} = 3.7V$ ,  $V_{OUT} = 1.2V$ , 3MHz operation,  $T_A = 25^\circ C$



**Figure 27:**  
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current

**SD3 + SD4 + SD5 Efficiency vs. Output**

**Current:**  $V_{IN} = 3.7V$ ,  $V_{OUT} = 1.2V$ ,  
XFL4020 1 $\mu$ H coil,  $T_A = 25^\circ C$

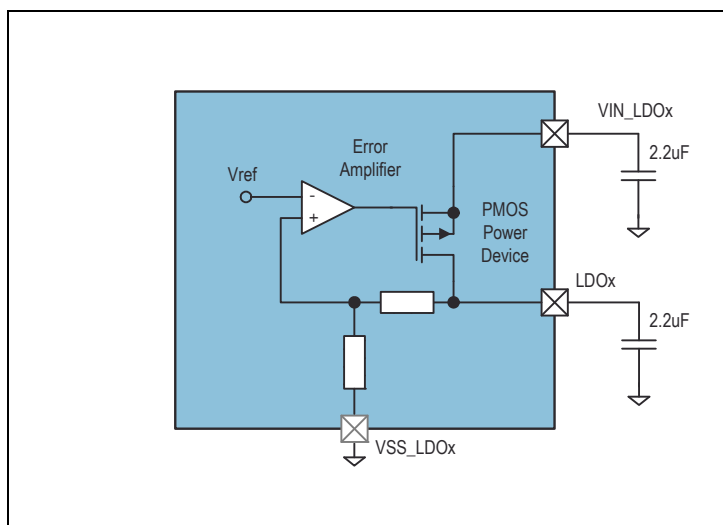


**Universal IO LDO Regulators**

2 universal IO range LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.8 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

**Figure 28:**  
Universal IO LDO Block Diagram

**AS3709 LDO:** Shows the detailed Universal IO LDO Block Diagram





**Parameter**

**Figure 29:**  
**Universal IO LDO Electrical Characteristics**

| Symbol         | Parameter                     | Note                                                                             | Min   | Typ   | Max | Unit          |
|----------------|-------------------------------|----------------------------------------------------------------------------------|-------|-------|-----|---------------|
| $V_{IN}$       | Input Voltage Range           | Pin VIN_LDOx                                                                     | 1.75  |       | 5.5 | V             |
| $V_{OUT\_TOL}$ | Output Voltage Tolerance      | Min. 40mV                                                                        | -3    |       | +3  | %             |
| $V_{OUT}$      | Output Voltage Range          | Pin LDOx<br>$I_{OUT} < 150\text{mA}$ , 25mV steps                                | 0.825 |       | 3.3 | V             |
| $I_{OUT\_L}$   | Output Current <sup>(1)</sup> | $I_{doX\_ilimit} = 0$ (150mA)                                                    | 0     |       | 150 | mA            |
| $I_{LIMIT\_L}$ | Current Limit <sup>(1)</sup>  |                                                                                  |       | 300   |     | mA            |
| $I_{OUT\_H}$   | Output Current <sup>(1)</sup> | $I_{doX\_ilimit} = 1$ (300mA)                                                    | 0     |       | 300 | mA            |
| $I_{LIMIT\_H}$ | Current Limit <sup>(1)</sup>  |                                                                                  |       | 500   |     | mA            |
| $R_{ON}$       | On Resistance                 | LDO1, LDO2                                                                       |       | 0.6   |     | $\Omega$      |
| PSRR           | Power Supply Rejection Ratio  | $f=1\text{kHz}$                                                                  | 60    |       |     | dB            |
|                |                               | $f=100\text{kHz}$                                                                | 30    |       |     |               |
| $I_{OFF}$      | Shut Down Current             |                                                                                  |       | 100   |     | nA            |
| $I_Q$          | Quiescent Current             | Without load                                                                     |       | 30    | 43  | $\mu\text{A}$ |
| $t_{START}$    | Startup Time                  | Low current used during start-up                                                 |       |       | 500 | $\mu\text{s}$ |
| $V_{LNR}$      | Line Regulation               | Static                                                                           |       | 0.07  |     | %/V           |
|                |                               | Transient; Slope:<br>$t_r=15\mu\text{s}$ ; $\Delta 1\text{V}$                    |       | 20    |     | mV            |
| $V_{LDR}$      | Load Regulation               | Static                                                                           |       | 0.014 |     | %/mA          |
|                |                               | Transient; Slope:<br>$t_r=15\mu\text{s}$ ; $1\text{mA} \rightarrow 300\text{mA}$ |       | 30    |     | mV            |

**Note(s):**

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

**Figure 30:**  
**Universal IO LDO Electrical Characteristics**

| Symbol          | Parameter        | Note               | Min | Typ | Max | Unit    |
|-----------------|------------------|--------------------|-----|-----|-----|---------|
| $C_{OUT\_LDOx}$ | Output Capacitor | Ceramic X5R or X7R | 0.7 | 2.2 |     | $\mu F$ |
| $C_{VIN\_LDOx}$ | Input Capacitor  | Ceramic X5R or X7R | 1   | 2.2 |     | $\mu F$ |

### Low Power LDO V2\_5 Regulator

The low power LDO V2\_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption and still offering reasonable characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 0.7 $\mu F$  must be connected to the output.

#### Parameter

**Figure 31:**  
**Low Power V2\_5 LDO Electrical Characteristics**

| Symbol      | Parameter            | Note                                                               | Min | Typ | Max | Unit     |
|-------------|----------------------|--------------------------------------------------------------------|-----|-----|-----|----------|
|             | Supply Voltage Range | See $V_{SUP}$                                                      |     |     |     |          |
| $V_{OUT}$   | Output Voltage       |                                                                    | 2.4 | 2.5 | 2.6 | V        |
| $R_{ON}$    | On Resistance        | Guaranteed by design                                               |     | 50  |     | $\Omega$ |
| $I_{OFF}$   | Shut Down Current    |                                                                    |     | 100 |     | nA       |
| $I_Q$       | Quiescent Current    | Guaranteed by design, consider chip internal load for measurements |     | 3   |     | $\mu A$  |
| $t_{START}$ | Startup Time         |                                                                    |     | 200 |     | $\mu s$  |

**Figure 32:**  
**Universal IO LDO Electrical Characteristics**

| Symbol      | Parameter        | Note               | Min | Typ | Max | Unit    |
|-------------|------------------|--------------------|-----|-----|-----|---------|
| $C_{V2\_5}$ | Output Capacitor | Ceramic X5R or X7R | 0.7 | 1   |     | $\mu F$ |

## Detailed Description - System Functions

### Start-Up

#### Normal Start-Up

During a normal reset cycle (e.g. after the battery is inserted), after  $V_{2\_5}$  is above  $V_{POR}$  and  $V_{SUP}$  is above  $ResVoltRise$  a normal startup happens:

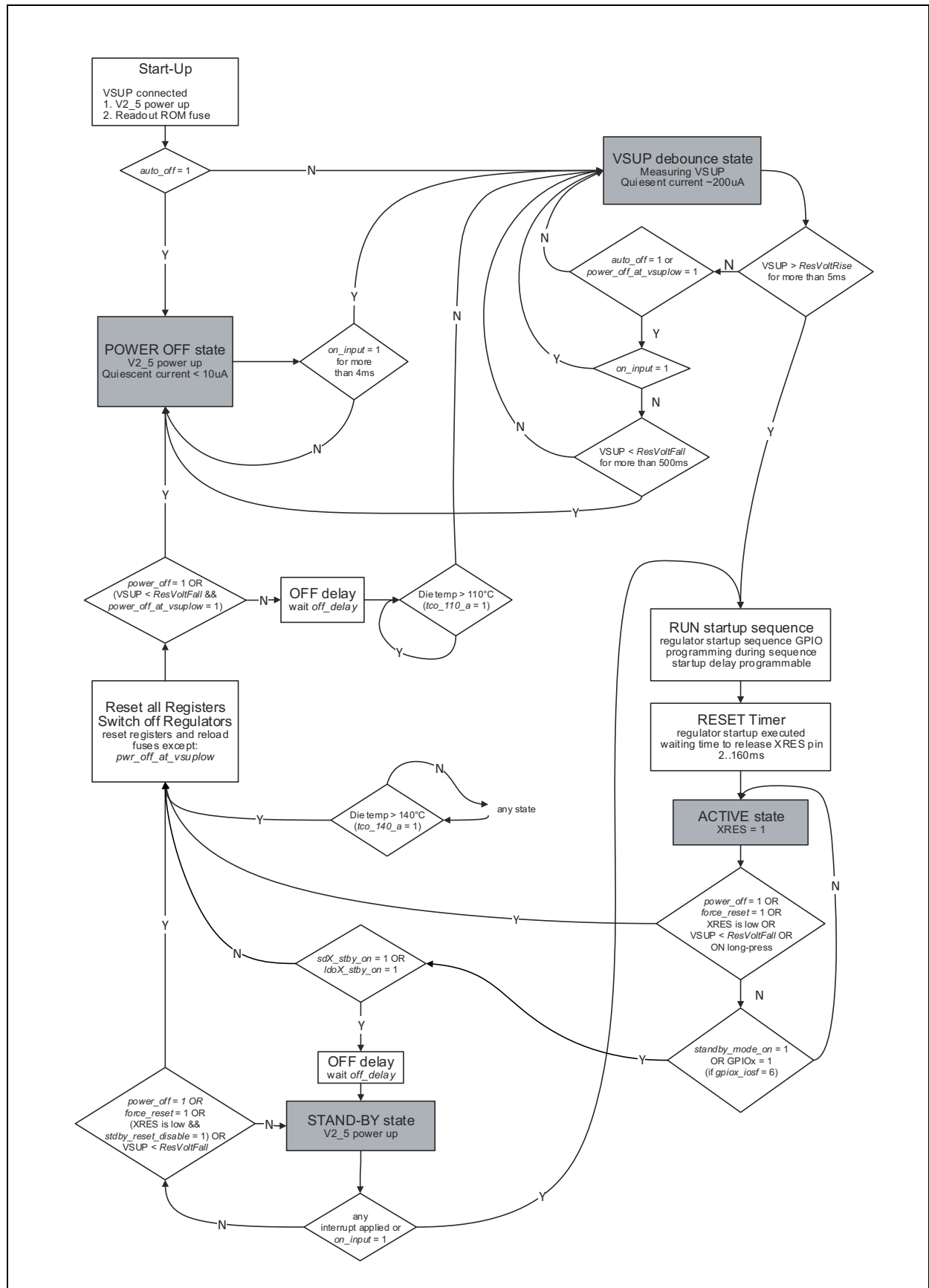
- Configuration of DC/DCs (combined mode or separated) is read from the Boot-OTP
- Startup state machine reads out the internal Boot-OTP
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset-Timer expires (external pin XRES)

#### Parameter

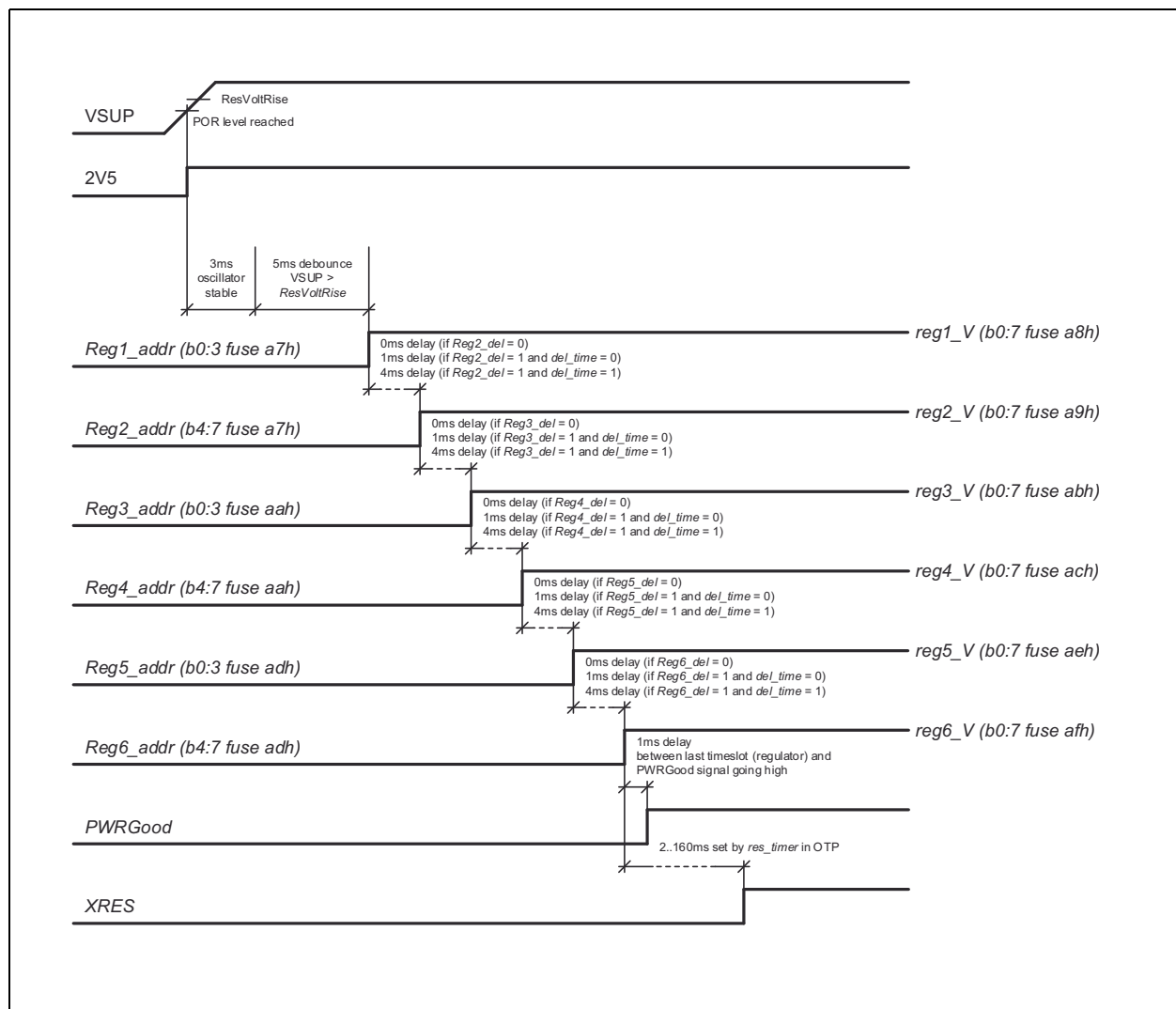
**Figure 33:**  
**ON Input Start-Up Condition**

| Symbol       | Parameter             | Note | Min | Typ | Max | Unit    |
|--------------|-----------------------|------|-----|-----|-----|---------|
| $V_{ON\_IL}$ | ON Low Level Voltage  |      |     |     | 0.4 | V       |
| $V_{ON\_IH}$ | ON High Level Voltage |      | 1.4 |     |     | V       |
| $I_{ON\_PD}$ | ON Pull Down Current  |      | 4   | 12  |     | $\mu A$ |

**Figure 34:**  
**Start-Up Flowchart**

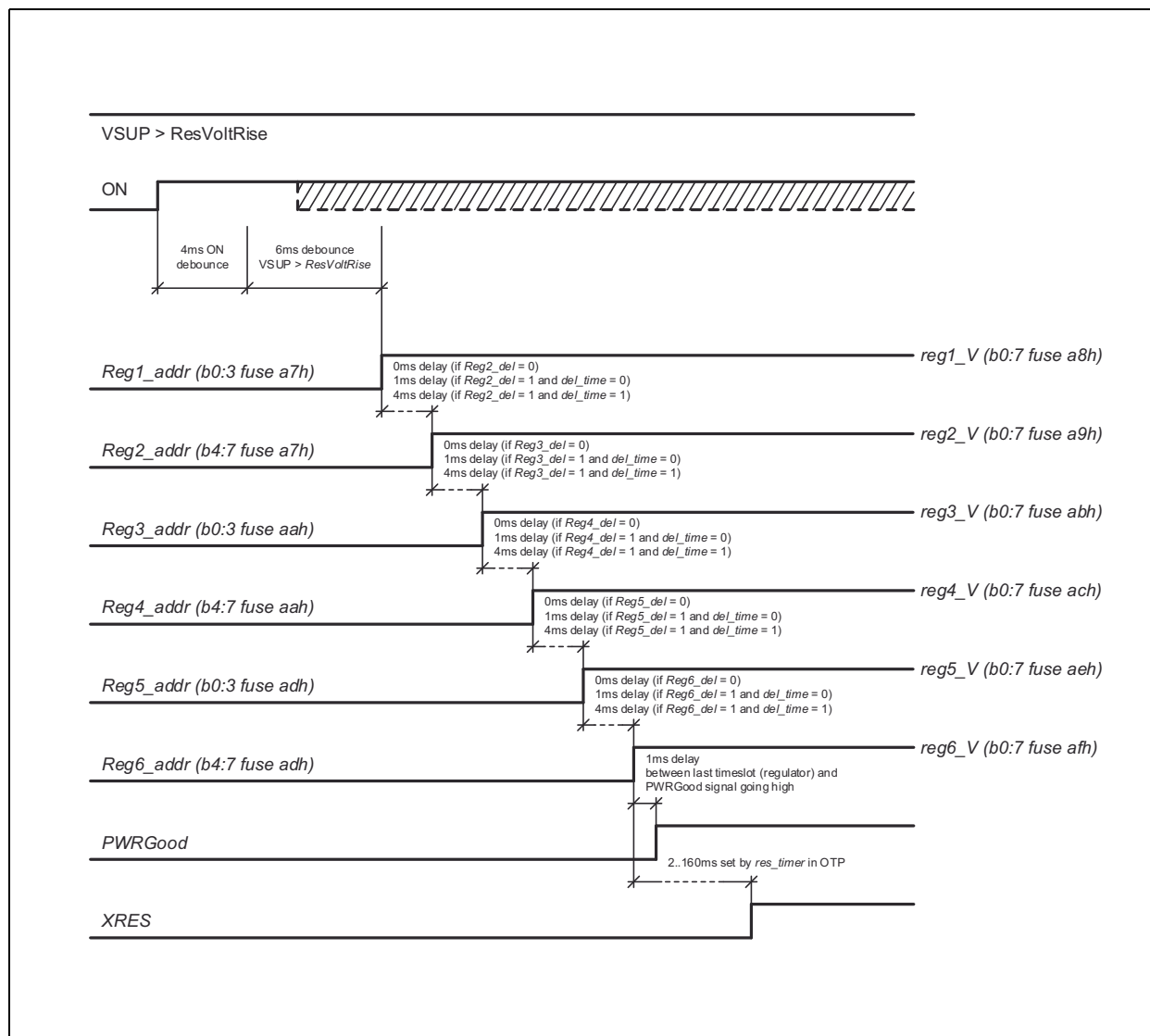


**Figure 35:**  
**Start-Up Sequence Diagram 1/3**



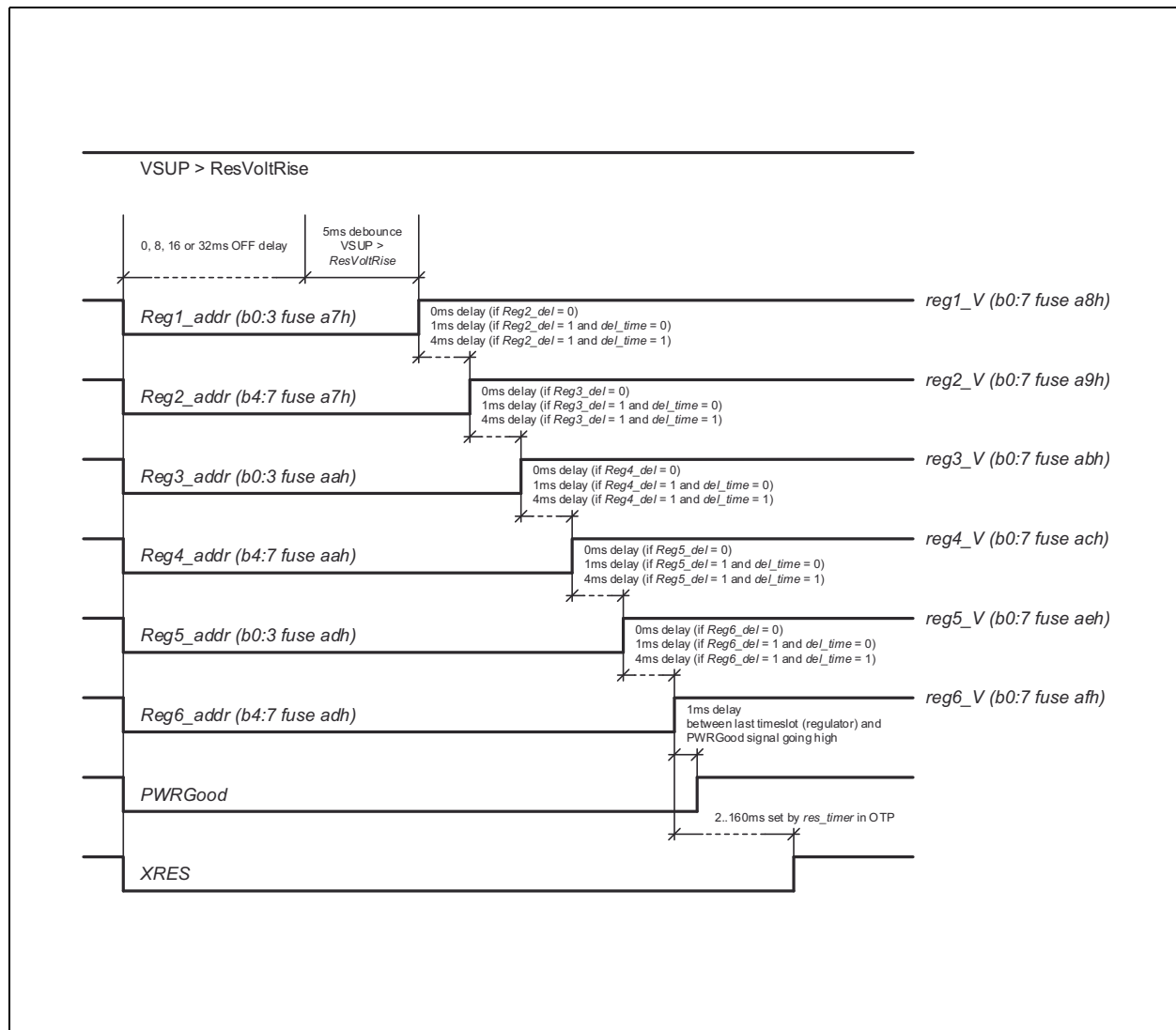
**Start-Up Sequence:** This diagram shows the timing of a startup from scratch (first VSUP connection)

**Figure 36:**  
**Start-Up Sequence Diagram 2/3**



**Start-Up Sequence:** This diagram shows the timing of a startup initiated by the ON-key press

**Figure 37:**  
**Start-Up Sequence Diagram 3/3**



**Start-Up Sequence:** This diagram shows the timing of a reset command followed by a startup

## Reset

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added. During each reset cycle the following states are controlled by the AS3709:

- Pin XRES is forced to GND
- Normal startup with programmable power-on sequence and regulator voltages
- Reset is active until the programmable reset timer (set by register bits *res\_timer*<2:0>) expires
- All registers are set to their default values after power-on, except the reset control- and status-registers

## RESET Reasons

Reset can be activated from 7 different sources:

- $V_{POR}$  has been reached ( $V_{SUP}$  reached POR level)
- ResVoltFall was reached ( $V_{SUP}$  drops below ResVoltFall)
- Software forced reset
- Power off mode
- External triggered through the pin XRES
- Overtemperature
- ON-key long press

## Voltage Detection

There are two types of voltage dependent resets:  $V_{POR}$  and  $V_{XRES}$ .  $V_{POR}$  monitors the voltage on V2\_5 and  $V_{XRES}$  monitors the voltage on  $V_{SUP}$ . The linear regulator for V2\_5 is always on and uses the voltage  $V_{SUP}$  as its source. The pin XRES is only released if V2\_5 is above  $V_{POR}$  and  $V_{SUP}$  is above ResVoltRise.

## Power OFF

To put the chip into ultralow power mode, write '1' into *power\_off*.

The chip stays in power off mode until

- The external pin ON is pulled high
- The  $V_{POR}$  level is touched to start a complete reset cycle

The bit *power\_off* is automatically cleared by this reset cycle.

During *power\_off* state all circuits are shut-off except the Low Power LDO (V2\_5). Thus the current consumption of AS3709 is reduced to less than 7µA. The digital part is supplied by V2\_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers, all other registers are set to their default value after power-on.



**Software Forced Reset**

Writing '1' into the register bit *force\_reset* immediately starts a reset cycle. The bit *force\_reset* is automatically cleared by this reset.

**External Triggered Reset**

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

**Overtemperature Reset**

The reset cycle can be started by overtemperature conditions.

**Long ON-Key Press**

When applying a high level on the ON input pin for 4s/8s (depending on *on\_reset\_delay*) a reset is initiated. This is thought as a safety feature when the SW hangs up.

**Parameter**

**Figure 38:**  
**XRES Input Characteristics**

| Symbol         | Parameter                | Note | Min | Typ | Max | Unit |
|----------------|--------------------------|------|-----|-----|-----|------|
| $V_{XRES\_IL}$ | RESET Low Level Voltage  |      |     |     | 0.4 | V    |
| $V_{XRES\_IH}$ | RESET High Level Voltage |      | 1.4 |     |     | V    |

**Figure 39:**  
**RESET Levels**

| Symbol                | Parameter                                                                                                                         | Note                                                              | Min | Typ                        | Max | Unit |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|-----|----------------------------|-----|------|
| V <sub>POR</sub>      | Overall Power On Reset                                                                                                            | Monitor voltage on V2_5 power on reset for all internal functions | 1.5 | 2.0                        | 2.3 | V    |
| V <sub>RES_RISE</sub> | RESET Level for V <sub>SUP</sub> Rising                                                                                           | Monitor voltage on V <sub>SUP</sub> rising level                  |     | ResVoltRise <sup>(1)</sup> |     | V    |
| V <sub>RES_FALL</sub> | RESET Level for V <sub>SUP</sub> Falling                                                                                          | Monitor voltage on V <sub>SUP</sub> falling level                 |     | 2.7                        |     | V    |
|                       |                                                                                                                                   | if <i>SupResEn</i> = 1 only                                       |     | ResVoltFall <sup>(2)</sup> |     | V    |
| V <sub>RES_MASK</sub> | Mask Time for V <sub>XRES_fall</sub><br>Duration for V <sub>SUP</sub> < ResVoltFall until a reset cycle is started <sup>(3)</sup> | <i>FastResEn</i> = 0                                              |     | 3                          |     | ms   |
|                       |                                                                                                                                   | <i>FastResEn</i> = 1                                              |     | 4                          |     | μs   |

**Note(s):**

1. The selection of the range and level is done via OTP. It's recommended to set the ResVoltRise level 200mV above the ResVoltFall level to have a hysteresis.
2. 2.7V is the default value, other levels can be set via SW.
3. XRES signal is debounced with the specified mask time for rising- and falling slope of VSUP
4. VRES\_FALL is only accepted if the reset condition is longer than VRES\_MASK. This guard time is used to avoid a complete reset of the system in case of short drops of VSUP.

**Figure 40:**  
**ResVoltRise/ResVoltFall Levels**

| Mode | 000  | 001  | 010  | 011  | 100  | 101  | 110  | 111  |
|------|------|------|------|------|------|------|------|------|
| 3.3V | 2.7V | 2.8V | 2.9V | 3.0V | 3.1V | 3.2V | 3.3V | 3.4V |
| 5.0V | 3.6V | 3.7V | 3.8V | 3.9V | 4.0V | 4.1V | 4.2V | 4.4V |

**Note(s):**

1. If bit reslevel\_5V is "1", then the 5.0V mode is selected.

## Stand-By

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or GPIO of the PMU. The interrupt has to be enabled and GPIO has to be configured before going to stand-by.

**Figure 41:**  
Stand-By

| State          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Enter via GPIO | <p>To enter stand-by mode the following settings have to be done:</p> <ul style="list-style-type: none"> <li>• Enable just these IRQ sources which should lead to leave stand-by mode.</li> <li>• Make sure that IRQ is inactive (IRQ flags get cleared by register reading)</li> <li>• Set the GPIO to input (<i>gpioX_mode</i> = 0)</li> <li>• Set the GPIO for stand-by control (<i>gpioX_iosf</i> = 6)</li> <li>• Set <i>regX_select</i> to define the sequence for going into stand-by for up to 3 regulators</li> <li>• Set <i>regX_voltage_stby</i> if another voltage is needing during stand-by</li> <li>• Define which regulators should be kept powered during stand-by (<i>sdX_stby_on</i> and <i>ldoX_stby_on</i>)</li> <li>• Activate the selected GPIO</li> </ul> |
| Enter via SW   | <p>To enter stand-by mode the following settings have to be done:</p> <ul style="list-style-type: none"> <li>• Enable just these IRQ sources which should lead to leave stand-by mode.</li> <li>• Make sure that IRQ is inactive (IRQ flags get cleared by register reading)</li> <li>• Define which regulators should be kept powered during stand-by (<i>sdX_stby_on</i> and <i>ldoX_stby_on</i>)</li> <li>• Set the delay for going into stand-by after the SW command (<i>off_delay</i>)</li> <li>• Set <i>standby_mode_on</i> to 1</li> </ul>                                                                                                                                                                                                                               |
| Stand-By       | <p>V2_5 chip supply is kept ON<br/>All other regulators are switched OFF dependent on the bits <i>sdX_stby_on</i> and <i>ldoX_stby_on</i><br/>XRES goes active (can be disabled with <i>standby_reset_disable</i>) and <i>pwr_good</i> goes inactive</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Leave          | <p>The chip will come out of stand-by with</p> <ul style="list-style-type: none"> <li>• IRQ activation or</li> <li>• GPIO control (if entered via GPIO)</li> </ul> <p>Start-Up sequence is provided defined by the boot ROM.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## Internal References

### Low Power Mode

Use bit *low\_power\_on* to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3709 by 45µA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

**Note(s):** Low power mode can be controlled by the serial interface.

**Figure 42:**  
**Reference Parameter**

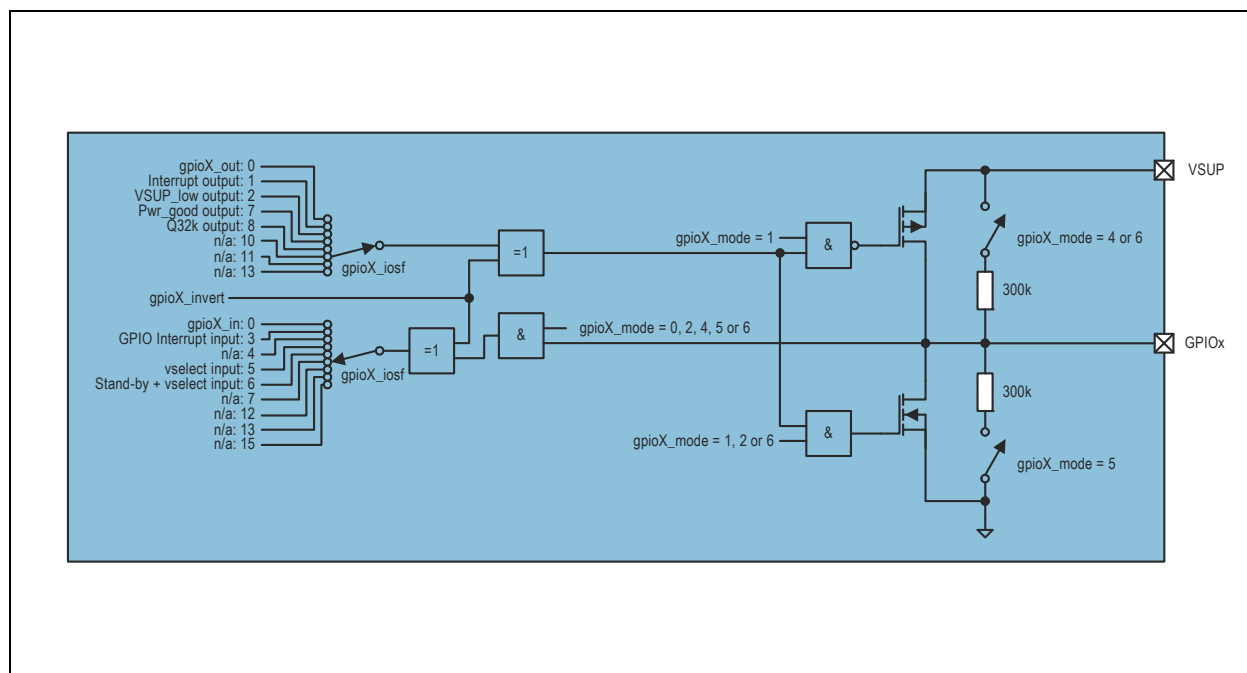
| Symbol    | Parameter                            | Note                                                         | Min | Typ       | Max | Unit |
|-----------|--------------------------------------|--------------------------------------------------------------|-----|-----------|-----|------|
| $f_{CLK}$ | Accuracy of Internal Reference Clock | Adjustable by serial interface register <code>clk_int</code> | -12 | $f_{CLK}$ | +12 | %    |

## GPIO Pins

The device contains 2 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), push-pull output or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

The polarity of the input and output signals can be inverted with the corresponding *gpioX\_invert* bit, all further descriptions refer to normal (non-inverted) mode.

**Figure 43:**  
**GPIO Block Diagram**



**GPIO Block Diagram:** Shows the internal structure of the IO pads

**Figure 44:**  
**GPIO Pin Characteristics**

| Symbol          | Parameter                    | Note                                              | Min                 | Typ | Max             | Unit       |
|-----------------|------------------------------|---------------------------------------------------|---------------------|-----|-----------------|------------|
| $V_{GPIO\_max}$ | Max. Voltage on GPIO1/2 Pins | Pin $V_{SUP}$ is used as supply for the GPIO pins |                     |     | $V_{SUP} + 0.3$ | V          |
| $V_{OL}$        | Low Level Output Voltage     | $I_{OL}=+1mA$ digital output                      |                     |     | +0.4            | V          |
| $V_{OH}$        | High Level Output Voltage    | $I_{OH}=-1mA$ ; digital push-pull output          | $0.8 \cdot V_{SUP}$ |     |                 | V          |
| $V_{IL}$        | Low Level Input Voltage      | Digital input                                     |                     |     | 0.4             | V          |
| $V_{IH}$        | High Level Input Voltage     | Digital input                                     | 1.4                 |     |                 | V          |
| $I_{LEAKAGE}$   | Leakage Current              | High impedance                                    |                     |     | 10              | $\mu A$    |
| $R_{pull-up}$   | Pull-Up Resistance           | If enabled; $V_{SUP} = 3.6V$                      |                     | 300 |                 | k $\Omega$ |
| $R_{pull-down}$ | Pull-Down Resistance         | If enabled; $V_{SUP} = 3.6V$                      |                     | 300 |                 | k $\Omega$ |

**GPIO Pins:** Shows the key electrical parameter of the GPIO pins.  $V_{SUP}=2.7$  to  $5.5V$ ; unless otherwise mentioned.

## IO Functions

### Normal IO Operation

If set to input, the logic level of the signal present at the GPIOx pin can be read from *gpioX\_in*. If the output mode is chosen, *gpioX\_out* specifies the logic level of the GPIOx pin.

This mode is also used for the on/off control of the DC/DC and LDOs. The selection which regulator is controlled by which GPIO, is done with the *gpio\_ctrl\_sdX* or *gpio\_ctrl\_ldoX* bits. The *gpioX\_mode* should be set to input.

### Interrupt Output

GPIOx pin logic state is derived from the interrupt signal XINT. Whenever an interrupt is present the GPIOx pin will be pulled high.

The *gpioX\_mode* should be set to output.

### VSUP\_low Output

GPIOx pin will go high if  $V_{SUP}$  falls below ResVoltFall and SupResEn = 0.

The *gpioX\_mode* should be set to output.

### GPIO Interrupt Input

A falling or rising edge will set the *gpio\_int* bit.

The *gpioX\_mode* should be set to input.

### Vselect Input

As long as the GPIOx pin is high the DC/DCs and LDOs operate with the normal register settings. If the GPIOx pin goes low the settings will change to the ones stored in *regX\_voltage*. The *gpioX\_mode* should be set to input.

**Figure 45:**  
GPIO Vselect Modes

| gpio1_iosf | gpio2_iosf | Vselect Mode                                                                                                       |
|------------|------------|--------------------------------------------------------------------------------------------------------------------|
| <> 5       | <> 5       | No voltage select by GPIO for regulator                                                                            |
| <> 5       | 5          | GPIO2 controls regulator selected by <i>reg1_select</i> and <i>reg2_select</i>                                     |
| 5          | <> 5       | GPIO1 controls regulator selected by <i>reg1_select</i> and <i>reg2_select</i>                                     |
| 5          | 5          | GPIO1 controls regulator selected by <i>reg1_select</i><br>GPIO2 controls regulator selected by <i>reg2_select</i> |

**IO Functions:** Shows the 4 different Vselect modes, depending on the setting of *gpioX\_iosf*

### Stand-By and Vselect Input

This mode is very similar to the Vselect mode described in the previous paragraph. In addition to switch between 2 register settings of 2 regulators the chip is set into stand-by mode when the GPIOx pin goes low and wakes up again when the pin is pulled high.

The *gpioX\_mode* should be set to input.

GPIO1 and GPIO2 may be used to control two regulators separately.

**Figure 46:**  
Stand-By and Vselect Modes

| gpio1_iosf | gpio2_iosf | Vselect Mode                                                                                                       | Stand-By Control |
|------------|------------|--------------------------------------------------------------------------------------------------------------------|------------------|
| <> 6       | <> 6       | no voltage select by GPIO for regulator                                                                            | No               |
| <> 6       | 6          | GPIO2 controls regulator selected by <i>reg1_select</i> and <i>reg2_select</i>                                     | Yes              |
| 6          | <> 6       | GPIO1 controls regulator selected by <i>reg1_select</i> and <i>reg2_select</i>                                     | Yes              |
| 6          | 6          | GPIO1 controls regulator selected by <i>reg1_select</i><br>GPIO2 controls regulator selected by <i>reg2_select</i> | Yes              |

**IO Functions:** Shows the 4 different Vselect and Stand-By control modes, depending on the setting of *gpioX\_iosf*

### **PWRGOOD Output**

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators.

The *gpioX\_mode* should be set to output.

### **Supervisor**

All step-down DC/DCs have an integrated over-current protection.

An overtemperature protection of the chip is also integrated which can be switched on with the serial interface signal *temp\_pmc\_on* (enabled by default; it is not recommended to disable the overtemperature protection).

### **Temperature Supervision**

The chip has two signals for the serial interface: *ov\_temp\_110* and *ov\_temp\_140*.

The flag *ov\_temp\_110* is automatically reset if the overtemperature condition is removed, whereas *ov\_temp\_140* has to be reset by the serial interface with the signal *rst\_ov\_temp\_140*. If the flag *ov\_temp\_140* is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T110 level (including hysteresis). The flag *ov\_temp\_140* is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

**Figure 47:**  
**Overtemperature Protection**

| Symbol            | Parameter                              | Min | Typ | Max | Unit |
|-------------------|----------------------------------------|-----|-----|-----|------|
| T <sub>110</sub>  | ov_temp_110 rising threshold           | 95  | 110 | 125 | °C   |
| T <sub>140</sub>  | ov_temp_140 rising threshold           | 125 | 140 | 155 | °C   |
| T <sub>HYST</sub> | ov_temp_110 and ov_temp_140 hysteresis |     | 5   |     | °C   |

## Interrupt Generation

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt 1...2* register are set by pulling low pin XINT (XINT has to be selected as a GPIO output function). All the interrupt sources can be enabled in the Interrupt Mask 1...2 register. The Interrupt 1...2 registers are cleared automatically after the host controller has read them. To prevent the AS3709 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers, the GPIO pin (GPIO output function) will be released. As soon as the transferred bits of the interrupt register have been cleared the GPIO pin (GPIO output function) will be pulled low in case a new interrupt has occurred in the meantime. By doing so, the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the *Interrupt 1* register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling low the GPIO pin) before the Interrupt 2 register has been read.

## 2-Wire-Serial Control Interface

### Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components



**I<sup>2</sup>C Protocol**

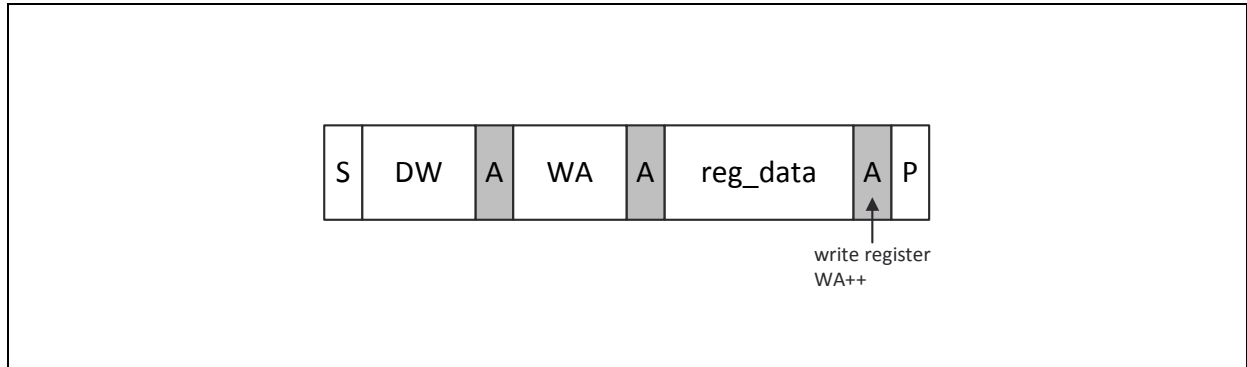
**Figure 48:**  
**2-Wire Serial Symbol Definition**

| Symbol   | Definition                        | RW | Note               |
|----------|-----------------------------------|----|--------------------|
| S        | Start condition after Stop        | R  | 1 bit              |
| Sr       | Repeated Start                    | R  | 1 bit              |
| DW       | Device address for Write          | R  | 1000 0000b (80h)   |
| DR       | Device address for Read           | R  | 1000 0001b (81h)   |
| WA       | Word address                      | R  | 8 bit              |
| A        | Acknowledge                       | W  | 1 bit              |
| N        | No Acknowledge                    | R  | 1 bit              |
| reg_data | Register data/write               | R  | 8 bit              |
| data (n) | Register data/read                | W  | 8 bit              |
| P        | Stop condition                    | R  | 1 bit              |
| WA++     | Increment word address internally | R  | During acknowledge |
|          | AS3709 (= slave) receive data     |    |                    |
|          | AS3709 (= slave) transmits data   |    |                    |

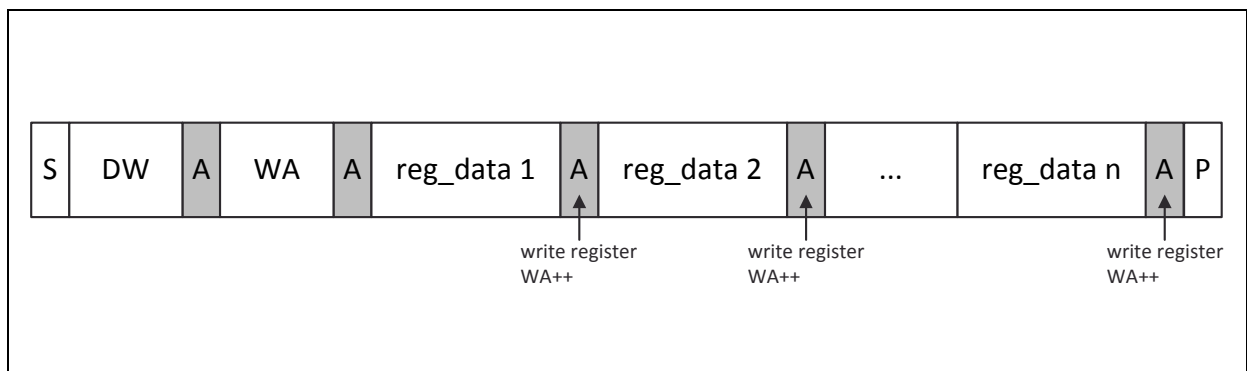
### I<sup>2</sup>C Write Access

Byte Write and Page Write formats are used to write data to the slave.

**Figure 49:**  
I<sup>2</sup>C Byte Write



**Figure 50:**  
I<sup>2</sup>C Page Write



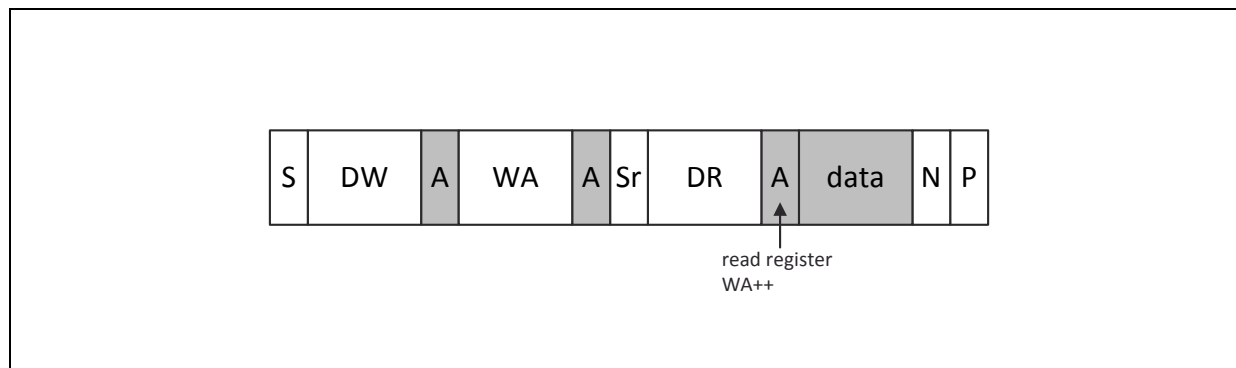
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1<sup>st</sup> register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

### I<sup>2</sup>C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

**Figure 51:**  
I<sup>2</sup>C Random Read

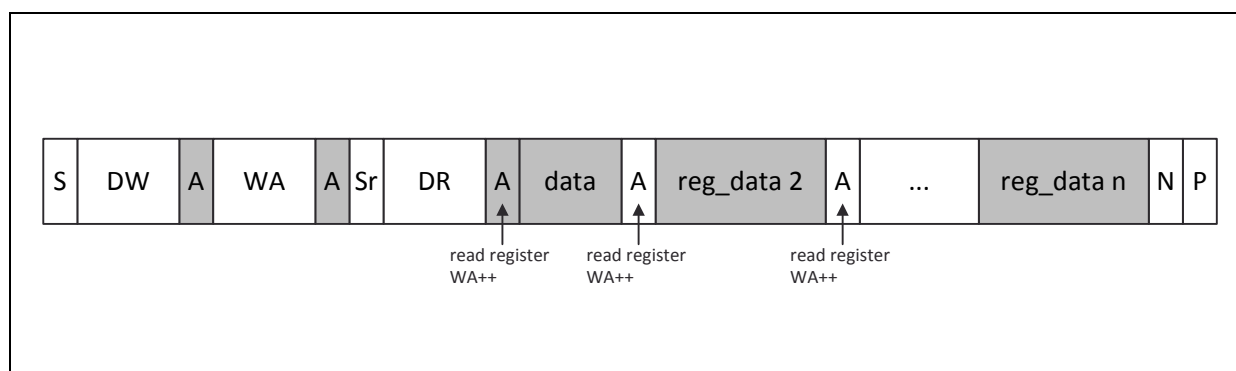


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

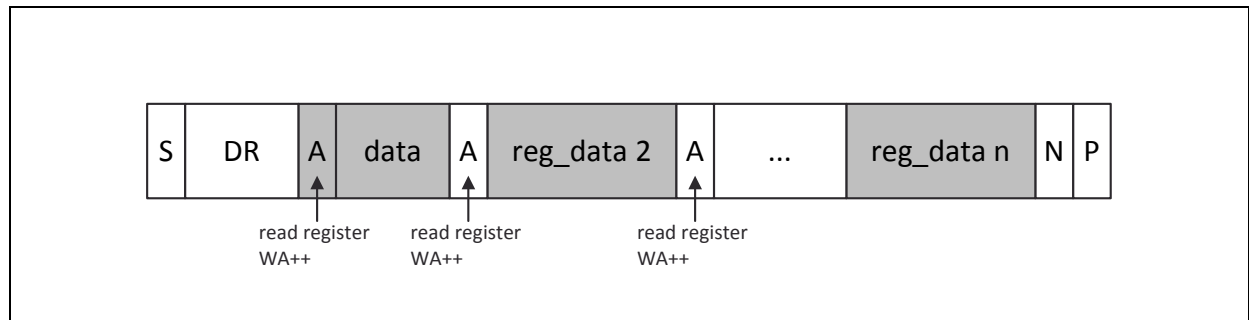
**Figure 52:**  
I<sup>2</sup>C Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master.

The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

**Figure 53:**  
**I<sup>2</sup>C Current Address Read**



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1<sup>st</sup> register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

### I<sup>2</sup>C Parameter

**Figure 54:**  
**I<sup>2</sup>C SDA/SCL Characteristics**

| Symbol          | Parameter                        | Min | Typ | Max | Unit |
|-----------------|----------------------------------|-----|-----|-----|------|
| V <sub>IL</sub> | SCL,SDA Low Level Input Voltage  |     |     | 0.4 | V    |
| V <sub>IH</sub> | SCL,SDA High Level Input Voltage | 1.4 |     |     | V    |

The AS3709 is compatible to the NXP two wire specification [www.nxp.com/documents/user\\_manual/UM10204.pdf](http://www.nxp.com/documents/user_manual/UM10204.pdf) Version 4.0 Feb 2012 for standard mode and fast mode (no fast mode plus or high speed mode support).

## Register Description

**Figure 55:**  
**Register Overview**

| Addr | Name           | <D7>               | <D6>            | <D5>               | <D4>       | <D3>               | <D2>            | <D1>               | <D0>       |
|------|----------------|--------------------|-----------------|--------------------|------------|--------------------|-----------------|--------------------|------------|
| 00h  | SD1Voltage     | sd1_frequ          | sd1_vsel<6:0>   |                    |            |                    |                 |                    |            |
| 01h  | SD2Voltage     | sd2_frequ          | sd2_vsel<6:0>   |                    |            |                    |                 |                    |            |
| 02h  | SD3Voltage     | sd3_frequ          | sd3_vsel<6:0>   |                    |            |                    |                 |                    |            |
| 03h  | SD4Voltage     | sd4_frequ          | sd4_vsel<6:0>   |                    |            |                    |                 |                    |            |
| 04h  | SD5Voltage     | sd5_frequ          | sd5_vsel<6:0>   |                    |            |                    |                 |                    |            |
| 05h  | LDO1Voltage    | ldo1_ilimit        | ldo1_vsel<6:0>  |                    |            |                    |                 |                    |            |
| 06h  | LDO2Voltage    | ldo2_ilimit        | ldo2_vsel<6:0>  |                    |            |                    |                 |                    |            |
| 0ch  | GPIO1control   | gpio1_invert       | gpio1_iosf<6:3> |                    |            |                    | gpio1_mode<2:0> |                    |            |
| 0dh  | GPIO2control   | gpio2_invert       | gpio2_iosf<6:3> |                    |            |                    | gpio2_mode<2:0> |                    |            |
| 10h  | SDcontrol      | -                  | ldo2_enable     | ldo1_enable        | sd5_enable | sd4_enable         | sd3_enable      | sd2_enable         | sd1_enable |
| 20h  | GPIOsignal_out | -                  |                 |                    |            | -                  | -               | gpio2_out          | gpio1_out  |
| 21h  | GPIOsignal_in  | -                  |                 |                    |            | -                  | -               | gpio2_in           | gpio1_in   |
| 22h  | Reg1_Voltage   | reg1_voltage<7:0>  |                 |                    |            |                    |                 |                    |            |
| 23h  | Reg2_Voltage   | reg2_voltage<7:0>  |                 |                    |            |                    |                 |                    |            |
| 24h  | Reg_control    | reg2_select<7:4>   |                 |                    |            | reg1_select<3:0>   |                 |                    |            |
| 25h  | GPIOctrl_sd    | gpio_ctrl_sd4<7:6> |                 | gpio_ctrl_sd3<5:4> |            | gpio_ctrl_sd2<3:2> |                 | gpio_ctrl_sd1<1:0> |            |

| Addr | Name                    | <D7>               | <D6>               | <D5>                | <D4>            | <D3>                | <D2>             | <D1>               | <D0>                 |
|------|-------------------------|--------------------|--------------------|---------------------|-----------------|---------------------|------------------|--------------------|----------------------|
| 26h  | GPIOctrl_Ido            | -                  | -                  | gpio_ctrl_ldo2<5:4> |                 | gpio_ctrl_ldo1<3:2> |                  | gpio_ctrl_sd5<1:0> |                      |
| 29h  | SD_control3             | sd5_slave          | sd4_slave          | sd2_slave           | sd5_fsel        | sd5_fast            | sd5_low_noise    | -                  |                      |
| 30h  | SD_control1             | sd4_low_noise      | sd3_low_noise      | sd2_low_noise       | sd1_low_noise   | sd4_fast            | sd3_fast         | sd2_fast           | sd1_fast             |
| 31h  | SD_control2             | sd_dvm_select<7:6> |                    | dvm_time<5:4>       |                 | sd4_fsel            | sd3_fsel         | sd2_fsel           | sd1_fsel             |
| 32h  | Supply_voltage_monitor  | FastResEn          | SupResEn           | ResVoltFall<5:3>    |                 |                     | ResVoltRise<2:0> |                    |                      |
| 33h  | Startup_control         | -                  |                    |                     |                 |                     |                  | reslevel_5v        | power_off_at_vsuplow |
| 34h  | ResetTimer              | -                  | stby_reset_disable | auto_off            | off_delay<4:3>  |                     | res_timer<2:0>   |                    |                      |
| 35h  | ReferenceControl        | on_reset_delay     | -                  | clk_div2            | standby_mode_on | clk_int<3:1>        |                  |                    | low_power_on         |
| 36h  | ResetControl            | onkey_reset        | reset_reason<6:3>  |                     |                 |                     | on_input         | power_off          | force_reset          |
| 37h  | Overtemperature Control | tco_140_a          | tco_110_a          | temp_test<5:4>      |                 | rst_ov_temp_140     | ov_temp_140      | ov_temp_110        | temp_pmc_on          |
| 39h  | Reg_standby_mod1        | disable_regpd      | ldo2_stby_on       | ldo1_stby_on        | sd5_stby_on     | sd4_stby_on         | sd3_stby_on      | sd2_stby_on        | sd1_stby_on          |
| 73h  | RegStatus               | -                  |                    |                     | sd5_lv          | sd4_lv              | sd3_lv           | sd2_lv             | sd1_lv               |
| 74h  | InterruptMask1          | LowVsup_int_m      | ovtmp_int_m        | onkey_int_m         | sd5_lv_int_m    | sd4_lv_int_m        | sd3_lv_int_m     | sd2_lv_int_m       | sd1_lv_int_m         |
| 75h  | InterruptMask2          | -                  |                    |                     |                 |                     |                  | gpio_restart_int_m | gpio_int_m           |

| Addr | Name             | <D7>           | <D6>           | <D5>           | <D4>         | <D3>             | <D2>                 | <D1>               | <D0>         |
|------|------------------|----------------|----------------|----------------|--------------|------------------|----------------------|--------------------|--------------|
| 77h  | InterruptStatus1 | LowBat_int_i   | ovtmp_int_i    | onkey_int_i    | sd5_lv_int_i | sd4_lv_int_i     | sd3_lv_int_i         | sd2_lv_int_i       | sd1_lv_int_i |
| 78h  | InterruptStatus2 | -              |                |                |              |                  |                      | gpio_restart_int_i | gpio_int_i   |
| 90h  | ASIC_ID1         | asic_id1<7:0>  |                |                |              |                  |                      |                    |              |
| 91h  | ASIC_ID2         | fab_id<7:4>    |                |                |              | revision<3:0>    |                      |                    |              |
| a3h  | Fuse3            | del_time       | i2c_deva_bit1  | sequ_on        | sd5_slave    | sd2_slave        | reslevel_5v          |                    |              |
| a4h  | Fuse4            | auto_off       | res_timer<6:4> |                |              | ResVoltRise<3:1> |                      |                    | sd4_slave    |
| a5h  | Fuse5            | LDO1_gpio1_sel | SD5_gpio1_sel  | on_reset_delay | onkey_reset  | gpio12_in_en     | power_off_at_vsuplow | sd1_5_fsel         | sd1_5_fast   |
| a6h  | Fuse6            | sd3_gpio1_sel  | sd2_gpio1_sel  | sd1_gpio1_sel  | Reg6_delay   | Reg5_delay       | Reg4_delay           | Reg3_delay         | Reg2_delay   |
| a7h  | Fuse7            | Reg2_addr<7:4> |                |                |              | Reg1_addr<3:0>   |                      |                    |              |
| a8h  | Fuse8            | reg1_V<7:0>    |                |                |              |                  |                      |                    |              |
| a9h  | Fuse9            | reg2_V<7:0>    |                |                |              |                  |                      |                    |              |
| aah  | Fuse10           | Reg4_addr<7:4> |                |                |              | Reg3_addr<3:0>   |                      |                    |              |
| abh  | Fuse11           | reg3_V<7:0>    |                |                |              |                  |                      |                    |              |
| ach  | Fuse12           | reg4_V<7:0>    |                |                |              |                  |                      |                    |              |
| adh  | Fuse13           | Reg6_addr<7:4> |                |                |              | Reg5_addr<3:0>   |                      |                    |              |
| aeh  | Fuse14           | reg5_V<7:0>    |                |                |              |                  |                      |                    |              |
| afh  | Fuse15           | reg6_V<7:0>    |                |                |              |                  |                      |                    |              |

## Detailed Register Description

**Figure 56:**  
**SD1Voltage Register (Address 00h)**

| Addr: 00h |           | SD1Voltage |        |                                                                                                                                                                                                                                                                                                 |
|-----------|-----------|------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default    | Access | Bit Description                                                                                                                                                                                                                                                                                 |
| 7         | sd1_frequ | 0          | RW     | Selects between high and low frequency dependent on <i>sd1_fsel</i><br><b>0</b> : 2MHz if sd1_fsel=0, 3MHz if sd1_fsel=1<br><b>1</b> : 3MHz if sd1_fsel=0, 4MHz if sd1_fsel=1                                                                                                                   |
| 6:0       | sd1_vsel  | 'b0000000  | RW     | The voltage select bits set the SD1 output voltage level and power the SD1 converter down.<br><b>00h</b> : SD1 powered down<br><b>01h-40h</b> : $V_{SD1}=0.6V+sd1\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD1}=1.4V+(sd1\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD1}=2.6V+(sd1\_vsel-70h)*50mV$ |

**Figure 57:**  
**SD2Voltage Register (Address 01h)**

| Addr: 01h |           | SD2Voltage |        |                                                                                                                                                                                                                                                                                                 |
|-----------|-----------|------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default    | Access | Bit Description                                                                                                                                                                                                                                                                                 |
| 7         | sd2_frequ | 0          | RW     | Selects between high and low frequency dependent on <i>sd2_fsel</i><br><b>0</b> : 2MHz if sd2_fsel=0, 3MHz if sd2_fsel=1<br><b>1</b> : 3MHz if sd2_fsel=0, 4MHz if sd2_fsel=1                                                                                                                   |
| 6:0       | sd2_vsel  | 'b0000000  | RW     | The voltage select bits set the SD2 output voltage level and power the SD2 converter down.<br><b>00h</b> : SD2 powered down<br><b>01h-40h</b> : $V_{SD2}=0.6V+sd2\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD2}=1.4V+(sd2\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD2}=2.6V+(sd2\_vsel-70h)*50mV$ |



**Figure 58:**  
**SD3Voltage Register (Address 02h)**

| Addr: 02h |           | SD3Voltage    |        |                                                                                                                                                                                                                                                                                                 |
|-----------|-----------|---------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default       | Access | Bit Description                                                                                                                                                                                                                                                                                 |
| 7         | sd3_frequ | 0             | RW     | Selects between high and low frequency dependent on <i>sd3_fsel</i><br><b>0</b> : 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1<br><b>1</b> : 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1                                                                                                                   |
| 6:0       | sd3_vsel  | 'b000<br>0000 | RW     | The voltage select bits set the SD3 output voltage level and power the SD3 converter down.<br><b>00h</b> : SD3 powered down<br><b>01h-40h</b> : $V_{SD3}=0.6V+sd3\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD3}=1.4V+(sd3\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD3}=2.6V+(sd3\_vsel-70h)*50mV$ |

**Figure 59:**  
**SD4Voltage Register (Address 03h)**

| Addr: 03h |           | SD4Voltage    |        |                                                                                                                                                                                                                                                                                                 |
|-----------|-----------|---------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default       | Access | Bit Description                                                                                                                                                                                                                                                                                 |
| 7         | sd4_frequ | 0             | RW     | Selects between high and low frequency dependent on <i>sd4_fsel</i><br><b>0</b> : 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1<br><b>1</b> : 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1                                                                                                                   |
| 6:0       | sd4_vsel  | 'b000<br>0000 | RW     | The voltage select bits set the SD4 output voltage level and power the SD4 converter down.<br><b>00h</b> : SD4 powered down<br><b>01h-40h</b> : $V_{SD4}=0.6V+sd4\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD4}=1.4V+(sd4\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD4}=2.6V+(sd4\_vsel-70h)*50mV$ |

**Figure 60:**  
**SD5Voltage Register (Address 04h)**

| Addr: 04h |           | SD5Voltage |        |                                                                                                                                                                                                                                                                                                 |
|-----------|-----------|------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default    | Access | Bit Description                                                                                                                                                                                                                                                                                 |
| 7         | sd5_frequ | 0          | RW     | Selects between high and low frequency dependent on <i>sd5_fsel</i><br><b>0</b> : 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1<br><b>1</b> : 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1                                                                                                                   |
| 6:0       | sd5_vsel  | 'b000 0000 | RW     | The voltage select bits set the SD5 output voltage level and power the SD5 converter down.<br><b>00h</b> : SD5 powered down<br><b>01h-40h</b> : $V_{SD4}=0.6V+sd4\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD4}=1.4V+(sd4\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD4}=2.6V+(sd4\_vsel-70h)*50mV$ |

**Figure 61:**  
**LDO1Voltage Register (Address 05h)**

| Addr: 05h |             | LDO1Voltage |        |                                                                                                                                                                                                                                                       |
|-----------|-------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name    | Default     | Access | Bit Description                                                                                                                                                                                                                                       |
| 7         | ldo1_ilimit | 0           | RW     | Sets limit of LDO1<br><b>0</b> : 150mA operating range<br><b>1</b> : 300mA operating range                                                                                                                                                            |
| 6:0       | ldo1_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO1 output voltage 0.825V...3.3V, 25mV steps<br><b>00h</b> : LDO1 off<br><b>01h-24h</b> : $V_{LDO1}=0.8V+ldo1\_vsel*25mV$<br><b>25h-3fh</b> : Do not use<br><b>40h-7Fh</b> : $V_{LDO1}=1.725V+(ldo1\_vsel-40h)*25mV$ |

**Figure 62:**  
**LDO2Voltage Register (Address 06h)**

| Addr: 06h |             | LDO2Voltage |        |                                                                                                                                                                                                                                                       |
|-----------|-------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name    | Default     | Access | Bit Description                                                                                                                                                                                                                                       |
| 7         | ldo2_ilimit | 0           | RW     | Sets limit of LDO2<br><b>0</b> : 150mA operating range<br><b>1</b> : 300mA operating range                                                                                                                                                            |
| 8:0       | ldo2_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO2 output voltage 0.825V...3.3V, 25mV steps<br><b>00h</b> : LDO2 off<br><b>01h-24h</b> : $V_{LDO2}=0.8V+ldo2\_vsel*25mV$<br><b>25h-3fh</b> : Do not use<br><b>40h-7Fh</b> : $V_{LDO2}=1.725V+(ldo2\_vsel-40h)*25mV$ |

**Figure 63:**  
**GPIO1control Register (Address 0ch)**

| Addr: 0ch |              | GPIO1control |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------|--------------|--------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name     | Default      | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7         | gpio1_invert | 0            | RW     | Invert GPIO1 input/output<br><b>0</b> : Normal mode<br><b>1</b> : Invert input or output                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6:3       | gpio1_iosf   | 'b0000       | RW     | Select the GPIO1 special function<br><b>0</b> : Normal I/O operation<br><b>1</b> : Interrupt output<br><b>2</b> : VSUP_low output<br><b>3</b> : GPIO interrupt input<br><b>4</b> : NA<br><b>5</b> : Vselect input, (apply on reg1_select and reg2_select, if gpio2_iosf=5 then apply on reg1_select only)<br><b>6</b> : standby + Vselect + restart interrupt input<br><b>7</b> : pwr_good output<br><b>8</b> : NA<br><b>9</b> : NA<br><b>10</b> : NA<br><b>11</b> : NA<br><b>12</b> : NA<br><b>13</b> : NA<br><b>14</b> : NA<br><b>15</b> : NA |
| 2:0       | gpio1_mode   | 'b011        | RW     | Selects the GPIO1 mode (I, I/O, Tri, Pulls)<br><b>0</b> : Input<br><b>1</b> : Output (push and pull)<br><b>2</b> : IO (open drain, only NMOS is active)<br><b>3</b> : NA<br><b>4</b> : Input with pullup<br><b>5</b> : Input with pulldown<br><b>6</b> : IO (open drain (NMOS) with pullup)<br><b>7</b> : NA                                                                                                                                                                                                                                    |

**Figure 64:**  
**GPIO2control Register (Address 0dh)**

| Addr: 0dh |              | GPIO2control |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------|--------------|--------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name     | Default      | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7         | gpio2_invert | 0            | RW     | Invert GPIO2 input/output<br><b>0</b> : Normal mode<br><b>1</b> : Invert input or output                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6:3       | gpio2_iosf   | 'b0000       | RW     | Select the GPIO2 special function<br><b>0</b> : Normal i/o operation<br><b>1</b> : Interrupt output<br><b>2</b> : VSUP_low output<br><b>3</b> : GPIO interrupt input<br><b>4</b> : NA<br><b>5</b> : Vselect input, (apply on reg1_select and reg2_select, if gpio1_iosf=5 then apply on reg2_select only)<br><b>6</b> : standby + Vselect + restart interrupt input<br><b>7</b> : pwr_good output<br><b>8</b> : NA<br><b>9</b> : NA<br><b>10</b> : NA<br><b>11</b> : NA<br><b>12</b> : NA<br><b>13</b> : NA<br><b>14</b> : NA<br><b>15</b> : NA |
| 2:0       | gpio2_mode   | 'b011        | RW     | Selects the GPIO2 mode (I, I/O, Tri, Pulls)<br><b>0</b> : Input<br><b>1</b> : Output (push and pull)<br><b>2</b> : IO (open drain, only NMOS is active)<br><b>3</b> : NA<br><b>4</b> : Input with pullup<br><b>5</b> : Input with pulldown<br><b>6</b> : IO (open drain (NMOS) with pullup)<br><b>7</b> : NA                                                                                                                                                                                                                                    |

**Figure 65:**  
**SDcontrol Register (Address 10h)**

| Addr: 10h |             | SDcontrol |        |                                                                  |
|-----------|-------------|-----------|--------|------------------------------------------------------------------|
| Bit       | Bit Name    | Default   | Access | Bit Description                                                  |
| 7         | -           | 'b0       | N/A    | Do not use                                                       |
| 6         | ldo2_enable | 'b1       | RW     | Global LDO2 enable<br><b>0</b> : LDO2 off<br><b>1</b> : LDO2 on  |
| 5         | ldo1_enable | 'b1       | RW     | Global LDO1 enable<br><b>0</b> : LDO1 off<br><b>1</b> : LDO1 on  |
| 4         | sd5_enable  | 'b1       | RW     | Global stepdown5 enable<br><b>0</b> : SD off<br><b>1</b> : SD on |
| 3         | sd4_enable  | 'b1       | RW     | Global stepdown4 enable<br><b>0</b> : SD off<br><b>1</b> : SD on |
| 2         | sd3_enable  | 'b1       | RW     | Global stepdown3 enable<br><b>0</b> : SD off<br><b>1</b> : SD on |
| 1         | sd2_enable  | 'b1       | RW     | Global stepdown2 enable<br><b>0</b> : SD off<br><b>1</b> : SD on |
| 0         | sd1_enable  | 'b1       | RW     | Global stepdown1 enable<br><b>0</b> : SD off<br><b>1</b> : SD on |

**Figure 66:**  
**GPIOsignal\_out Register (Address 20h)**

| Addr: 20h |           | GPIOsignal_out |        |                                                                                        |
|-----------|-----------|----------------|--------|----------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default        | Access | Bit Description                                                                        |
| 7:2       | -         | 'b0000         | N/A    | Do not use                                                                             |
| 1         | gpio2_out | 0              | RW     | This bit determines the output signal of the GPIO2 pin when selected as output source. |
| 0         | gpio1_out | 0              | RW     | This bit determines the output signal of the GPIO1 pin when selected as output source. |

**Figure 67:**  
GPIOsignal\_in Register (Address 21h)

| Addr: 21h |          | GPIOsignal_in |        |                                                                                          |
|-----------|----------|---------------|--------|------------------------------------------------------------------------------------------|
| Bit       | Bit Name | Default       | Access | Bit Description                                                                          |
| 7:2       | -        | 'b0000        | N/A    | Do not use                                                                               |
| 1         | gpio2_in | 0             | RO     | This bit reflects the logic level of the GPIO2 pin when configured as digital input pin. |
| 0         | gpio1_in | 0             | RO     | This bit reflects the logic level of the GPIO1 pin when configured as digital input pin. |

**Figure 68:**  
Reg1\_Voltage Register (Address 22h)

| Addr: 22h |              | Reg1_Voltage |        |                                                                                                                                                                                                                                                                                |
|-----------|--------------|--------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name     | Default      | Access | Bit Description                                                                                                                                                                                                                                                                |
| 7:0       | reg1_voltage | 'b0000 0000  | RW     | This register is mapped to the register address 0h+Reg1_select, if gioX_iosf = 5 or 6 (Vselect input), and input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input.<br><b>0..FFh</b> : Selects voltage and frequency bits of DC/DC |

**Figure 69:**  
Reg2\_Voltage Register (Address 23h)

| Addr: 23h |              | Reg2_Voltage |        |                                                                                                                                                                                                                                                                             |
|-----------|--------------|--------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name     | Default      | Access | Bit Description                                                                                                                                                                                                                                                             |
| 7:0       | reg2_voltage | 'b0000 0000  | RW     | This register is mapped to the register address 0h+Reg1_select, if gioX_iosf=5 or 6 (Vselect input), and input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input<br><b>0..FFh</b> : Selects voltage and frequency bits of DC/DC |

**Figure 70:**  
**Reg\_control Register (Address 24h)**

| Addr: 24h |             | Reg_control |        |                                                                                        |
|-----------|-------------|-------------|--------|----------------------------------------------------------------------------------------|
| Bit       | Bit Name    | Default     | Access | Bit Description                                                                        |
| 7:4       | reg2_select | 'b1111      | RW     | Selects regulator for mapping feature; if reg_select2 ≥ 0Ch, then feature is disabled. |
| 3:0       | reg1_select | 'b1111      | RW     | Selects regulator for mapping feature; if reg_select1 ≥ 0Ch, then feature is disabled. |

**Figure 71:**  
**GPIOctrl\_sd Register (Address 25h)**

| Addr: 25h |               | GPIOctrl_sd |        |                                                                                                                                                                                                 |
|-----------|---------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default     | Access | Bit Description                                                                                                                                                                                 |
| 7:6       | gpio_ctrl_sd4 | 'b00        | RW     | Enable GPIO control of DC/DC SD4. GPIO ctrl only enabled,<br>if sd4_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |
| 5:4       | gpio_ctrl_sd3 | 'b00        | RW     | Enable GPIO control of DC/DC SD3. GPIO ctrl only enabled,<br>if sd3_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |
| 3:2       | gpio_ctrl_sd2 | 'b00        | RW     | Enable GPIO control of DC/DC SD2. GPIO ctrl only enabled,<br>if sd2_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |
| 1:0       | gpio_ctrl_sd1 | 'b00        | RW     | Enable GPIO control of DC/DC SD1. GPIO ctrl only enabled,<br>if sd1_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |

**Figure 72:**  
GPIOctrl\_Ido Register (Address 26h)

| Addr: 26h |                | GPIOctrl_Ido |        |                                                                                                                                                                                          |
|-----------|----------------|--------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name       | Default      | Access | Bit Description                                                                                                                                                                          |
| 7:6       | -              | 'b00         | N/A    | -                                                                                                                                                                                        |
| 5:4       | gpio_ctrl_ldo2 | 'b00         | RW     | Enable GPIO control of LDO2. GPIO ctrl only enabled, if ldo2_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |
| 3:2       | gpio_ctrl_ldo1 | 'b00         | RW     | Enable GPIO control of LDO1. GPIO ctrl only enabled, if ldo1_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA |
| 1:0       | gpio_ctrl_sd5  | 'b00         | RW     | Enable GPIO control of SD5. GPIO ctrl only enabled, if sd5_vsel > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : NA   |



**Figure 73:**  
**SD\_control3 Register (Address 29h)**

| Addr: 29h |               | SD_control3 |        |                                                                                                                                                                                                                                                                   |
|-----------|---------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default     | Access | Bit Description                                                                                                                                                                                                                                                   |
| 7         | sd5_slave     | 0           | RW     | Enables slave mode of SD5<br><b>0</b> : Normal mode of SD5<br><b>1</b> : SD5 is slave of SD3                                                                                                                                                                      |
| 7         | sd4_slave     | 0           | RW     | Enables slave mode of SD4<br><b>0</b> : Normal mode of SD4<br><b>1</b> : SD4 is slave of SD3                                                                                                                                                                      |
| 5         | sd2_slave     | 0           | RW     | Enables slave mode of SD2<br><b>0</b> : Normal mode of SD2<br><b>1</b> : SD2 is slave of SD1                                                                                                                                                                      |
| 4         | sd5_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by sd5_freque)<br><b>1</b> : 3 or 4MHz frequency (selectable by sd5_freque)                                                                                            |
| 3         | sd5_fast      | 0           | RW     | Selects a faster regulation mode for SD5 suitable for larger load changes.<br><b>0</b> : Normal mode, Cext=10μF<br><b>1</b> : Fast mode, Cext=22μF required                                                                                                       |
| 2         | sd5_low_noise | 0           | RW     | Enables low noise mode of SD5. If enabled smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode.<br>Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode.<br>Only minimum on time applied in skip mode. |
| 1:0       | -             | 'b00        | N/A    | -                                                                                                                                                                                                                                                                 |

**Figure 74:**  
**SD\_control1 Register (Address 30h)**

| Addr: 30h |               | SD_control1 |        |                                                                                                                                                                                                                                                                   |
|-----------|---------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default     | Access | Bit Description                                                                                                                                                                                                                                                   |
| 7         | sd4_low_noise | 0           | RW     | Enables low noise mode of SD4. If enabled smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode.<br>Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode.<br>Only minimum on time applied in skip mode. |
| 6         | sd3_low_noise | 0           | RW     | Enables low noise mode of SD3. If enabled smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode.<br>Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode.<br>Only minimum on time applied in skip mode. |
| 5         | sd2_low_noise | 0           | RW     | Enables low noise mode of SD2. If enabled smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode.<br>Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode.<br>Only minimum on time applied in skip mode. |
| 4         | sd1_low_noise | 0           | RW     | Enables low noise mode of SD1. If enabled smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode.<br>Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode.<br>Only minimum on time applied in skip mode. |
| 3         | sd4_fast      | 0           | RW     | Selects a faster regulation mode for SD4 suitable for larger load changes.<br><b>0</b> : Normal mode, Cext=10μF<br><b>1</b> : Fast mode, Cext=22μF required                                                                                                       |
| 2         | sd3_fast      | 0           | RW     | Selects a faster regulation mode for SD3 suitable for larger load changes.<br><b>0</b> : Normal mode, Cext=10μF<br><b>1</b> : Fast mode, Cext=22μF required                                                                                                       |
| 1         | sd2_fast      | 0           | RW     | Selects a faster regulation mode for SD2 suitable for larger load changes.<br><b>0</b> : Normal mode, Cext=10μF<br><b>1</b> : Fast mode, Cext=22μF required                                                                                                       |
| 0         | sd1_fast      | 0           | RW     | Selects a faster regulation mode for SD1 suitable for larger load changes.<br><b>0</b> : Normal mode, Cext=10μF<br><b>1</b> : Fast mode, Cext=22μF required                                                                                                       |

**Figure 75:**  
**SD\_control2 Register (Address 31h)**

| Addr: 31h |               | SD_control2 |        |                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------|---------------|-------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default     | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                      |
| 7:6       | sd_dvm_select | 'b00        | RW     | Apply DVM counter to the following DC/DC converter<br><b>0</b> : Select SD1 for DVM<br><b>1</b> : Select SD2 for DVM<br><b>2</b> : Select SD3 for DVM<br><b>3</b> : Select SD5 for DVM                                                                                                                                                                                               |
| 5:4       | dvm_time      | 'b00        | RW     | Time steps of DVM voltage change of selected step down, if voltage of step Down is changed during operation (sd_x_vsel) voltage is decreased/increased by single steps 12.5mV<br><b>0</b> : 0 $\mu$ s, immediate change (no DVM)<br><b>1</b> : 4 $\mu$ s time delay between steps<br><b>2</b> : 8 $\mu$ s time delay between steps<br><b>3</b> : 16 $\mu$ s time delay between steps |
| 3         | sd4_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by sd4_frequ)<br><b>1</b> : 3 or 4MHz frequency (selectable by sd4_frequ)                                                                                                                                                                                                                 |
| 2         | sd3_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by sd3_frequ)<br><b>1</b> : 3 or 4MHz frequency (selectable by sd3_frequ)                                                                                                                                                                                                                 |
| 1         | sd2_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by sd2_frequ)<br><b>1</b> : 3 or 4MHz frequency (selectable by sd2_frequ)                                                                                                                                                                                                                 |
| 0         | sd1_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by sd1_frequ)<br><b>1</b> : 3 or 4MHz frequency (selectable by sd1_frequ)                                                                                                                                                                                                                 |

**Figure 76:**  
**Supply\_voltage\_monitor Register (Address 32h)**

| Addr: 32h |             | Supply_voltage_monitor |          |                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------|-------------|------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name    | Default                | Access   | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7         | FastResEn   | 0                      | RW       | <b>0</b> : ResVoltFall debounce time = 3ms<br><b>1</b> : ResVoltFall debounce time = 4μs (tbd)                                                                                                                                                                                                                                                                                                                            |
| 6         | SupResEn    | 0                      | RW       | <b>0</b> : A reset is generated if V <sub>SUP</sub> falls below 2.7V <sup>(1)</sup><br><b>1</b> : A reset is generated if V <sub>SUP</sub> falls below ResVoltFall                                                                                                                                                                                                                                                        |
| 5:3       | ResVoltFall | 'b000                  | RW       | This value determines the reset level ResVoltFall for falling V <sub>SUP</sub> . It is recommended to set this value at least 200mV lower than ResVoltRise (the levels differ between 3.3V and 5V supply)<br><b>0</b> : 2.7V / 3.6V<br><b>1</b> : 2.8V / 3.7V<br><b>2</b> : 2.9V / 3.8V<br><b>3</b> : 3.0V / 3.9V<br><b>4</b> : 3.1V / 4.0V<br><b>5</b> : 3.2V / 4.1V<br><b>6</b> : 3.3V / 4.2V<br><b>7</b> : 3.4V / 4.4V |
| 2:0       | ResVoltRise | 'b000                  | RO (OTP) | This value determines the reset level ResVoltRise for rising V <sub>SUP</sub> . It is recommended to set this value at least 200mV higher than ResVoltFall (the levels differ between 3.3V and 5V supply)<br><b>0</b> : 2.7V / 3.6V<br><b>1</b> : 2.8V / 3.7V<br><b>2</b> : 2.9V / 3.8V<br><b>3</b> : 3.0V / 3.9V<br><b>4</b> : 3.1V / 4.0V<br><b>5</b> : 3.2V / 4.1V<br><b>6</b> : 3.3V / 4.2V<br><b>7</b> : 3.4V / 4.4V |

**Note(s):**

1. If V<sub>SUP</sub> falls below ResVoltFall only an interrupt is generated (if enabled) and the μProcessor can shut down the system.

**Figure 77:**  
**Startup\_Control Register (Address 33h)**

| Addr: 33h |                          | Startup_Control |        |                                                                                                                                                                                                                                                                                                                                    |
|-----------|--------------------------|-----------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name                 | Default         | Access | Bit Description                                                                                                                                                                                                                                                                                                                    |
| 7:2       | -                        | 'b000<br>0000   | N/A    | Do not use                                                                                                                                                                                                                                                                                                                         |
| 1         | reslevel_5v              | 0               | RW     | Selects the 5V supply reset level (see ResVoltRise and ResVoltFall)<br><b>0</b> : 3.3V level<br><b>1</b> : 5.0V level                                                                                                                                                                                                              |
| 0         | power_off_<br>at_vsuplow | 0               | RW     | Switch on Power off mode if low $V_{SUP}$ is detected during active or standby mode (Pin ON= low and bit auto_off=0)<br><b>0</b> : If low $V_{SUP}$ is detected, $V_{SUP}$ is continuously monitored and chip startup initiated if $V_{SUP}$ is above ResVoltRise<br><b>1</b> : If low $V_{SUP}$ is detected, enter power off mode |

**Figure 78:**  
**ResetTimer Register (Address 34h)**

| Addr: 34h |                    | ResetTimer |        |                                                                                                                                                                                                                                                                                             |
|-----------|--------------------|------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name           | Default    | Access | Bit Description                                                                                                                                                                                                                                                                             |
| 7         | -                  | 'b0        | N/A    | Do not use                                                                                                                                                                                                                                                                                  |
| 6         | stby_reset_disable | 0          | RW     | Disable Reset output signal (pin XRES) in standby mode.<br><b>0</b> : Normal mode, reset is active in standby mode<br><b>1</b> : No reset in standby mode and during exit of stand-by mode                                                                                                  |
| 5         | auto_off           | 0          | RO     | Defines startup behavior at first V <sub>SUP</sub> connection<br><b>0</b> : Startup of chip if V <sub>SUP</sub> >ResVltRise<br><b>1</b> : Enter power off mode (Startup with ON key)                                                                                                        |
| 4:3       | off_delay          | 'b01       | RW     | Set delay between I <sup>2</sup> C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command.<br><b>0</b> : No delay<br><b>1</b> : 8 ms<br><b>2</b> : 16 ms<br><b>3</b> : 32 ms                                                                      |
| 2:0       | res_timer          | 'b000      | RW     | Set Reset Time, after the last regulator has started<br><b>0</b> : RESTIME = 2ms<br><b>1</b> : RESTIME = 4ms<br><b>2</b> : RESTIME = 8ms<br><b>3</b> : RESTIME = 16ms<br><b>4</b> : RESTIME = 32ms<br><b>5</b> : RESTIME = 64ms<br><b>6</b> : RESTIME = 128ms<br><b>7</b> : RESTIME = 160ms |

**Figure 79:**  
**ReferenceControl Register (Address 35h)**

| Addr: 35h |                 | ReferenceControl |        |                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------|-----------------|------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name        | Default          | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                   |
| 7         | on_reset_delay  | 0                | RW     | Sets the on reset delay time<br><b>0</b> : 8 s (if onkey_reset=1)<br><b>1</b> : 4 s (if onkey_reset=1)                                                                                                                                                                                                                                                                            |
| 6         | -               | 0                | RW     | -                                                                                                                                                                                                                                                                                                                                                                                 |
| 5         | clk_div2        | 0                | RW     | Divide internal clock oscillator by 2 to reduce quiescent current for low power operation<br><b>0</b> : Normal mode<br><b>1</b> : Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DC/DC converters are divided by two. Reduced transient performance of DC/DC converters.                                                   |
| 4         | standby_mode_on | 0                | RW     | Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by register Reg standby mode. XRES will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously on. |
| 3:1       | clk_int         | 'b000            | RW     | Sets the internal CLK frequency $f_{CLK}$ used for fuel gauge, DC/DCs, PWM, ...<br><b>0</b> : 4 MHz (default)<br><b>1</b> : 3.8 MHz<br><b>2</b> : 3.6 MHz<br><b>3</b> : 3.4 MHz<br><b>4</b> : 3.2 MHz<br><b>5</b> : 3.0 MHz<br><b>6</b> : 2.8 MHz<br><b>7</b> : 2.6 MHz<br>All frequencies, timings and delays in this datasheet are based on 4MHz clk_int                        |
| 0         | low_power_on    | 0                | RW     | Enable low power mode of internal reference.<br><b>0</b> : Standard mode<br><b>1</b> : Low power mode - all specification except noise parameters are still valid. Iq reduced by approx. 30µA                                                                                                                                                                                     |

**Figure 80:**  
**ResetControl Register (Address 36h)**

| Addr: 36h |              | ResetControl |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------|--------------|--------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name     | Default      | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7         | onkey_reset  | 0            | RW     | <b>0</b> : Reset after 4/8 seconds ON pressed disabled<br><b>1</b> : Reset after 4/8 seconds ON pressed enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6:3       | reset_reason | 'b0000       | RW     | Flags to indicate to the software the reason for the last reset<br><b>0</b> : V <sub>POR</sub> has been reached (V <sub>SUP</sub> connection from scratch)<br><b>1</b> : ResVoltFall was reached (V <sub>SUP</sub> drop below 2.75V)<br><b>2</b> : Software forced by force_reset<br><b>3</b> : Software forced by power_off and ON was pulled high<br><b>4</b> : Software forced by power_off and charger was detected<br><b>5</b> : External triggered through the pin XRES<br><b>6</b> : Reset caused by overtemperature T140<br><b>7</b> : NA<br><b>8</b> : Reset caused by 4/8 seconds ON press<br><b>9</b> : NA<br><b>10</b> : NA<br><b>11</b> : Reset caused by interrupt in standby mode<br><b>12</b> : Reset caused by ON pulled high in standby mode |
| 2         | on_input     | 0            | R_PUSH | <b>Read:</b> This flag represents the state of the ON pad directly<br><b>Write:</b> Setting to 1 resets the 4/8 seconds. onkey_reset timer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1         | power_off    | 0            | RW     | Setting to 1 starts a reset cycle, but waits after the Reg_off state for a falling edge on the pin ON                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 0         | force_reset  | 0            | RW     | Setting to 1 starts a complete reset cycle                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |



**Figure 81:**  
**OvertemperatureControl Register (Address 37h)**

| Addr: 37h |                 | OvertemperatureControl |        |                                                                                                                                                                                             |
|-----------|-----------------|------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name        | Default                | Access | Bit Description                                                                                                                                                                             |
| 7         | tco_140_a       | b0                     | RO     | Only used for production test                                                                                                                                                               |
| 6         | tco_110_a       | b0                     | RO     | Only used for production test                                                                                                                                                               |
| 5:4       | temp_test       | b00                    | RW     |                                                                                                                                                                                             |
| 3         | rst_ov_temp_140 | 0                      | RWP    | If the overtemperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterward 0 to rst_ov_temp_140. |
| 2         | ov_temp_140     | 0                      | RO     | Flag that the overtemperature threshold 2 (T140) has been reached - this flag is not reset by an overtemperature caused reset and has to be reset by rst_ov_temp_140.                       |
| 1         | ov_temp_110     | 0                      | RO     | Flag that the overtemperature threshold 1 (T110) has been reached                                                                                                                           |
| 0         | temp_pmc_on     | 1                      | RO     | Switch on / off the temperature supervision; default: on - all other bits are only valid if set to 1 leave at 1, do not disable                                                             |

**Figure 82:**  
**Reg\_standby\_mod1 Register (Address 39h)**

| Addr: 39h |               | Reg_standby_mod1 |        |                                                                                                                                                                                 |
|-----------|---------------|------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default          | Access | Bit Description                                                                                                                                                                 |
| 7         | disable_regpd | 0                | RW     | This bit disables the pulldown of all regulators<br><b>0</b> : Normal operation approx. 1kΩ pulldown of all regulators<br><b>1</b> : Pulldown disabled >100kΩ of all regulators |
| 6         | ldo2_stby_on  | 0                | RW     | Enable LDO2 in standby mode                                                                                                                                                     |
| 5         | ldo1_stby_on  | 0                | RW     | Enable LDO1 in standby mode                                                                                                                                                     |
| 4         | sd5_stby_on   | 0                | RW     | Enable Step down 4 in standby mode                                                                                                                                              |
| 3         | sd4_stby_on   | 0                | RW     | Enable Step down 4 in standby mode                                                                                                                                              |
| 2         | sd3_stby_on   | 0                | RW     | Enable Step down 3 in standby mode                                                                                                                                              |
| 1         | sd2_stby_on   | 0                | RW     | Enable Step down 2 in standby mode                                                                                                                                              |
| 0         | sd1_stby_on   | 0                | RW     | Enable Step down 1 in standby mode                                                                                                                                              |

**Figure 83:**  
**RegStatus Register (Address 73h)**

| Addr: 73h |          | RegStatus |        |                                                                                                    |
|-----------|----------|-----------|--------|----------------------------------------------------------------------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                                                                                    |
| 7:5       | -        | 'b000     | N/A    | Do not use                                                                                         |
| 4         | sd5_lv   | 0         | RO     | Bit is set when voltage of SD5 drops below low voltage threshold (-5%) (1ms debounce time default) |
| 3         | sd4_lv   | 0         | RO     | Bit is set when voltage of SD4 drops below low voltage threshold (-5%) (1ms debounce time default) |
| 2         | sd3_lv   | 0         | RO     | Bit is set when voltage of SD3 drops below low voltage threshold (-5%) (1ms debounce time default) |
| 1         | sd2_lv   | 0         | RO     | Bit is set when voltage of SD2 drops below low voltage threshold (-5%) (1ms debounce time default) |
| 0         | sd1_lv   | 0         | RO     | Bit is set when voltage of SD1 drops below low voltage threshold (-5%) (1ms debounce time default) |

**Figure 84:**  
**InterruptMask1 Register (Address 74h)**

| Addr: 74h |               | InterruptMask1 |        |                                  |
|-----------|---------------|----------------|--------|----------------------------------|
| Bit       | Bit Name      | Default        | Access | Bit Description                  |
| 7         | LowVsup_int_m | 1              | RW     | Set to 0 to enable the interrupt |
| 6         | ovtmp_int_m   | 1              | RW     | Set to 0 to enable the interrupt |
| 5         | onkey_int_m   | 1              | RW     | Set to 0 to enable the interrupt |
| 4         | sd5_lv_int_m  | 1              | RW     | Set to 0 to enable the interrupt |
| 3         | sd4_lv_int_m  | 1              | RW     | Set to 0 to enable the interrupt |
| 2         | sd3_lv_int_m  | 1              | RW     | Set to 0 to enable the interrupt |
| 1         | sd2_lv_int_m  | 1              | RW     | Set to 0 to enable the interrupt |
| 0         | sd1_lv_int_m  | 1              | RW     | Set to 0 to enable the interrupt |

**Figure 85:**  
**InterruptMask2 Register (Address 75h)**

| Addr: 75h |          | InterruptMask2 |        |                 |
|-----------|----------|----------------|--------|-----------------|
| Bit       | Bit Name | Default        | Access | Bit Description |
| 7:2       | -        | 'b0000 00      | N/A    | Do not use      |

| Addr: 75h |                    | InterruptMask2 |        |                                  |
|-----------|--------------------|----------------|--------|----------------------------------|
| Bit       | Bit Name           | Default        | Access | Bit Description                  |
| 1         | gpio_restart_int_m | 1              | RW     | Set to 0 to enable the interrupt |
| 0         | gpio_int_m         | 1              | RW     | Set to 0 to enable the interrupt |

**Figure 86:**  
**InterruptStatus1 Register (Address 77h)**

| Addr: 77h |              | InterruptStatus1 |        |                                                                  |
|-----------|--------------|------------------|--------|------------------------------------------------------------------|
| Bit       | Bit Name     | Default          | Access | Bit Description                                                  |
| 7         | LowBat_int_i | 0                | POP    | Bit is set when $V_{SUP}$ drops below vres_fall rising edge only |
| 6         | ovtmp_int_i  | 0                | POP    | Bit is set when 110deg is exceeded rising edge only              |
| 5         | onkey_int_i  | 0                | POP    | Rising and falling edge                                          |
| 4         | sd5_lv_int_i | 0                | POP    | Rising edge only                                                 |
| 3         | sd4_lv_int_i | 0                | POP    | Rising edge only                                                 |
| 2         | sd3_lv_int_i | 0                | POP    | Rising edge only                                                 |
| 1         | sd2_lv_int_i | 0                | POP    | Rising edge only                                                 |
| 0         | sd1_lv_int_i | 0                | POP    | Rising edge only                                                 |

**Figure 87:**  
**InterruptStatus2 Register (Address 78h)**

| Addr: 78h |                    | InterruptStatus2 |        |                         |
|-----------|--------------------|------------------|--------|-------------------------|
| Bit       | Bit Name           | Default          | Access | Bit Description         |
| 7:2       | -                  | 'b0000 00        | N/A    | Do not use              |
| 1         | gpio_restart_int_i | 0                | POP    | Falling edge            |
| 0         | gpio_int_i         | 0                | POP    | Rising and falling edge |

**Figure 88:**  
**ASIC\_ID1 Register (Address 90h)**

| Addr: 90h |          | ASIC_ID1   |        |                 |
|-----------|----------|------------|--------|-----------------|
| Bit       | Bit Name | Default    | Access | Bit Description |
| 7:0       | asic_id1 | 'b10001110 | RO     | -               |

**Figure 89:**  
**ASIC\_ID2 Register (Address 91h)**

| Addr: 91h |          | ASIC_ID2 |        |                 |
|-----------|----------|----------|--------|-----------------|
| Bit       | Bit Name | Default  | Access | Bit Description |
| 7:4       | fab_id   | 'b0000   | RO     | -               |
| 3:0       | revision | 'b0010   | RO     | Metal fuse!!!   |

**Figure 90:**  
**Fuse 3 Register (Address a3h)**

| Addr: a3h |               | Fuse3   |        |                                                                                                                   |
|-----------|---------------|---------|--------|-------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default | Access | Bit Description                                                                                                   |
| 7         | del_time      | b0      | RW     | Selects delay time before the regulator startup<br>0 : Delay time 1ms if enabled<br>1 : Delay time 4ms if enabled |
| 6         | i2c_deva_bit1 | b0      | RW     | Selects I <sup>2</sup> C address<br>0 : I <sup>2</sup> C address = 80h<br>1 : I <sup>2</sup> C address = 82h      |
| 5         | sequ_on       | b0      | RW     | Startup sequence enabled if set                                                                                   |
| 4         | sd5_slave     | b0      | RW     | Enables slave mode of SD5<br>0 : Normal mode of SD5<br>1 : SD5 is slave of SD3                                    |
| 3         | sd2_slave     | b0      | RW     | Enables slave mode of SD2<br>0 : Normal mode of SD2<br>1 : SD2 is slave of SD1                                    |
| 2         | reslevel_5v   | b0      | RW     | Selects the 5V supply reset level (see ResVoltRise and ResVoltFall)<br>0 : 3.3V level<br>1 : 5.0V level           |

**Figure 91:**  
**Fuse 4 Register (Address a4h)**

| Addr: a4h |             | Fuse4   |        |                                                                                                                                                                                                                                                                                                                                                     |
|-----------|-------------|---------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name    | Default | Access | Bit Description                                                                                                                                                                                                                                                                                                                                     |
| 7         | auto_off    | b0      | RW     | Defines startup behavior at first VSUP connection<br>0 : Startup of chip if VSUP>ResVoltRise<br>1 : Enter power off mode (Startup with ON key)                                                                                                                                                                                                      |
| 6:4       | res_timer   | b000    | RW     | Set Rest Time, after the last regulator has started<br>0 : RESTIME = 2ms<br>1 : RESTIME = 4ms<br>2 : RESTIME = 8ms<br>3 : RESTIME = 16ms<br>4 : RESTIME = 32ms<br>5 : RESTIME = 64ms<br>6 : RESTIME = 128ms<br>7 : RESTIME = 160ms                                                                                                                  |
| 3:1       | ResVoltRise | b000    | RW     | This value determines the reset level ResVoltRise for rising VSUP. It is recommended to set this value at least 200mV higher than ResVoltFall (the level differ between 3.3V and 5V supply)<br>0 : 2.7V / 3.6V<br>1 : 2.8V / 3.7V<br>2 : 2.8V / 3.8V<br>3 : 3.0V / 3.9V<br>4 : 3.1V / 4.0V<br>5 : 3.2V / 4.1V<br>6 : 3.3V / 4.2V<br>7 : 3.4V / 4.4V |
| 0         | sd4_slave   | b0      | RW     | Enables slave mode of SD4<br>0 : Normal mode of SD4<br>1 : SD4 is slave of SD3                                                                                                                                                                                                                                                                      |

**Figure 92:**  
**Fuse 5 Register (Address a5h)**

| Addr: a5h |                      | Fuse5   |        |                                                                                                                                                                                                                                                                                         |
|-----------|----------------------|---------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name             | Default | Access | Bit Description                                                                                                                                                                                                                                                                         |
| 7         | LDO1_gpio1_sel       | b0      | RW     | Enable GPIO1 control of LDO1<br>0 : No GPIO control<br>1 : Controlled by GPIO1                                                                                                                                                                                                          |
| 6         | SD5_gpio1_sel        | b0      | RW     | Enable GPIO1 control of SD5<br>0 : No GPIO control<br>1 : Controlled by GPIO1                                                                                                                                                                                                           |
| 5         | on_reset_delay       | b0      | RW     | Sets the on reset delay time<br>0 : 8 s (if onkey_reset = 1)<br>1 : 4 s (if onkey_reset = 1)                                                                                                                                                                                            |
| 4         | onkey_reset          | b0      | RW     | 0 : Reset after 4/8 seconds ON pressed disabled<br>1 : Reset after 4/8 seconds ON pressed enabled                                                                                                                                                                                       |
| 3         | gpio12_in_en         | b0      | RW     | Enables input_pulldown for gpio1,gpio2 if this bit is set<br>0 : gpio1_mode and gpio2_mode are default (b011)<br>1 : gpio1_mode and gpio2_mode set to (b101) input with pulldown                                                                                                        |
| 2         | power_off_at_vsuplow | b0      | RW     | Switch on Power off mode if low VSUP is detected during active or stand-by mode (ON = low and auto_off = 0)<br>0 : If low VSUP is detected, VSUP is continuously monitored and chip startup initiated if VSUP is above ResVoltRise<br>1 : If low VSUP is detected, enter power off mode |
| 1         | sd1_5_fsel           | b0      | RW     | Selects between high and low frequency range<br>0 : 2 or 3MHz frequency (selectable by sd1..sd5_frequ)<br>1 : 3 or 4MHz frequency (selectable by sd1..sd5_frequ)                                                                                                                        |
| 0         | sd1_5_fast           | b0      | RW     | Selects a faster regulation mode for SD1...SD5 suitable for larger load changes<br>0 : Normal mode, Cout (according spec)<br>1 : Fast mode, 2 x Cout (according spec)                                                                                                                   |

**Figure 93:**  
**Fuse6 Register (Address a6h)**

| Addr: a6h |               | Fuse6   |        |                                                                               |
|-----------|---------------|---------|--------|-------------------------------------------------------------------------------|
| Bit       | Bit Name      | Default | Access | Bit Description                                                               |
| 7         | sd3_gpio1_sel | b0      | RW     | Enable GPIO1 control of SD3<br>0 : No GPIO control<br>1 : Controlled by GPIO1 |
| 6         | sd2_gpio1_sel | b0      | RW     | Enable GPIO1 control of SD2<br>0 : No GPIO control<br>1 : Controlled by GPIO1 |
| 5         | sd1_gpio1_sel | b0      | RW     | Enable GPIO1 control of SD1<br>0 : No GPIO control<br>1 : Controlled by GPIO1 |
| 4         | Reg6_delay    | b0      | RW     | 0 : No delay before the startup<br>1 : 1 / 4 ms delay before the startup      |
| 3         | Reg5_delay    | b0      | RW     | 0 : No delay before the startup<br>1 : 1 / 4 ms delay before the startup      |
| 2         | Reg4_delay    | b0      | RW     | 0 : No delay before the startup<br>1 : 1 / 4 ms delay before the startup      |
| 1         | Reg3_delay    | b0      | RW     | 0 : No delay before the startup<br>1 : 1 / 4 ms delay before the startup      |
| 0         | Reg2_delay    | b0      | RW     | 0 : No delay before the startup<br>1 : 1 / 4 ms delay before the startup      |

**Figure 94:**  
**Fuse7 Register (Address a7h)**

| Addr: a7h |           | Fuse7   |        |                                                                                                                                                                                                 |
|-----------|-----------|---------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default | Access | Bit Description                                                                                                                                                                                 |
| 7:4       | Reg2_addr | b0000   | RW     | Define startup regulator 2<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |
| 3:0       | Reg1_addr | b0000   | RW     | Define startup regulator 1<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |

**Figure 95:**  
**Fuse 8 Register (Address a8h)**

| Addr: a8h |          | Fuse8     |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg1_V   | b00000000 | RW     | Define startup voltage for regulator 1 |

**Figure 96:**  
**Fuse 9 Register (Address a9h)**

| Addr: a9h |          | Fuse9     |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg2_V   | b00000000 | RW     | Define startup voltage for regulator 2 |



**Figure 97:**  
**Fuse 10 Register (Address aah)**

| Addr: aah |           | Fuse10  |        |                                                                                                                                                                                                 |
|-----------|-----------|---------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default | Access | Bit Description                                                                                                                                                                                 |
| 7:4       | Reg4_addr | b0000   | RW     | Define startup regulator 4<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |
| 3:0       | Reg3_addr | b0000   | RW     | Define startup regulator 3<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |

**Figure 98:**  
**Fuse 11 Register (Address abh)**

| Addr: abh |          | Fuse11    |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg3_V   | b00000000 | RW     | Define startup voltage for regulator 3 |

**Figure 99:**  
**Fuse 12 Register (Address a8h)**

| Addr: ach |          | Fuse12    |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg4_V   | b00000000 | RW     | Define startup voltage for regulator 4 |

**Figure 100:**  
**Fuse 13 Register (Address adh)**

| Addr: adh |           | Fuse13  |        |                                                                                                                                                                                                 |
|-----------|-----------|---------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit       | Bit Name  | Default | Access | Bit Description                                                                                                                                                                                 |
| 7:4       | Reg6_addr | b0000   | RW     | Define startup regulator 6<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |
| 3:0       | Reg5_addr | b0000   | RW     | Define startup regulator 5<br>0 : SD1 (0h)<br>1 : SD2 (1h)<br>2 : SD3 (2h)<br>3 : SD4 (3h)<br>4 : SD5 (4h)<br>5 : LDO1 (5h)<br>6 : LDO2 (6h)<br>7 : GPIO1 (ch)<br>8 : GPIO2 (dh)<br>9 : NA (fh) |

**Figure 101:**  
**Fuse 14 Register (Address aeh)**

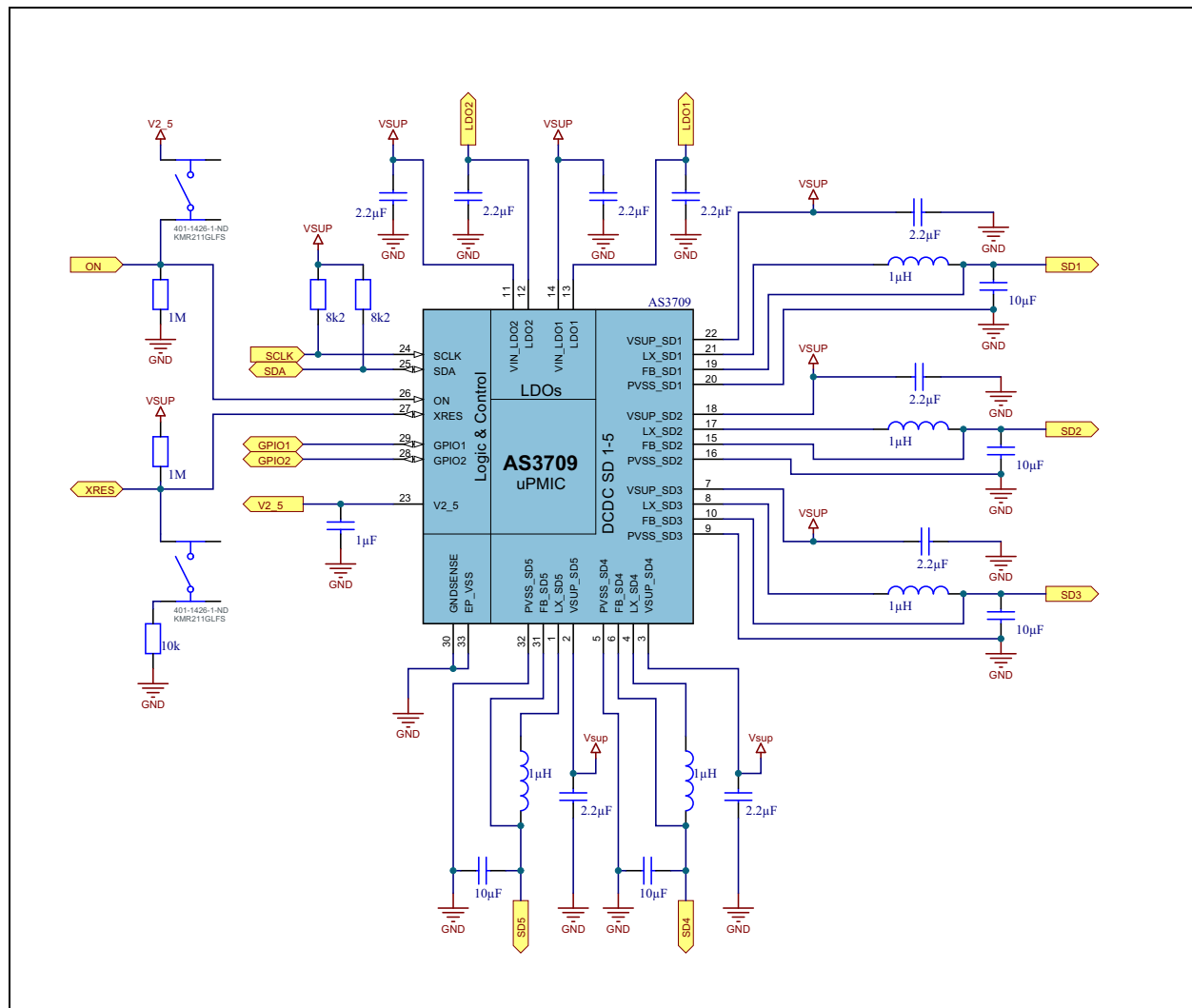
| Addr: aeh |          | Fuse14    |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg5_V   | b00000000 | RW     | Define startup voltage for regulator 5 |

**Figure 102:**  
**Fuse 15 Register (Address afh)**

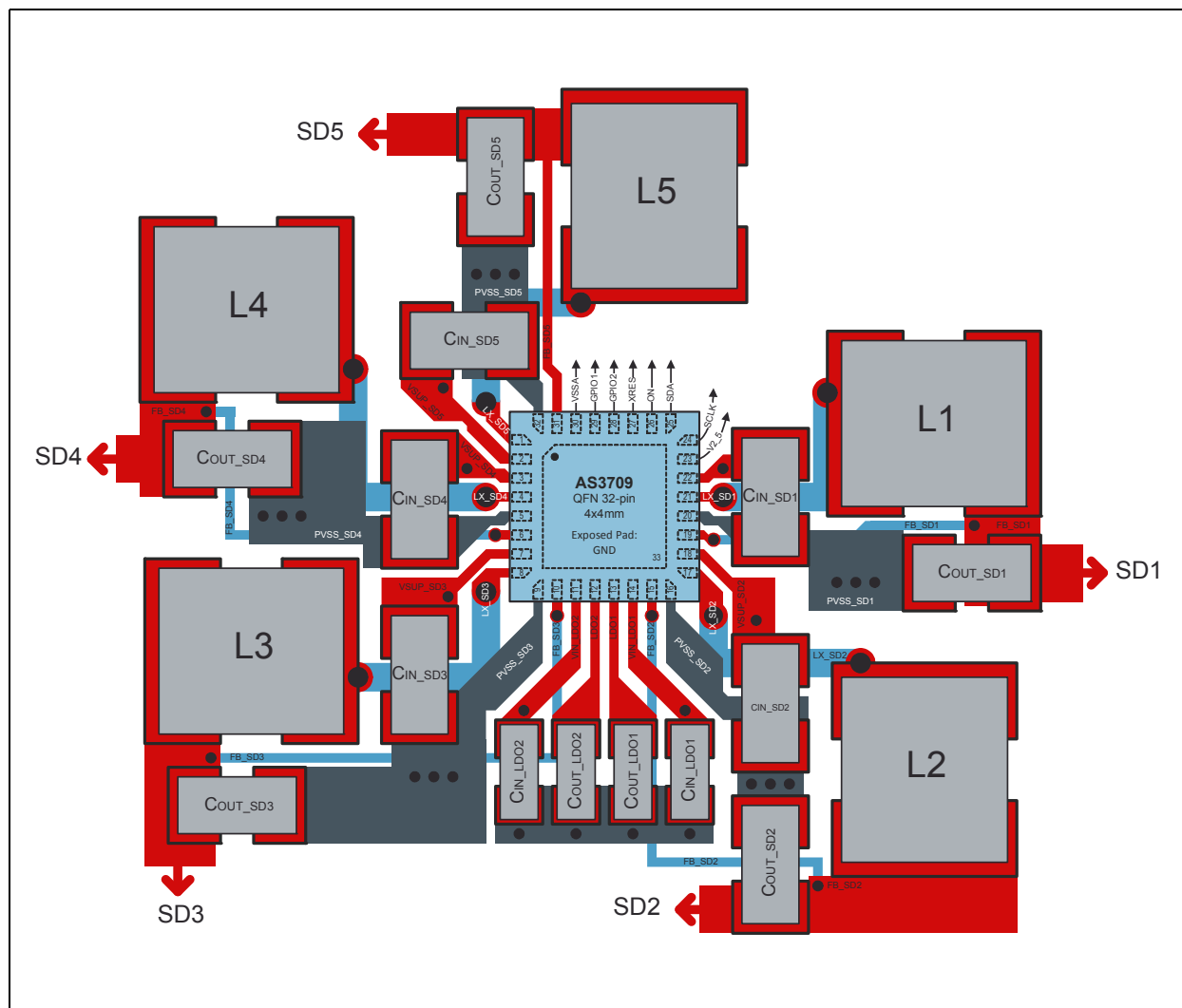
| Addr: afh |          | Fuse15    |        |                                        |
|-----------|----------|-----------|--------|----------------------------------------|
| Bit       | Bit Name | Default   | Access | Bit Description                        |
| 7:0       | reg6_V   | b00000000 | RW     | Define startup voltage for regulator 6 |

## Application Information

### Figure 103: Application Schematic

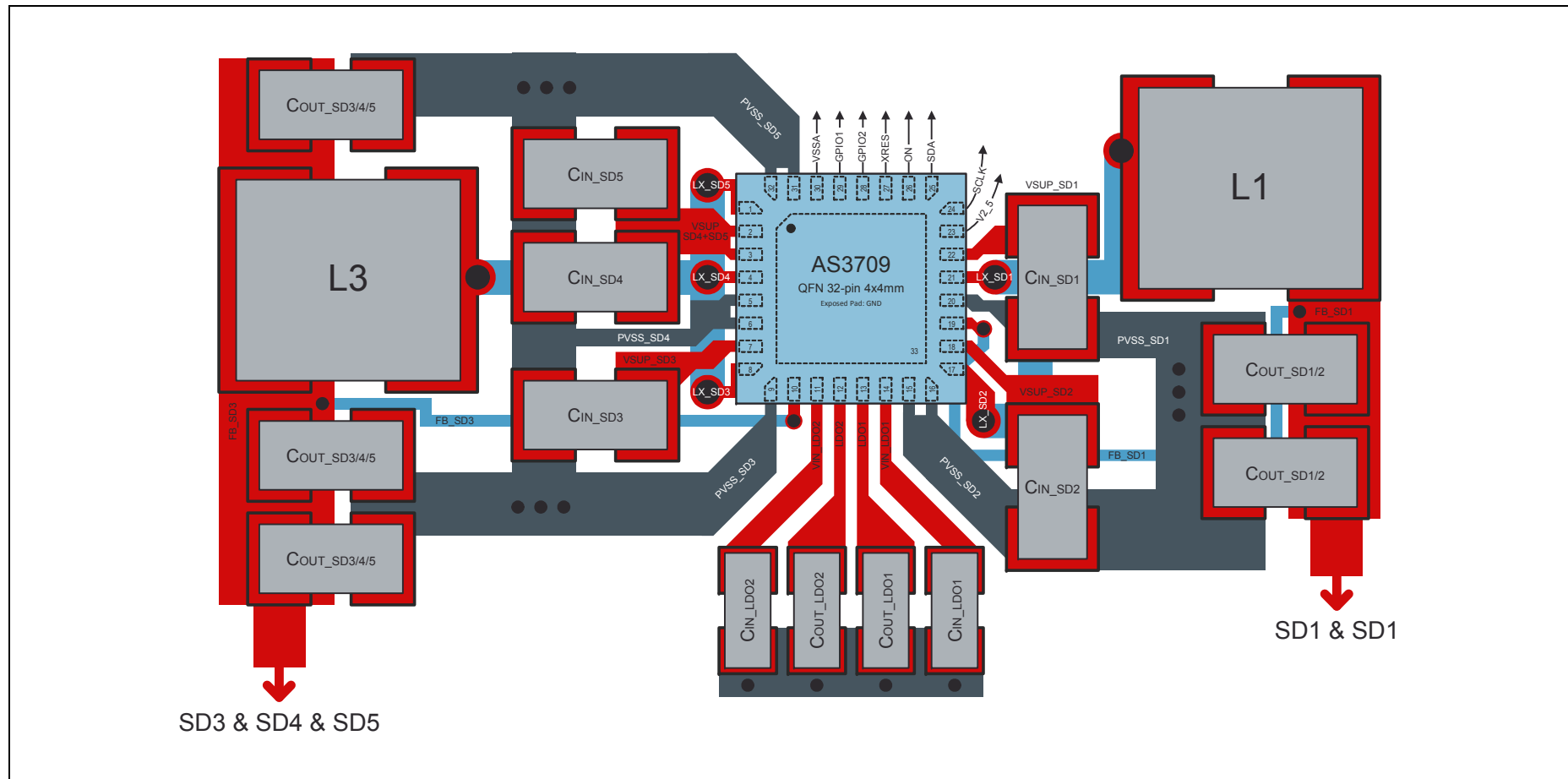


**Figure 104:**  
**Layout Guidelines 1/3**



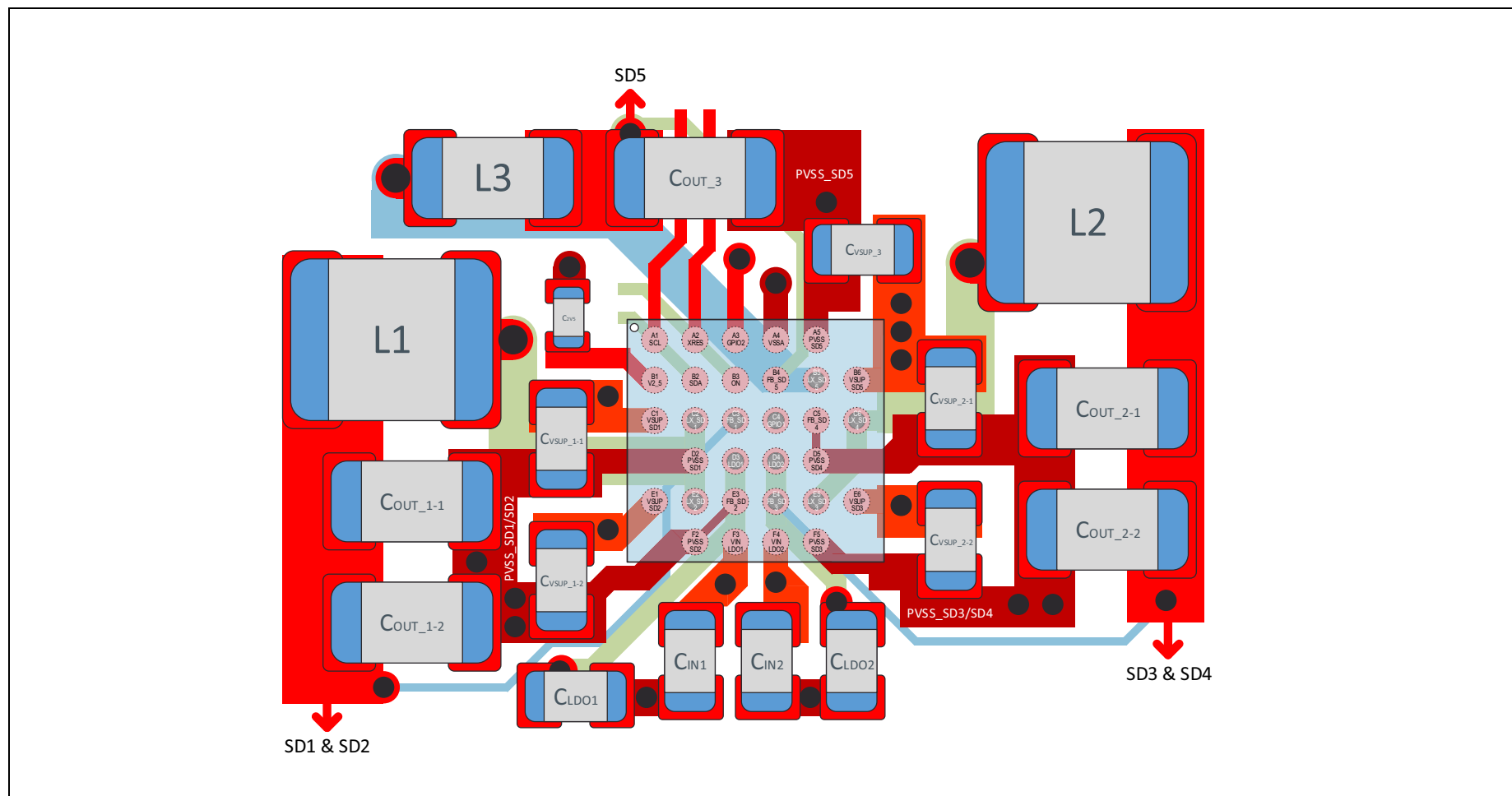
**Layout Guidelines 1/3:** This figure shows the recommended layout and placement of the external components for the 5 x 1A application circuit. Red lines and areas are connections on TOP layer. Grey lines and areas are GND and PVSS connections on TOP layer. Light blue lines and areas are connections on an inner layer or BOTTOM layer. Black round dots are vias. VSUP areas should be connected to an inner VSUP plane via vias. GND and PVSS areas should be connected to an inner GND plane via vias. A PCB with minimum 4 layers is recommended.

**Figure 105:**  
**Layout Guidelines 2/3**



**Layout Guidelines 2/3:** This figure shows the recommended layout and placement of the external components for the 1 x 2A & 1 x 3A application circuit. Red lines and areas are connections on TOP layer. Grey lines and areas are GND and PVSS connections on TOP layer. Light blue lines and areas are connections on an inner layer or BOTTOM layer. Black round dots are vias. VSUP areas should be connected to an inner VSUP plane via vias. GND and PVSS areas should be connected to an inner GND plane via vias. A PCB with minimum 4 layers is recommended.

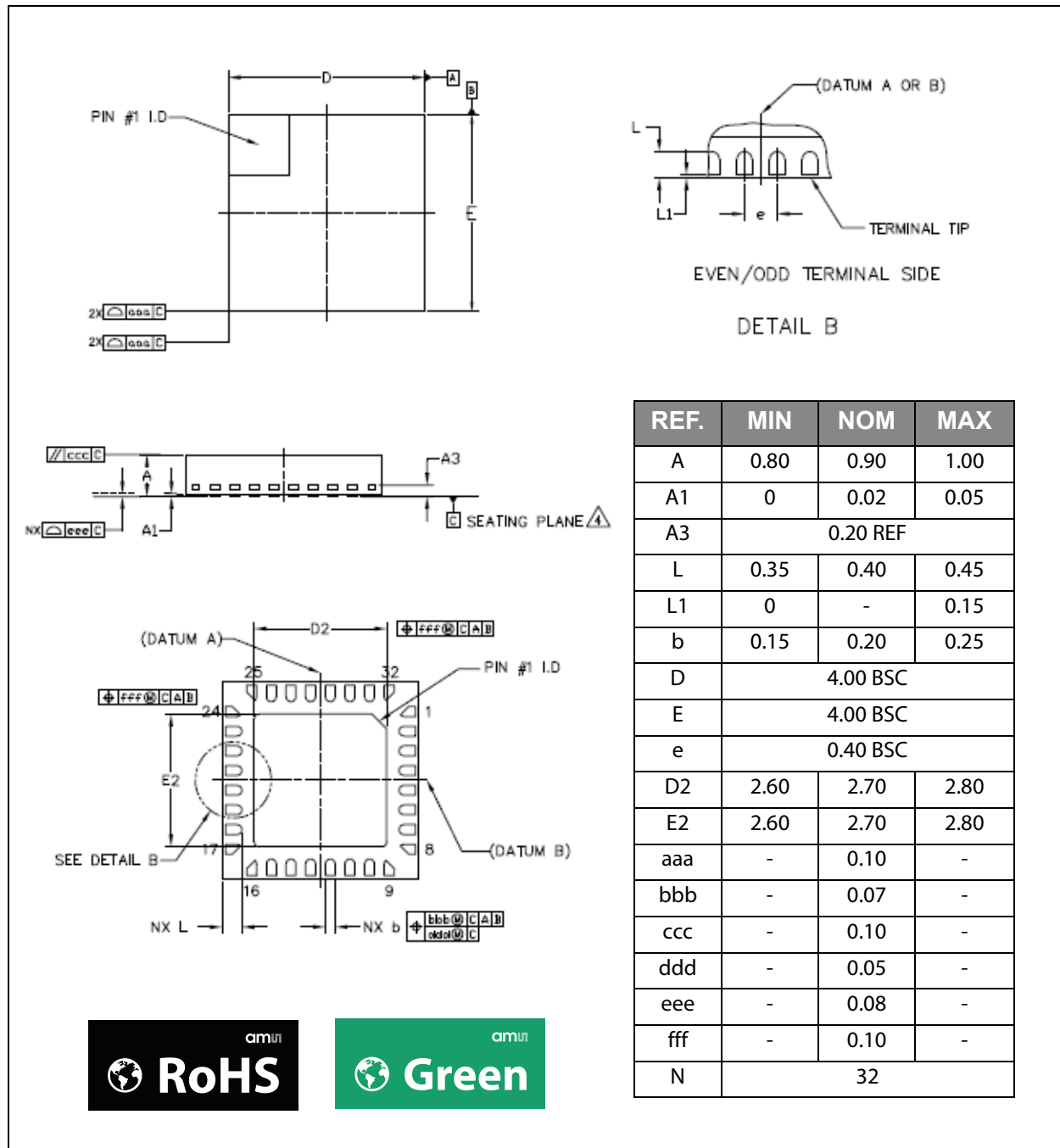
**Figure 106:**  
**WL-CSP Layout Guidelines 3/3**



**Layout Guidelines 3/3:** This figure shows the recommended layout and placement of the external components for the 1 x 1A & 2 x 2A application circuit. Red lines and areas are connections on TOP layer. Dark red lines and areas are GND and PVSS lines on TOP layer. Orange lines and areas are VSUP lines on TOP layer. Light green lines and areas are connections on an inner layer and light blue lines and areas are connections on BOTTOM layer. Black round dots are vias. VSUP areas should be connected to an inner VSUP plane via vias. GND and PVSS areas should be connected to an inner GND plane via vias. A PCB with min 6 layers is recommended.

## Package Drawings & Markings

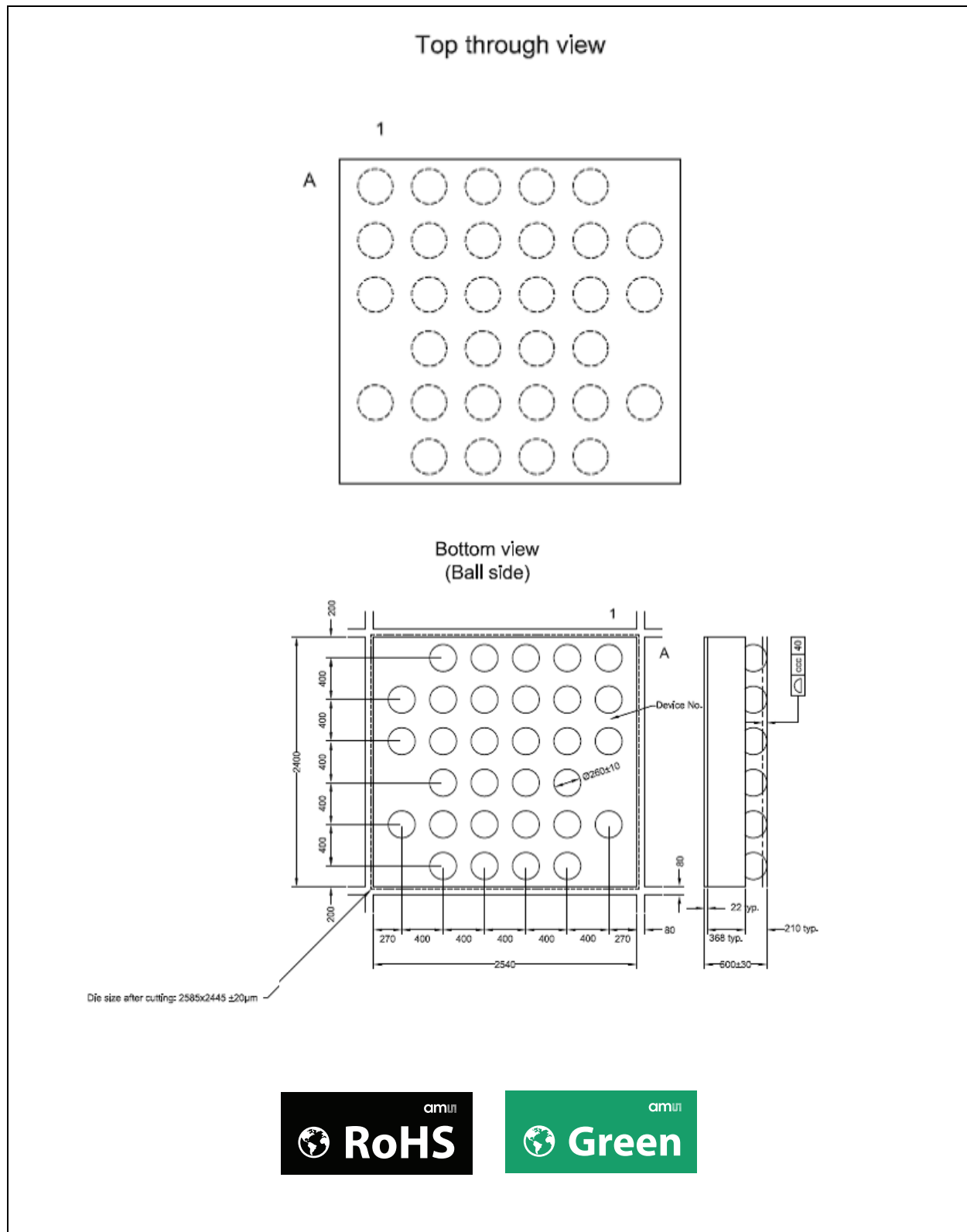
**Figure 107:**  
QFN32 4x4 0.4mm Pitch Package Drawing



### Note(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

**Figure 108:**  
**WL-CSP36 0.4mm Pitch Package Drawing**



**Note(s):**

1. Pin 1 = A1
2. ccc Coplanarity
3. All linear dimensions are in μm



Figure 109:  
QFN Marking

**QFN Marking:** Shows the package marking of the QFN product version.



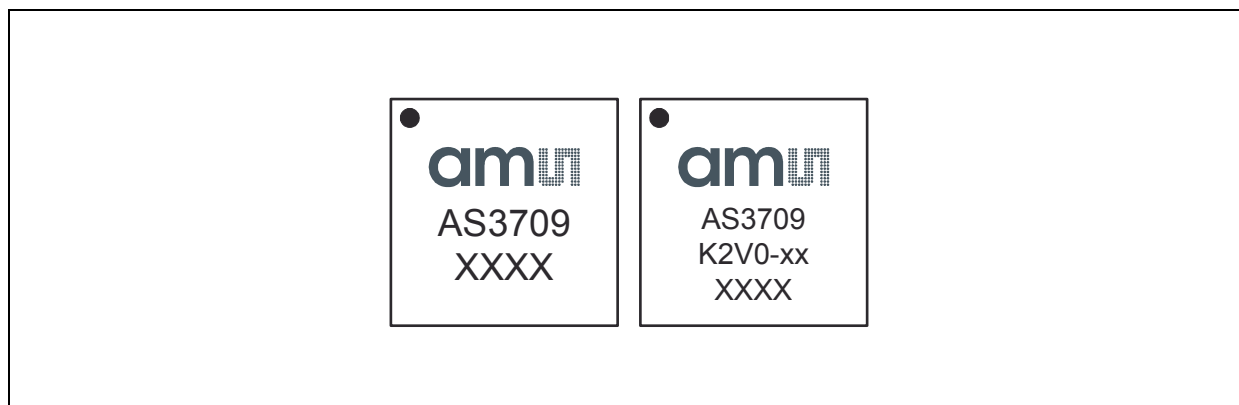
Figure 110:  
QFN Package Code

| YY   | WW                 | X                | ZZ          |
|------|--------------------|------------------|-------------|
| Year | Manufacturing week | Plant identifier | Free choice |

Figure 111:  
Start-Up Revision Code

| Revision Code | Sequence                                                                      |
|---------------|-------------------------------------------------------------------------------|
| K2V0-ES       | Engineering samples, no sequence programmed or sequence programmed on request |
| K2V0-00       | Standard programming (no sequence programmed)                                 |
| K2V0-xx       | Customer specified sequence programmed during production test                 |

**Figure 112:**  
WL-CSP Marking



**Figure 113:**  
WL-CSP Code

| XXXX      |
|-----------|
| Tracecode |

**Figure 114:**  
Start-Up Revision Code

| Revision Code | Sequence                                                                      |
|---------------|-------------------------------------------------------------------------------|
| K2V0-ES       | Engineering samples, no sequence programmed or sequence programmed on request |
| "empty"       | Standard programming (no sequence programmed)                                 |
| K2V0-00       | Standard programming (no sequence programmed)                                 |
| K2V0-xx       | Customer specified sequence programmed during production test                 |

## Ordering & Contact Information

**Figure 115:**  
**Ordering Information**

| Ordering Code  | Package        | Marking  | OTP Programming                  | Delivery Form           | Delivery Quantity |
|----------------|----------------|----------|----------------------------------|-------------------------|-------------------|
| AS3709-BQFR-ES | 32-pin QFN 4x4 | K2V0-ES  | Sequence programmable on request | Tray                    | Max. 50 pcs       |
| AS3709-BQFM-00 | 32-pin QFN 4x4 | K2V0-00  | Default sequence                 | Tape & Reel (mini reel) | 1000 pcs/reel     |
| AS3709-BQFM-?? | 32-pin QFN 4x4 | K2V0-??  | Customer specified sequence      | Tape & Reel (mini reel) | 1000 pcs/reel     |
| AS3709-BQFT-?? | 32-pin QFN 4x4 | K2V0-??  | Customer specified sequence      | Tape & Reel             | 6000 pcs/reel     |
| AS3709-BWLW-ES | 36-ball WL-CSP | K2V0-ES  | Sequence programmable on request | Waffle Pack             | Max. 50 pcs       |
| AS3709-BWLM-00 | 36-ball WL-CSP | K2V0-00  | Default sequence                 | Tape & Reel (mini reel) | 1000 pcs/reel     |
| AS3709-BWLM-?? | 36-ball WL-CSP | K2V0-0?? | Customer specified sequence      | Tape & Reel (mini reel) | 1000 pcs/reel     |
| AS3709-BWLT-?? | 36-ball WL-CSP | K2V0-??  | Customer specified sequence      | Tape & Reel             | 6000 pcs/reel     |

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|--------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice                                                                    |
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**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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