

Ultra-Low Noise, Precision, High Slew Rate Wideband Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate 28V/μs (Min)
- Wide Gain Bandwidth ($A_V \geq 10$) 100MHz (Min)
- Low Noise (@ 1kHz) 4.5nV/√Hz (Max)
- Low Offset Voltage 100μV (Max)
- Low Offset Drift With Temperature .. 1.8μV/°C (Max)
- High CMRR 100dB (Min)
- High Voltage Gain 700V/mV (Min)

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5147/883 monolithic operational amplifier features an unparalleled combination of precision D.C. and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed wideband capability.

This amplifier's impressive list of features include low V_{OS} , wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

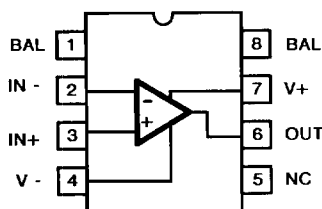
Using the HA-5147/883 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

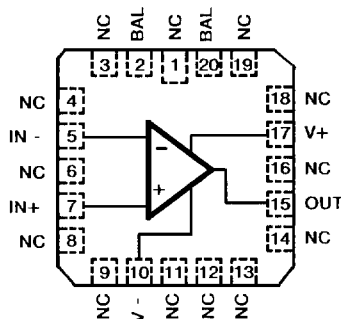
This device can easily be used as a design enhancement by directly replacing the 725, OP-25, OP-06, OP-07, OP-27 and OP-37 where gains are greater than ten. The HA-5147/883 is available in TO-99 Metal Can, Ceramic 8 Pin Mini-DIP, and 20 Pin Ceramic LCC packages.

Pinouts

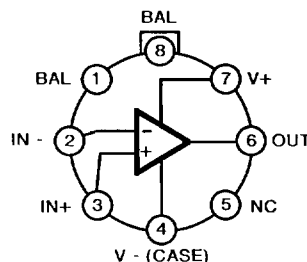
HA7-5147/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5147/883 (CERAMIC LCC)
TOP VIEW



HA2-5147/883 (METAL CAN)
TOP VIEW



Specifications HA-5147/883

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	44V
Differential Input Voltage (Note 6)	0.7V
Voltage at Either Input Terminal	V+ to V-
Input Current	25mA
Differential Output Current	Full Short Circuit Protection
Junction Temperature (T _J)	+175°C
Storage Temperature Range	-65°C to +150°C
ESD Rating	< 2000V
Lead Temperature (Soldering 10 sec)	+275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	84°C/W	25°C/W
Metal Can Package	98°C/W	30°C/W
Package Power Dissipation Limit at +75°C for T _J ≤ +175°C		
Ceramic DIP Package	1.22W	
Ceramic LCC Package	1.19W	
Metal Can Package	1.02W	
Package Power Dissipation Derating Factor Above +75°C		
Ceramic DIP Package	12.2mW/°C	
Ceramic LCC Package	11.9mW/°C	
Metal Can Package	10.2mW/°C	

Recommended Operating Conditions

Operating Temperature Range	-55°C to +125°C	V _{INcm} ≤ 1/2 (V+ - V-)
Operating Supply Voltage	±15V	R _L ≥ 600Ω

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V _{IO}	V _{CM} = 0V	1	+25°C	-100	100	μV
			2, 3	+125°C, -55°C	-300	300	μV
Input Bias Current	I _B	V _{CM} = 0V R _S = 10kΩ, 50Ω $\left(\frac{ I_{B1} + I_{B2} }{2} \right)$	1	+25°C	-	80	nA
			2, 3	+125°C, -55°C	-	150	nA
Input Offset Current	I _{IO}	V _{CM} = 0V +R _S = 10kΩ -R _S = 10kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-135	135	nA
Common Mode Range	+CMR	V+ = 4.7V V- = -25.3V	1	+25°C	10.3	-	V
			2, 3	+125°C, -55°C	10.3	-	V
	-CMR	V+ = 25.3V V- = -4.7V	1	+25°C	-	-10.3	V
			2, 3	+125°C, -55°C	-	-10.3	V
Large Signal Voltage Gain	+A _{VOL}	V _{OUT} = 0V and +10V R _L = 2kΩ	4	+25°C	700	-	kV/V
			5, 6	+25°C, -55°C	300	-	kV/V
	-A _{VOL}	V _{OUT} = 0V and -10V R _L = 2kΩ	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV _{CM} = +11V	1	+25°C	100	-	dB
		ΔV _{CM} = +10V	2, 3	+125°C, -55°C	100	-	dB
	-CMRR	ΔV _{CM} = -11V	1	+25°C	100	-	dB
		ΔV _{CM} = -10V	2, 3	+125°C, -55°C	100	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = $\pm 15\text{V}$, $R_{\text{SOURCE}} = 50\Omega$, $R_{\text{LOAD}} = 100\text{k}\Omega$, $V_{\text{OUT}} = 0\text{V}$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	+V _{OUT1}	R _L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	-V _{OUT1}	R _L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	+V _{OUT2}	R _L = 600Ω	4	+25°C	10	-	V
-V _{OUT2}	R _L = 600Ω	4	+25°C	-	-10	V	
Output Current	+I _{OUT}	V _{OUT} = -10V	4	+25°C	16.5	-	mA
	-I _{OUT}	V _{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	+I _{CC}	V _{OUT} = 0V	1	+25°C	-	4	mA
		I _{OUT} = 0mA	2, 3	+125°C, -55°C	-	4	mA
	-I _{CC}	V _{OUT} = 0V	1	+25°C	-4	-	mA
		I _{OUT} = 0mA	2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV _{SUP} = 14V	1	+25°C	86	-	dB
		ΔV _{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV _{SUP} = 14V	1	+25°C	86	-	dB
		ΔV _{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	+V _{IOAdj}	Note 5	1	+25°C	V _{IO} -1	-	mV
			2, 3	+125°C, -55°C	V _{IO} -1	-	mV
	-V _{IOAdj}	Note 5	1	+25°C	V _{IO} +1	-	mV
			2, 3	+125°C, -55°C	V _{IO} +1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = $\pm 15\text{V}$, $R_{\text{SOURCE}} = 50\Omega$, $R_{\text{LOAD}} = 2\text{k}\Omega$, $C_{\text{LOAD}} = 50\text{pF}$, $A_{\text{VCL}} = +10\text{V/V}$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	$V_{\text{OUT}} = -4\text{V to } +4\text{V}$	7	+25°C	28	-	V/ μs
	-SR	$V_{\text{OUT}} = +4\text{V to } -4\text{V}$	7	+25°C	28	-	V/ μs
Rise & Fall Time	T _R	$V_{\text{OUT}} = 0 \text{ to } +200\text{mV}$ $10\% \leq T_R \leq 90\%$	7	+25°C	-	50	ns
	T _F	$V_{\text{OUT}} = 0 \text{ to } -200\text{mV}$ $10\% \leq T_F \leq 90\%$	7	+25°C	-	50	ns
Overshoot	+OS	$V_{\text{OUT}} = 0 \text{ to } +200\text{mV}$	7	+25°C	-	40	%
	-OS	$V_{\text{OUT}} = 0 \text{ to } -200\text{mV}$	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = $\pm 15V$, $R_{LOAD} = 2k\Omega$, $C_{LOAD} = 50pF$, $A_v = +10V/V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Average Offset Voltage Drift	$V_{IO TC}$	$V_{CM} = 0V$	1	$-55^{\circ}C$ to $+125^{\circ}C$	-	1.8	$\mu V/^{\circ}C$
Differential Input Resistance	R_{IN}	$V_{CM} = 0V$	1	$+25^{\circ}C$	0.8	-	$M\Omega$
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	$+25^{\circ}C$	-	0.25	μV_{p-p}
Input Noise Voltage Density	E_n	$R_S = 20\Omega$, $f_0 = 10Hz$	1, 4	$+25^{\circ}C$	-	8.0	$nV/\sqrt{Hz}$
		$R_S = 20\Omega$, $f_0 = 100Hz$	1, 4	$+25^{\circ}C$	-	5.6	$nV/\sqrt{Hz}$
		$R_S = 20\Omega$, $f_0 = 1kHz$	1, 4	$+25^{\circ}C$	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	$R_S = 2M\Omega$, $f_0 = 10Hz$	1, 4	$+25^{\circ}C$	-	4.0	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega$, $f_0 = 100Hz$	1, 4	$+25^{\circ}C$	-	2.3	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega$, $f_0 = 1kHz$	1, 4	$+25^{\circ}C$	-	0.6	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	$V_O = 100mV$, $f_0 = 10kHz$	1	$+25^{\circ}C$	120	-	MHz
		$V_O = 100mV$, $f_0 = 1MHz$	1	$+25^{\circ}C$	100	-	MHz
Full Power Bandwidth	FPBW	$V_{PEAK} = 10V$	1, 2	$+25^{\circ}C$	445	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 2k\Omega$, $C_L = 50pF$	1	$-55^{\circ}C$ to $+125^{\circ}C$	± 10	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	$+25^{\circ}C$	-	600	μs
Output Resistance	R_{OUT}	Open Loop	1	$+25^{\circ}C$	-	100	Ω
Quiescent Power Consumption	PC	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	$-55^{\circ}C$ to $+125^{\circ}C$	-	120	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using $FPBW = \text{Slew Rate} / (2\pi V_{PEAK})$.

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.

5. Offset adjustment range is $[V_{IO} (\text{Measured}) \pm 1mV]$ minimum referred to output.
This test is for functionality only to assure adjustment through 0V.

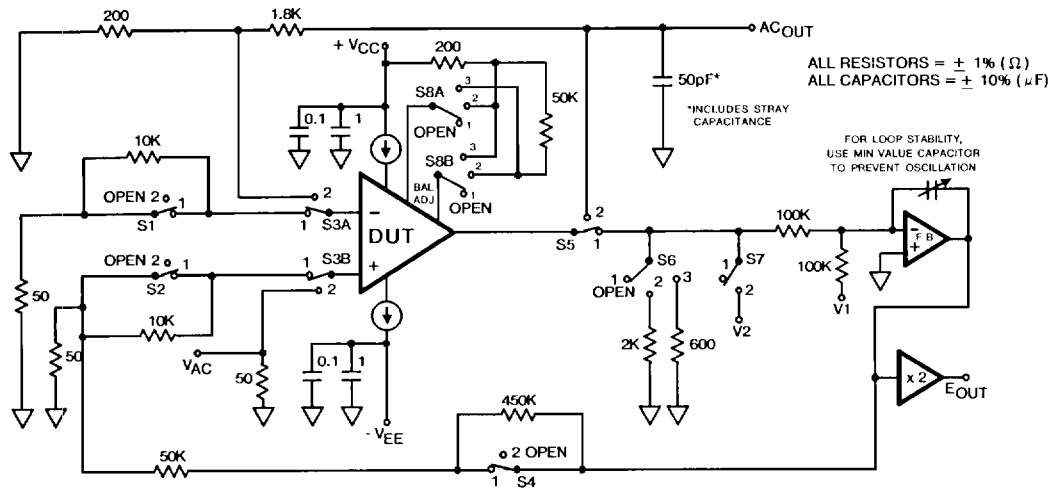
6. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

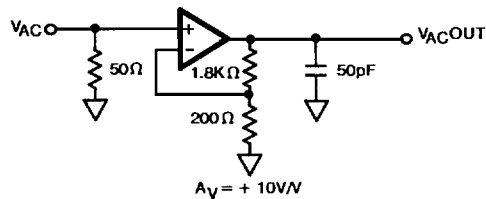
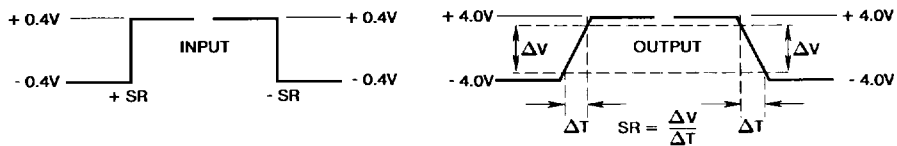
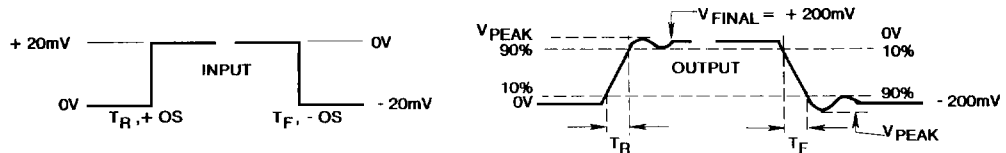
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO} , which is Subgroups 1, 2, and 3.

Test Circuit (Applies to Tables 1 and 2)

For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5147 Op-Amp Test Methods". The HA-5147/883 is A.C. Tested (Table 2) at $A_V = +10V/V$.

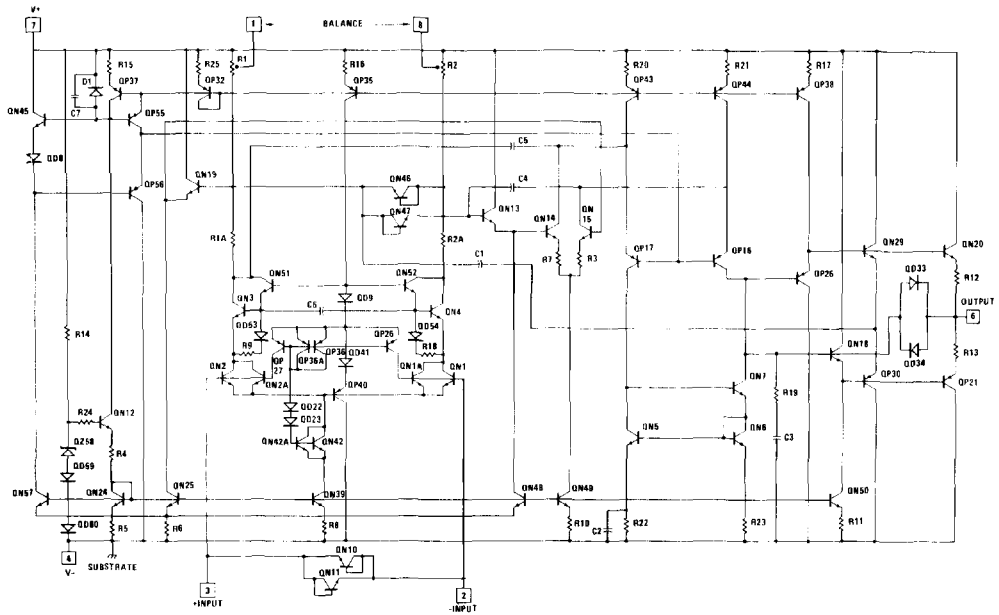
Test Waveforms**SIMPLIFIED TEST CIRCUIT** (Applies to Table 2)**SLEW RATE WAVEFORM****TRANSIENT RESPONSE WAVEFORM**

NOTE: Measured on Both positive and negative transitions.

The circuit diagram shows an operational amplifier (op-amp) configured as a precision rectifier. The op-amp has pins 1, 2, 3, 4, 5, 6, 7, and 8. Pin 1 is connected to pin 8. Pin 2 is connected to the inverting input (-). Pin 3 is connected to the non-inverting input (+). Pin 4 is connected to the negative supply rail. Pin 5 is connected to the negative supply rail. Pin 6 is connected to the output. Pin 7 is connected to the positive supply rail. Pin 8 is connected to the positive supply rail. The circuit includes a resistor R_1 connected between the input v and the inverting input. A diode D_2 is connected between the input v and the negative supply rail. A capacitor C_2 is connected between the input v and the negative supply rail. A resistor R_3 is connected between the non-inverting input and the negative supply rail. A feedback network consisting of a resistor R_2 and a diode D_1 is connected between the output and the inverting input. The output is labeled v_o .

$R_1 = R_3 = 1k\Omega, \pm 5\%, 1/4W$ (Min)
 $R_2 = 10k\Omega \pm 5\%, 1/4W$ (Min)
 $C_1 = C_2 = 0.01\mu F$ per Socket (Min) or $0.1\mu F$ /Row (Min)
 $D_1 = D_2 = IN4002$ or Equivalent/Board
 $|V(+)-V(-)| = 30V$

Schematic Diagram



Die Characteristics**DIE DIMENSIONS:**

104.3 x 65 x 19 mils
(2650 x 1650 x 483 μm)

METALLIZATION:

Type: Aluminum
Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$3.6 \times 10^5 \text{A/cm}^2$ @15mA

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:

Type: Silox
Thickness: $7\text{k}\text{\AA} \pm 0.7\text{k}\text{\AA}$

TRANSISTOR COUNT: 63**PROCESS: HFHB Bipolar Dielectric Isolation****DIE ATTACH:**

Material: Gold/Silicon Eutectic Alloy

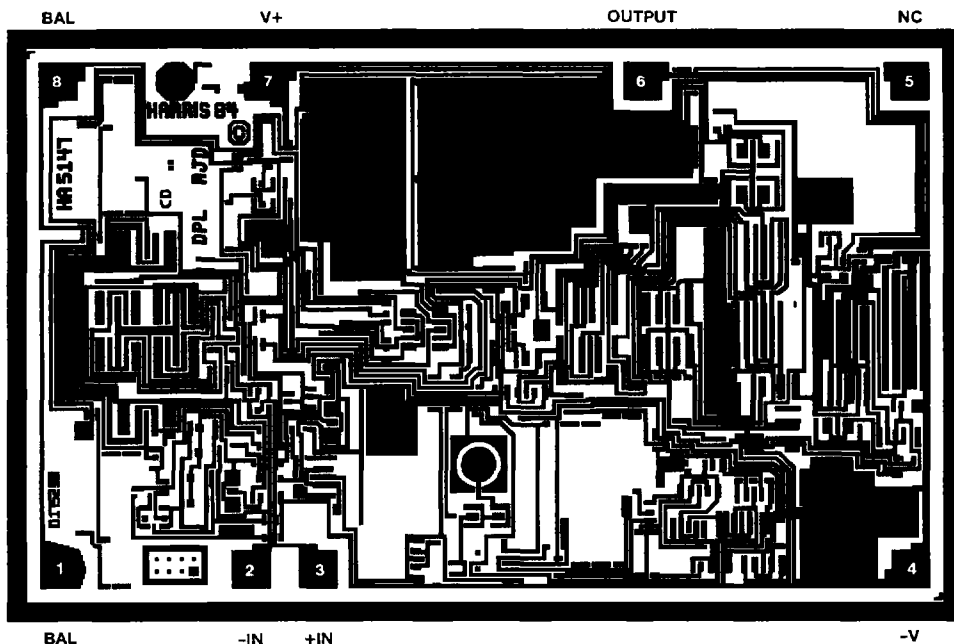
Temperature: Ceramic DIP — 460°C (Max)

Ceramic LCC — 420°C (Max)

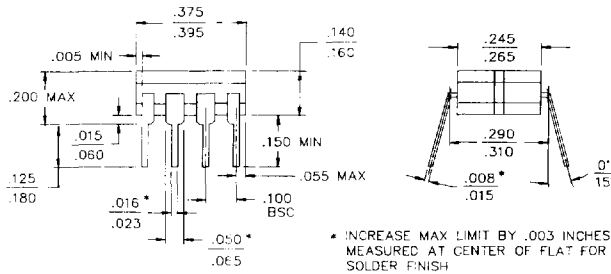
Metal Can — 420°C (Max)

Metallization Mask Layout

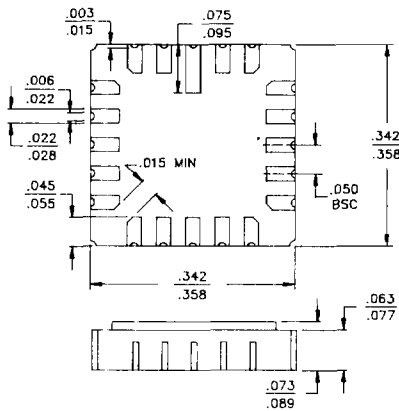
HA-5147/883



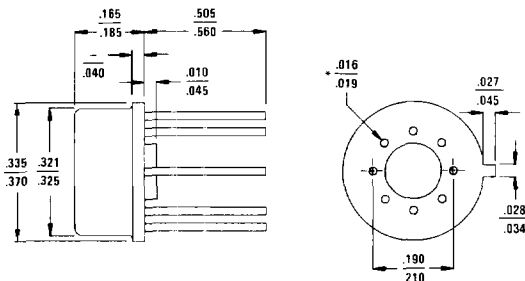
NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

Packaging †**8 PIN CERAMIC DIP**

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
 Material: Glass Frit
 Temperature: 450°C ± 10°C
 Method: Furnace Seal
INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al₂O₃
PACKAGE SEAL:
 Material: Gold/Tin (80/20)
 Temperature: 320°C ± 10°C
 Method: Furnace Braze
INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
 Material: No Seal Material
 Temperature: Room Temperature
 Method: Resistance Weld
INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

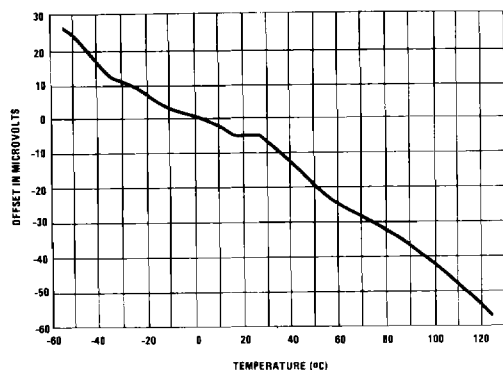
DESIGN INFORMATION

Ultra-Low Noise, Precision, High Slew Rate Wideband Operational Amplifier

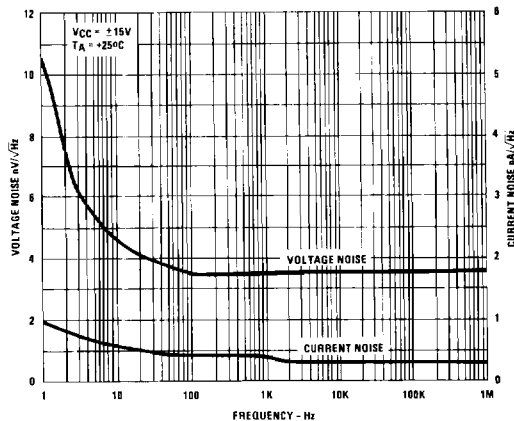
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$

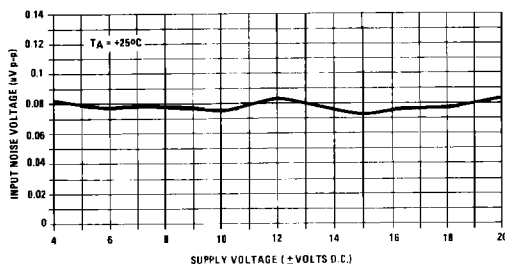
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



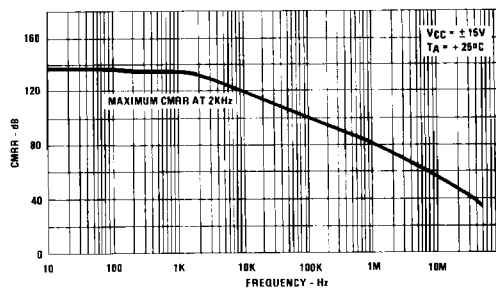
NOISE CHARACTERISTICS



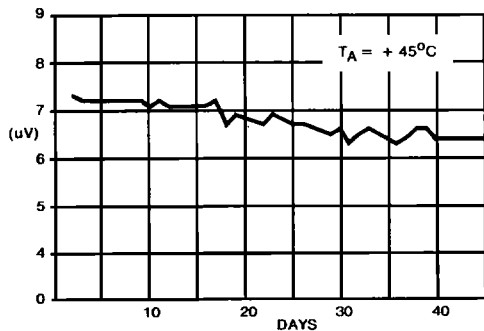
NOISE vs. SUPPLY VOLTAGE



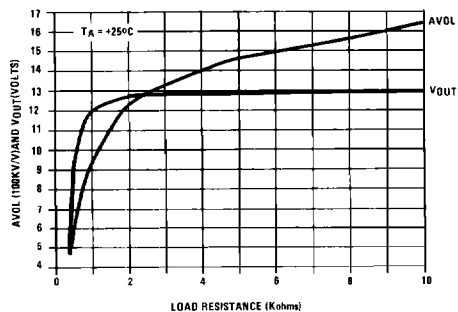
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME



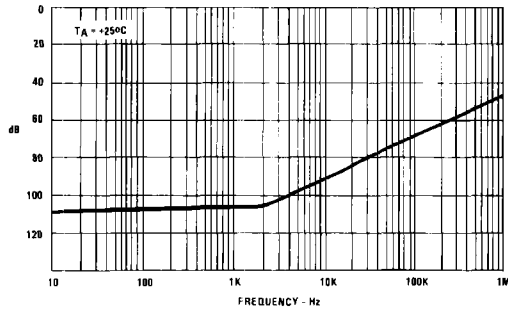
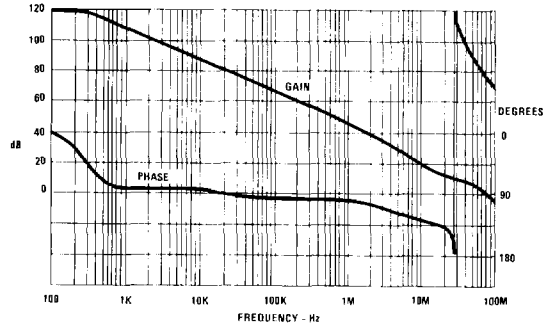
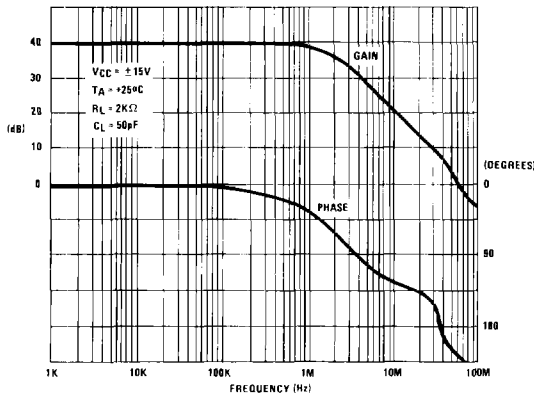
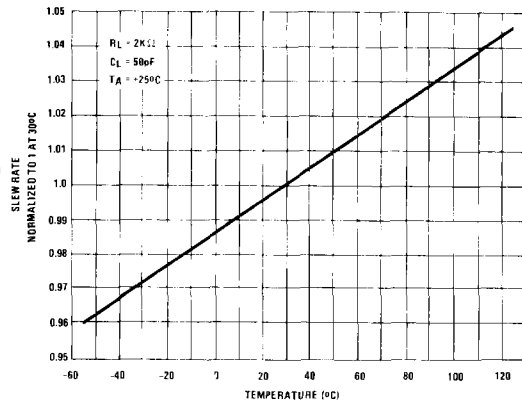
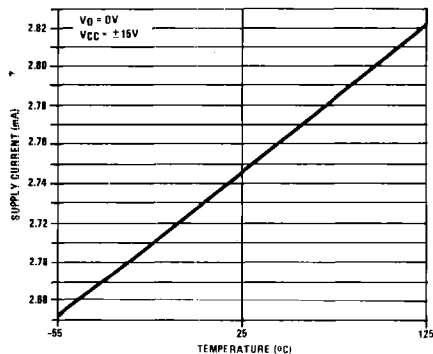
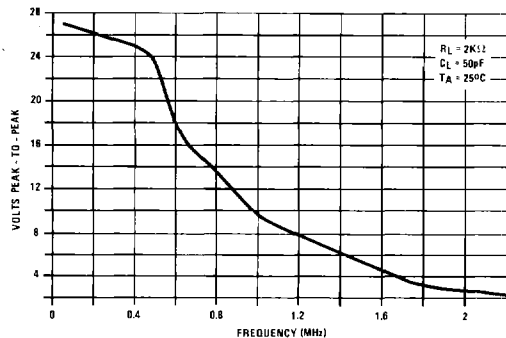
AVOL AND V_{OUT} vs. LOAD RESISTANCE



DESIGN INFORMATION (Continued)

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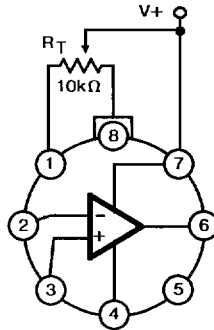
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$

PSRR vs. FREQUENCY**OPEN LOOP GAIN AND PHASE vs. FREQUENCY****CLOSED LOOP GAIN AND PHASE vs. FREQUENCY****NORMALIZED SLEW RATE vs. TEMPERATURE****SUPPLY CURRENT vs. TEMPERATURE** **$V_{\text{OUT MAX}}$ vs. FREQUENCY
UNDISTORTED SINEWAVE OUTPUT**

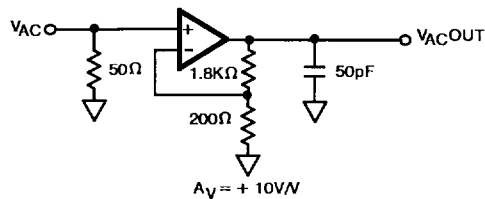
DESIGN INFORMATION (Continued)

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Typical Performance Information Unless Otherwise Specified: $T_A = +25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

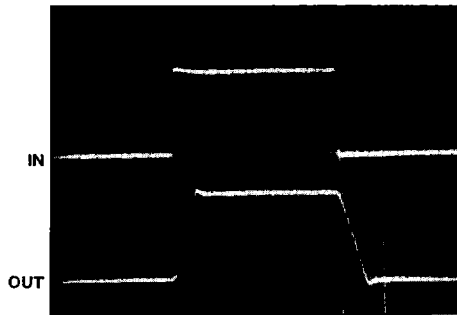
Tested Offset Adjustment Range is $|V_{\text{OS}}| + \text{mV}$ minimum referred to output. Typical Range is $\pm 4\text{mV}$ with $R_T = 10\text{k}\Omega$.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT**MEASURED LARGE SIGNAL RESPONSE**

Vertical Scale: (Volts: Input = 0.5V/Div.)

(Volts: Output = 5V/Div.)

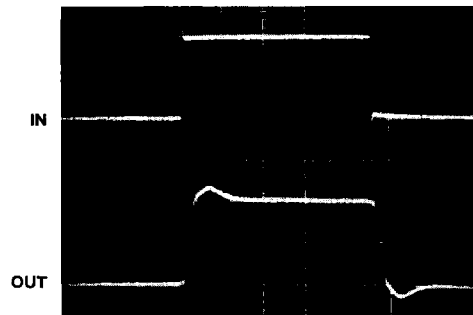
Horizontal Scale: (Time: 500ns/Div.)

**MEASURED SMALL SIGNAL RESPONSE**

Vertical Scale: (Volts: Input = 10mV/Div.)

(Volts: Output = 100mV/Div.)

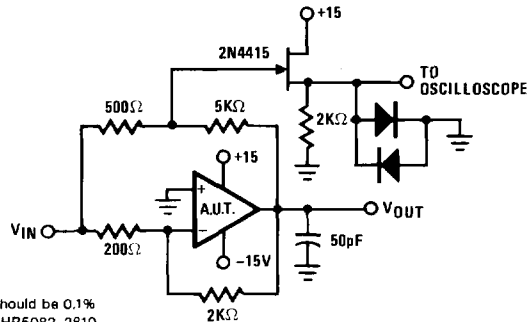
Horizontal Scale: (Time: 100ns/Div.)



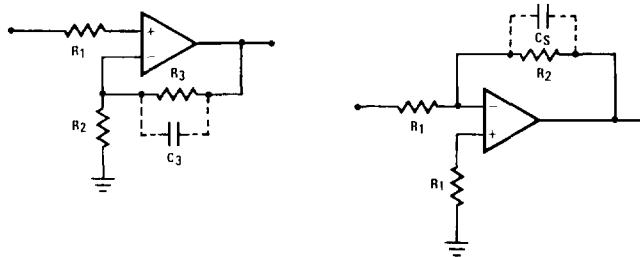
DESIGN INFORMATION (Continued)

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Typical Performance Information Unless Otherwise Specified: $T_A = +25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$

SETTLING TIME TEST CIRCUIT

- $A_V \approx -10$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2B10 recommended

SUGGESTED STABILITY CIRCUITS

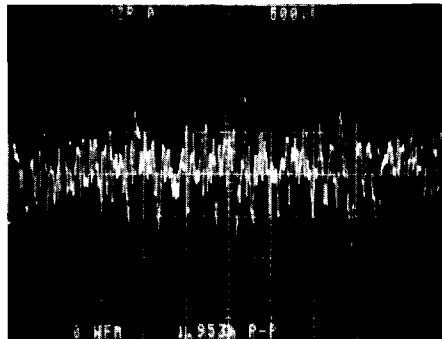
Low resistances are preferred for low noise applications as a $1\text{k}\Omega$ resistor has $4\text{nV}/\sqrt{\text{Hz}}$ of thermal noise. Total resistances of greater than $10\text{k}\Omega$ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH $A_{VCL} = 25,000\text{V/V}$

Horizontal Scale = 1sec/Div.

Vertical Scale = $0.002\mu\text{V/Div.}$

$0.08\mu\text{V}_{\text{p-p RTI}}$



DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = $\pm 15\text{V}$, $R_L = 2\text{k}\Omega$, $C_L = 50\text{pF}$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	$V_{CM} = 0\text{V}$	+25°C	30	Table 1	μV
		Full	70	Table 1	μV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	$\mu\text{V}/^\circ\text{C}$
	Versus Time	+45°C	0.71	1.5	$\mu\text{V}/\text{Month}$
Bias Current	$V_{CM} = 0\text{V}$	+25°C	± 15	Table 1	nA
		Full	± 35	Table 1	nA
Differential Input Resistance		+25°C	6	Table 3	M Ω
Input Noise Voltage	$f_o = 10\text{Hz}$	+25°C	4.4	Table 3	$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 100\text{Hz}$	+25°C	3.4	Table 3	$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 1\text{kHz}$	+25°C	3.2	Table 3	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10\text{Hz}$	+25°C	1.7	Table 3	$\text{pA}/\sqrt{\text{Hz}}$
	$f_o = 100\text{Hz}$	+25°C	1.0	Table 3	$\text{pA}/\sqrt{\text{Hz}}$
	$f_o = 1\text{kHz}$	+25°C	0.4	Table 3	$\text{pA}/\sqrt{\text{Hz}}$
Voltage Gain	$V_{OUT} = \pm 10\text{V}$	+25°C	1.8	Table 1	MV/V
		Full	1.2	Table 1	MV/V
CMRR	$\Delta V = \pm 10\text{V}$	Full	126	Table 1	dB
PSRR	$V_S = \pm 4$ to $\pm 18\text{V}$	Full	110	Table 1	dB
Slew Rate	$V_{OUT} = \pm 5\text{V}$	+25°C	35	Table 2	V/ μs
Overshoot	$V_{OUT} = \pm 200\text{mV}$	+25°C	20	Table 2	%
Settling Time	10V to 0.1%	+25°C	400	Table 3	ns
	10V to 0.01%	+25°C	800	1000	ns
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	± 4	± 5	V