OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HA-2405

August 2002 FN2892.5

30MHz, Digitally Selectable Four Channel Operational Amplifier

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

Each input-output combination of the HA-2406 is designed to be a 20V/µs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten. By connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation lead may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note AN514).

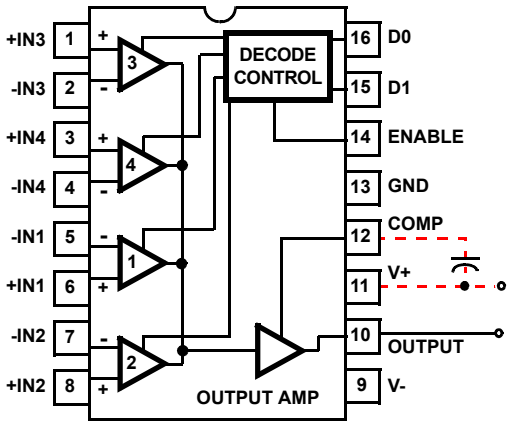
Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406. When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

During Disable Mode V_{OUT} goes to V-. For high output impedance during Disable, see HA2444.

For further design ideas, see Application Note AN514.

Pinout

HA-2406
(PDIP)
TOP VIEW)



Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk. . . . . -110dB
- High Slew Rate 20V/µs
- Low Offset Current 5nA
- Offset Voltage. 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ
- Compensation Pin for Unity Gain Capability

Applications

- Digital Control Of
  - Analog Signal Multiplexing
  - Op Amp Gains
  - Oscillator Frequencies
  - Filter Characteristics
  - Comparator Levels

Part Number Information

PART NO.	TEMP RANGE (^{O}C)	PACKAGE	PKG. NO.
HA3-2406-5	0 to 75	16 Ld PDIP	E16.3

TRUTH TABLE

D1	D0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None, V_{OUT} goes to V-

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage Between V+ and V- Terminals. 45V
Differential Input Voltage . . . . . V_{SUPPLY}
Output Current . . . . . Short Circuit Protected ($I_{SC} < \pm 33mA$)

Operating Conditions

Temperature Range
HA-2406-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	90

Maximum Junction Temperature (Plastic Package). . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: $V_{SUPPLY} = \pm 15.0V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-2406-5			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage		25	-	7	10	mV
		Full	-	-	12	mV
Bias Current (Note 7)		25	-	50	250	nA
		Full	-	-	500	nA
Offset Current (Note 7)		25	-	5	50	nA
		Full	-	-	100	nA
Input Resistance (Note 7)		25	-	30	-	MΩ
Common Mode Range		Full	±9.0	-	-	V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_{OUT} = 20V_{P-P}$	25	40	150	-	kV/V
		Full	20	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	Full	74	80	-	dB
Gain Bandwidth Product (Notes 2, 9)		25	15	30	-	MHz
Gain Bandwidth Product (Notes 3, 9)		25	3	6	-	MHz
Minimum Stable Gain	$C_{COMP} = 0$		10	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 2k\Omega$	Full	±10.0	±12.0	-	V
Output Current	$V_{OUT} = \pm 10V$	25	10	15	-	mA
Full Power Bandwidth (Notes 2, 8, 9)	$V_{OUT} = 20V_{P-P}$	25	240	320	-	kHz
Full Power Bandwidth (Notes 3, 8)	$V_{OUT} = 20V_{P-P}$	25	64	95	-	kHz
TRANSIENT RESPONSE (Note 10)						
Rise Time (Note 3)	$V_{OUT} = 200mV_{PEAK}$	25	-	30	100	ns
Overshoot (Note 3)	$V_{OUT} = 200mV_{PEAK}$	25	-	25	40	%
Slew Rate (Notes 2, 9)	$V_{OUT} = 10V_{P-P}$	25	15	20	-	V/µs
Slew Rate (Note 3)	$V_{OUT} = 10V_{P-P}$	25	4	6	-	Vµs
Settling Time (Notes 3, 4)	$V_{OUT} = 10V_{P-P}$	25	-	2.0	3.5	µs

Electrical Specifications Test Conditions: V_{SUPPLY} = ±15.0V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V. Limits apply to each of the four channels, when addressed. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{O}C)	HA-2406-5			UNITS
			MIN	TYP	MAX	
CHANNEL SELECT CHARACTERISTICS						
Digital Input Current	V_{IN} = 0V	Full	-	1	1.5	mA
Digital Input Current	V_{IN} = +5.0V	Full	-	15	-	nA
Output Delay (Notes 5, 9)		25	-	150	300	ns
Crosstalk (Note 6)		25	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS						
Supply Current		25	-	4.8	7.0	mA
Power Supply Rejection Ratio	V_S = ±10V to ±20V	Full	74	90	-	dB

NOTES:

2. A_V = +10, C_{COMP} = 0, R_L = 2kΩ, C_L = 50pF.
3. A_V = +1, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF.
4. To 0.1% of final value.
5. To 10% of final value; output then slews at normal rate to final value.
6. Unselected input to output; V_{IN} = ±10V.
7. Unselected channels have approximately the same input parameters.
8. Full power Bandwidth based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
9. Sample tested.
10. See Figure 13 for test circuit.

Schematic Diagram

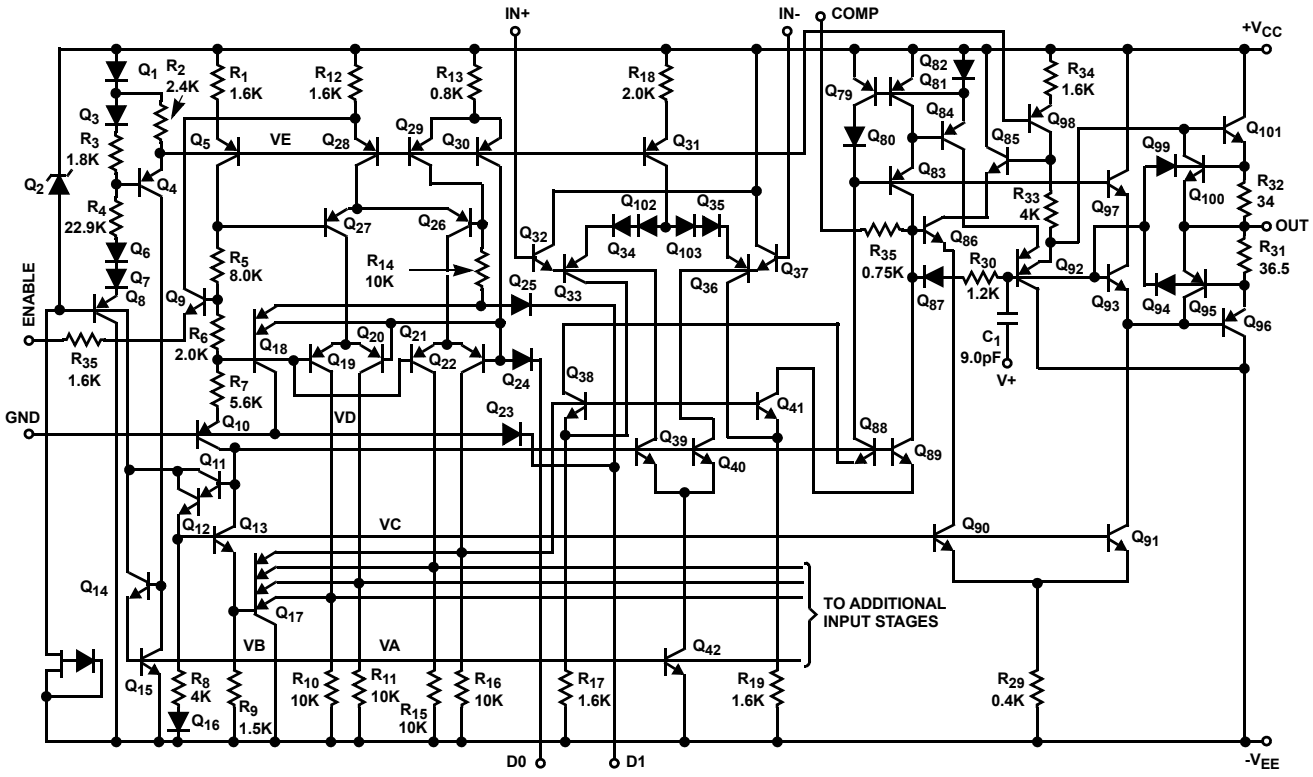


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage

Typical Applications

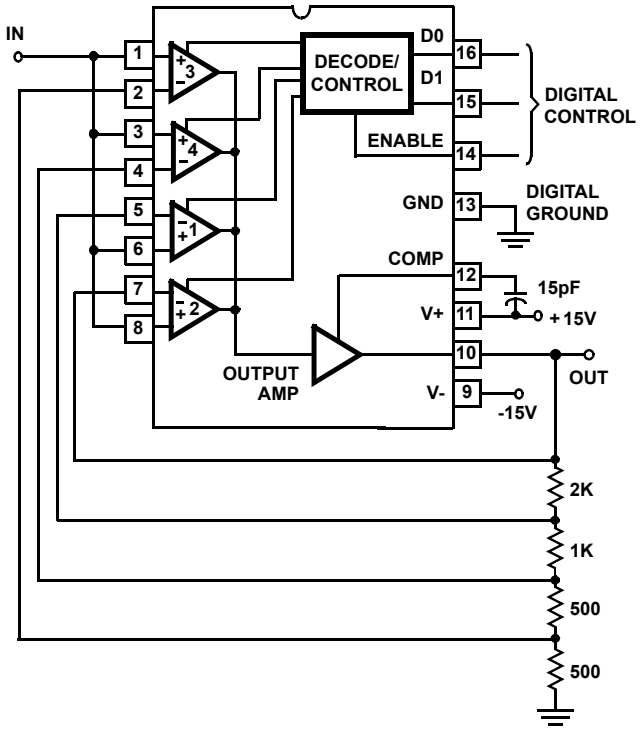
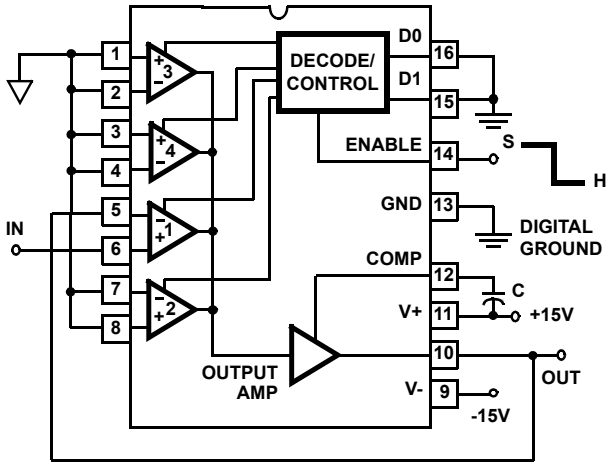


FIGURE 1. HA-2406 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



Sample Charging Rate $= \frac{I_1}{C} V/s$

Hold Drift Rate $= \frac{1_2}{C} V/s$

Switch Pedestal Error $= \frac{Q}{C} V$

$I1 \approx 150 \times 10\text{-}6A$

$I_2 \approx 200 \times 10^{-9}A$ at 25^oC

$\approx 600 \times 10^{-9}A$ at -55^oC

$\approx 100 \times 10^{-9}A$ at 125^oC

$Q \approx 2 \times 10^{-12}C$

FIGURE 2. HA-2406 SAMPLE AND HOLD

For more examples, see Intersil Application Note AN514.

Typical Performance Curves

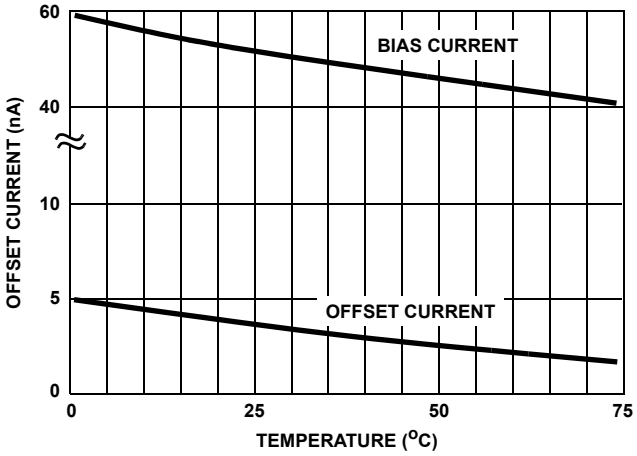


FIGURE 3. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

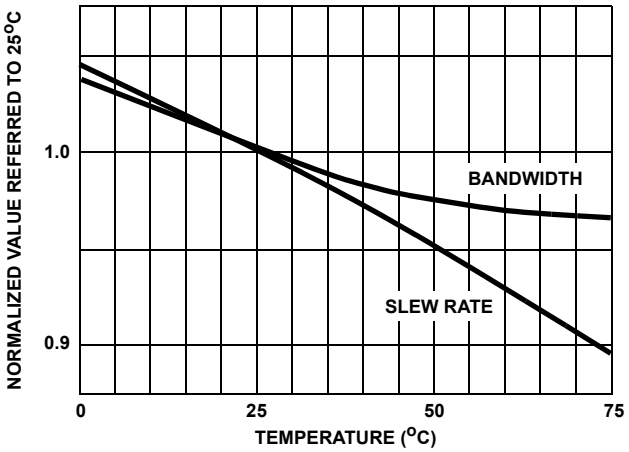


FIGURE 4. NORMALIZED AC PARAMETERS vs TEMPERATURE

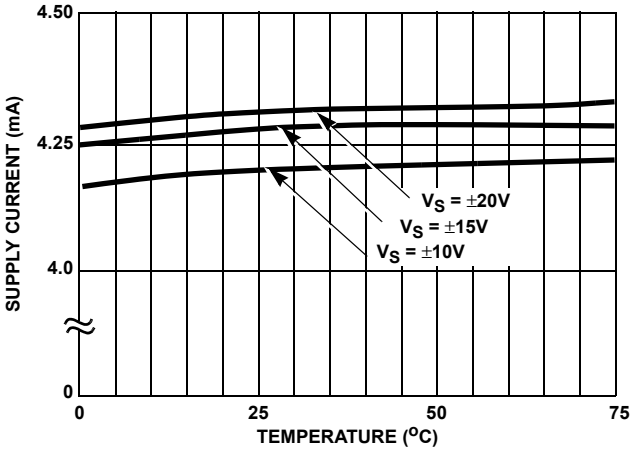


FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

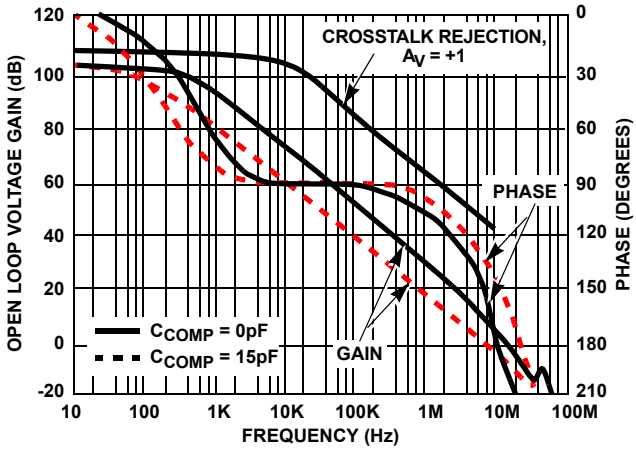


FIGURE 6. OPEN LOOP FREQUENCY AND PHASE RESPONSE

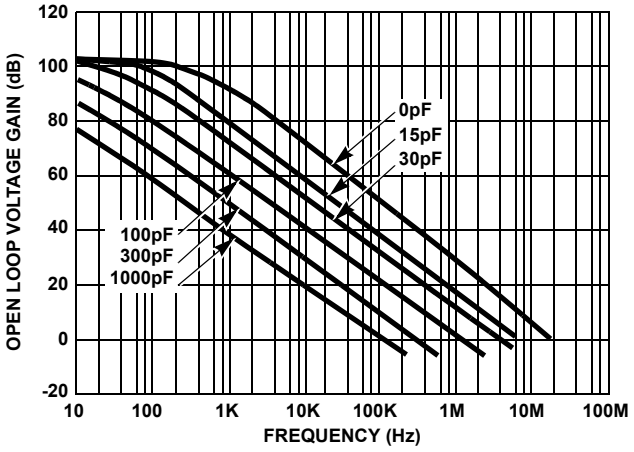


FIGURE 7. FREQUENCY RESPONSE vs C_{COMP}

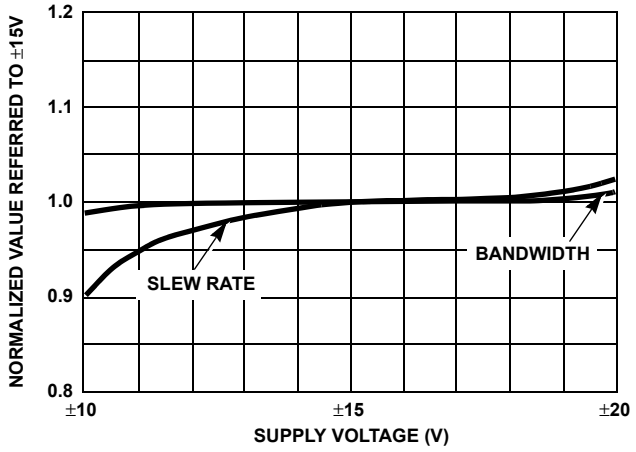


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

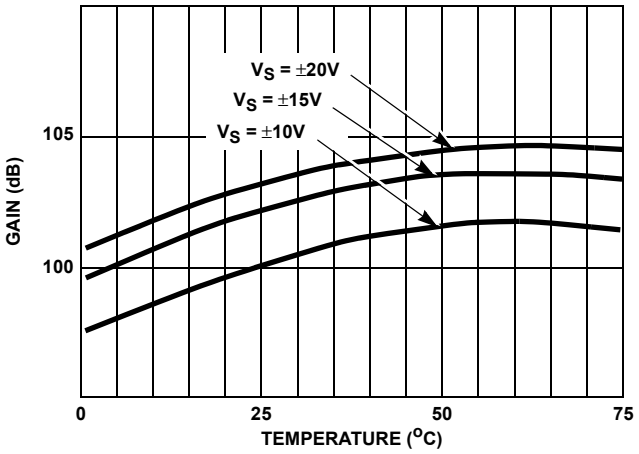


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

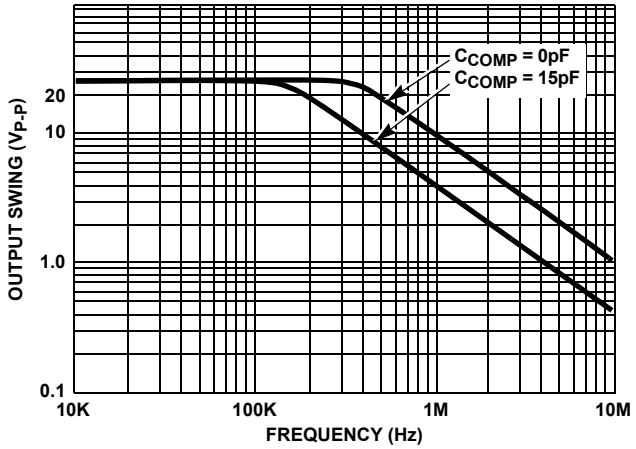


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY

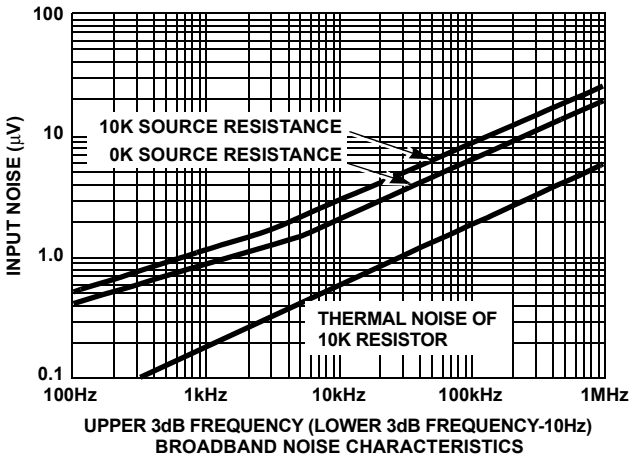


FIGURE 11. EQUIVALENT INPUT NOISE vs BANDWIDTH

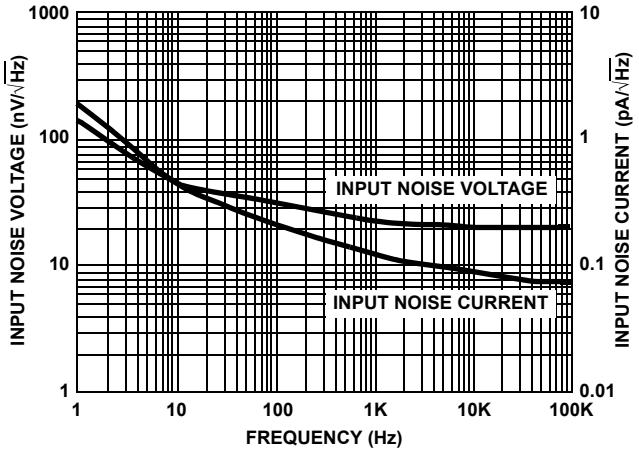


FIGURE 12. INPUT NOISE vs FREQUENCY

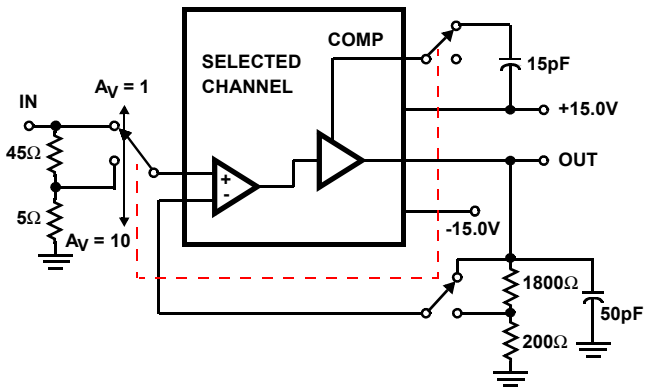
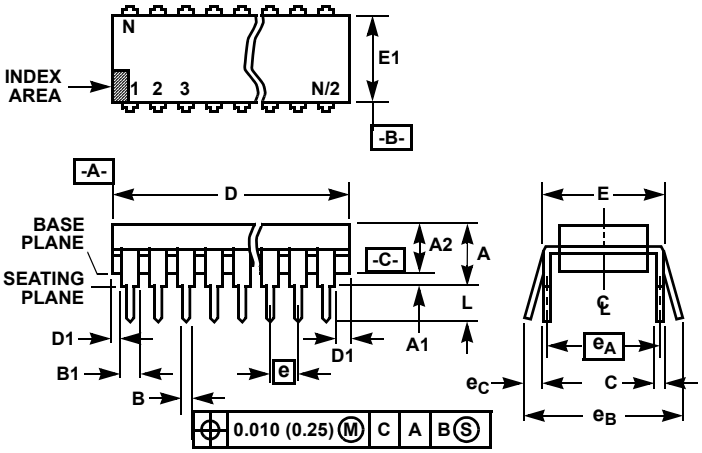


FIGURE 13. SLEW RATE AND TRANSIENT RESPONSE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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