Backlight Driver with I/O Expander

Data Sheet

ADP5520

FEATURES

- Efficient asynchronous boost converter for driving up to 6 white LEDs
- 2.7 V to 5.5 V input voltage range
- 128 programmable backlight LED current levels (30 mA maximum)
- Ambient light sensing with autonomous backlight adjustment
- Programmable backlight fade-in/fade-out times
- Programmable backlight dim and off times
- 8 configurable GPIO pins (input, output, up to 4 × 4 keypad)
- Up to 3 auxiliary LED current sinks (1 dedicated, 2 configurable)
- 64 programmable auxiliary LED current levels (14 mA maximum)
- Programmable auxiliary LED fade-in/fade-out times
- Programmable auxiliary LED on and off times (allows blinking)
- I²C-compatible serial interface
- Interrupt line for signaling an external processor ($\overline{INT}$)
- Hard reset ($\overline{RST}$)
- Current limit protection
- Thermal overload protection
- Available in small 4.0 mm × 4.0 mm, 24-lead LFCSP package

APPLICATIONS

- Display backlight driver for phones that require slider or flip keypad functions with single or multiple LED indicators

TYPICAL OPERATING CIRCUIT

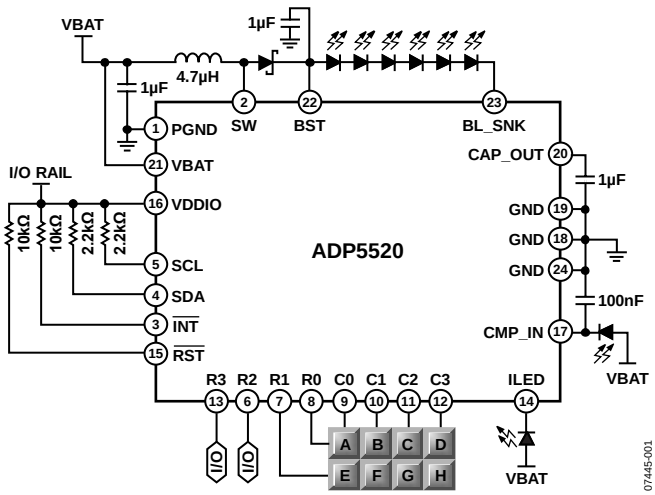

Figure 1.

GENERAL DESCRIPTION

The ADP5520 is a versatile single-chip, white LED backlight driver with a user configurable I/O expander. This device fits handset applications where the flip or slider section of the phone requires backlighting, I/O signaling and detecting, auxiliary LED lighting, and keypad functions. By incorporating an I²C-compatible serial interface and a single line interrupt, the ADP5520 significantly reduces the total number of lines required to interface with the baseband processor across the hinge flex.

The ADP5520 can detect ambient light levels and adjust the backlight brightness accordingly, resulting in extended battery operation.

Once configured, the ADP5520 is capable of controlling the flip/slider backlight intensity, on/off timing, dimming, and fading without the intervention of the main processor, which results in valuable battery power saving.

Rev. B

Document Feedback

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REVISION HISTORY

10/2017—Rev. A to Rev. B

Changed nINT, nRST, and nSTNBY to $\overline{\text{INT}}$, $\overline{\text{RST}}$, and $\overline{\text{STNBY}}$ ... Throughout
Change to Package Type Column, Table 4 ... 5
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Updated Outline Dimensions ... 38
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1/2010—Rev. 0 to Rev. A

Changes to Table 1 ... 3
Changes to Table 5 ... 6
Changes to Figure 32 ... 14
Updated Outline Dimensions ... 38
Changes to Ordering Guide ... 38

7/2008—Revision 0: Initial Version

SPECIFICATIONS

VBAT = 2.7 V to 4.8 V, T_J = −40°C to +125°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
VBAT Input Voltage Range	V_{BAT}		2.7		5.5	V
VDDIO Input Voltage Range	V_{VDDIO}		1.7		3.3[2]	V
Undervoltage Lockout Threshold	$UVLO_{VBAT}$	VBAT falling	1.7	2.1		V
	$UVLO_{VBAT}$	VBAT rising		2.4	2.7	V
	$UVLO_{VDDIO}$	VDDIO falling	1.1	1.3		V
	$UVLO_{VDDIO}$	VDDIO rising		1.4	1.62	V
SW leakage	$SW_{LEAKAGE}$			0.1	1	µA
SUPPLY CURRENT						
Shutdown Current[3]	I_{SD}	VDDIO = 0 V		0.1	1	µA
Standby Current[4]	I_{STNBY}	1.7 V ≤ VDDIO ≤ 3.3 V[2], $\overline{STNBY}$ = 0		25	45	µA
BACKLIGHT LED DRIVER (SW, BST)						
Current Limit (Peak Inductor Current)			450	600	750	mA
Switch On Resistance			100	200	400	mΩ
Overvoltage Limit			24.5	27	29.5	V
Boost Startup Time				1		ms
BACKLIGHT LED CURRENT SINK (BL_SNK)						
Full-Scale Backlight Current			26	30	32	mA
Backlight Current Ramp Rate		Fade timers disabled		0.3		mA/ms
AMBIENT LIGHT SENSOR (CMP_IN)						
Full-Scale Current	$BL_{FULLSCALE}$		0.7	1	1.2	mA
INPUT LOGIC LEVELS (SCL, SDA, $\overline{RST}$, C0, C1, C2, C3, R0, R1, R2, R3)[5]						
Logic Low Input Voltage	V_{IL}	1.7 V ≤ VDDIO ≤ 3.3 V[2]			0.3 × VDDIO	V
Logic High Input Voltage	V_{IH}	1.7 V ≤ VDDIO ≤ 3.3 V[2]	0.7 × VDDIO			V
Input Leakage Current	$V_{I-LEAKAGE}$	1.7 V ≤ VDDIO ≤ 3.3 V[2]		0.1	1	µA
INPUT LOGIC DEBOUNCE ($\overline{RST}$, C0, C1, C2, C3, R0, R1, R2, R3)[6]	$V_{IL-DBNC}$		50	75	100	µs
PUSH-PULL OUTPUT LOGIC LEVELS (C0, C1, C2, C3, R0, R1, R2, R3)[7]						
Logic Low Output Voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
Logic High Output Voltage	V_{OH}	I_{SOURCE} = 1 mA	VDDIO − 0.2			V
OPEN-DRAIN OUTPUT LOGIC LEVELS ($\overline{INT}$), SDA)						
Logic Low Output Voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
Logic High Leakage Current	$V_{OH-LEAKAGE}$	1.7 V ≤ VDDIO ≤ 3.3 V[2]		0.1	1	µA
AUX LED CURRENT SINK (ILED, C3, R3)[8]						
Leakage	$LED_{LEAKAGE}$	Sink disabled		0.1	1	µA
Full-scale Current Sink	$LED_{FULLSCALE}$	Applied pin voltage = 1 V	10.5	14	16.5	mA
GPIO PULL-UP RESISTANCE (C0, C1, C2, C3, R0, R1, R2, R3)[9]			50	65	80	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{HYS}	T_J falling		10		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Typical values are at T_A = 25°C, VBAT = 3.6 V.
[2] 3.3 V or VBAT, whichever is smaller.
[3] Internal LDO powered down, digital blocks inactive, I²C inactive, boost inactive.
[4] Internal LDO powered up, digital blocks active, I²C active, boost inactive.
[5] C0, C1, C2, C3, R0, R1, R2, and R3 are configured as digital inputs.
[6] C0, C1, C2, C3, R0, R1, R2, and R3 are configured as digital inputs, with debounce enabled.
[7] C0, C1, C2, C3, R0, R1, R2, and R3 are configured as digital outputs.
[8] C3 and R3 are configured as digital inputs with pull-up.
[9] C0, C1, C2, C3, R0, R1, R2, and R3 are configured as digital inputs with pull-up.

I²C TIMING SPECIFICATIONS

Table 2.

Parameter	Description	Min	Max	Unit
Delay from Reset Deassertion to I²C Access		60		µs
f_{SCL}	SCL clock frequency		400	kHz
t_{HIGH}	SCL high time	0.6		µs
t_{LOW}	SCL low time	1.3		µs
$t_{SU, DAT}$	Data setup time	100		ns
$t_{HD, DAT}$	Data hold time	0	0.9	µs
$t_{SU, STA}$	Setup time for repeated start	0.6		µs
$t_{HD, STA}$	Hold time for start/repeated start	0.6		µs
t_{BUF}	Bus free time for stop and start condition	1.3		µs
$t_{SU, STO}$	Setup time for stop condition	0.6		µs
t_R	Rise time for SCL and SDA	20 + 0.1 C_B	300	ns
t_F	Fall time for SCL and SDA	20 + 0.1 C_B	300	ns
t_{SP}	Pulse width of suppressed spike	0	50	µs
C_B[1]	Capacitive load for each bus line		400	pF

[1] C_B is the total capacitance of one bus line in picofarads.

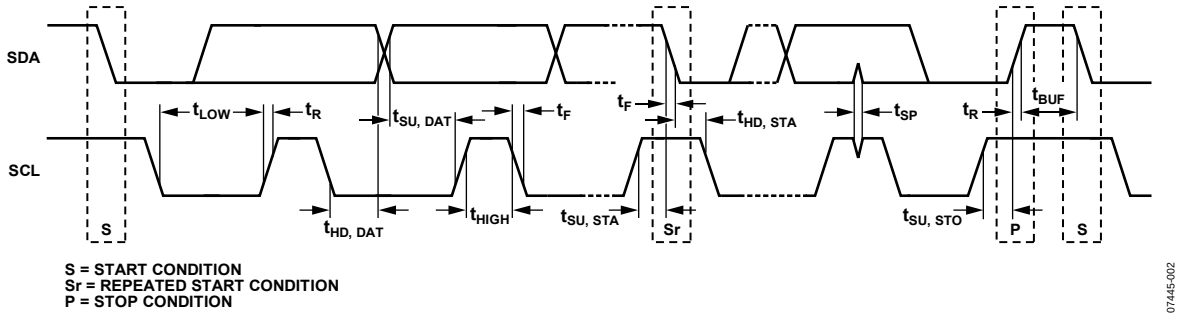

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VBAT to GND	−0.3 V to +6 V
VDDIO to GND	−0.3 V to VBAT
SW, BST to GND	−0.3 V to +30 V
ILED, R0, R1, R2, R3, C0, C1, C2, C3, CMP_IN, SCL, SDA, INT, RST, CAP_OUT, BL_SNK to GND	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Ambient Temperature Range	−40°C to +85°C[1]
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

[1] In applications where high power dissipation and poor thermal resistance are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependent on the maximum operating junction temperature ($T_{J(MAXOP)}$ = 125°C), the maximum power dissipation of the device ($PD_{(MAX)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), using the following equation: $T_{A(MAX)} = T_{J(MAXOP)} - (\theta_{JA} \times P_{D(MAX)})$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP (CP-24-14)	50	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

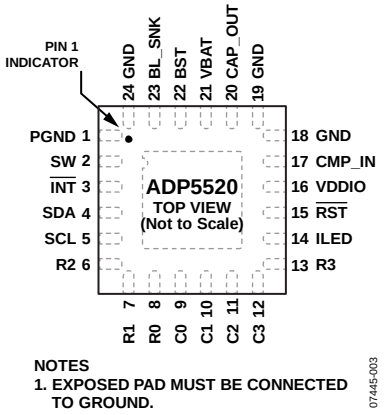

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PGND	Power Switch Output to Ground.
2	SW	Power Switch Input.
3	$\overline{\text{INT}}$	Processor Interrupt. This pin is active low, and open drain, Pull up to VDDIO.
4	SDA	I^2C-Compatible Serial Data Line. Open drain requires external pull-up to VDDIO.
5	SCL	I^2C-Compatible Serial Clock Line. Open drain requires external pull-up to VDDIO.
6	R2	Row 2 when configured in a keypad matrix, D2 when configured as an I/O.
7	R1	Row 1 when configured in a keypad matrix, D1 when configured as an I/O.
8	R0	Row 0 when configured in a keypad matrix, D0 when configured as an I/O.
9	C0	Column 0 when configured in a keypad matrix, D4 when configured as an I/O.
10	C1	Column 1 when configured in a keypad matrix, D5 when configured as an I/O.
11	C2	Column 2 when configured in a keypad matrix, D6 when configured as an I/O.
12	C3	Column 3 when configured in a keypad matrix, D7 when configured as an I/O, LED 2 when configured as a current sink.
13	R3	Row 3 when configured in a keypad matrix, D3 when configured as an I/O, LED 3 when configured as a current sink.
14	ILED	LED 1 Current Sink.
15	$\overline{\text{RST}}$	Reset Input, Active Low. This input signal resets the device to the power-up default conditions. Must be driven low for 75 µs (typical) to be valid.
16	VDDIO	Supply Voltage for the I/O Pins. Voltage is 1.7 V to 3.3 V (or VBAT, whichever is smaller). If VDDIO = 0, the device goes into full shutdown mode.
17	CMP_IN	Input for Ambient Light Sensing.
18	GND	Ground.
19	GND	Ground.
20	CAP_OUT	Capacitor for Internal 2.7 V LDO. A 1 µF capacitor must be connected between this pin and GND. Do not use this pin to supply external loads.
21	VBAT	Main Supply Voltage for the IC (2.7 V to 5.5 V).
22	BST	Overvoltage Monitor Input for the Boost Converter.
23	BL_SNK	Backlight Current Sink.
24	GND	Ground.
	EPAD	Exposed Pad. Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

VBAT = 3.6 V, T_A = 25°C, unless otherwise noted. Inductor = LPS4012-472MLB. Schottky rectifier = MBR140SFT1G.

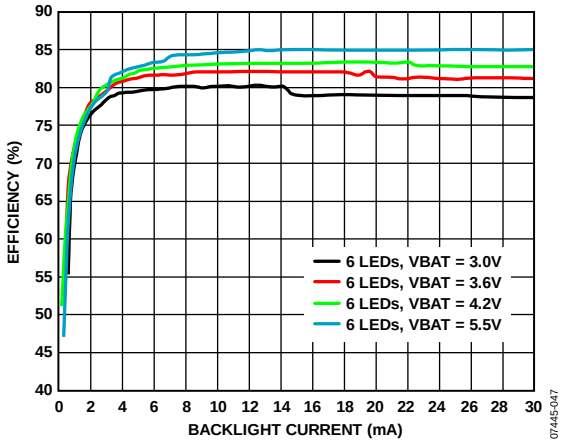

Figure 4. Efficiency vs. Backlight Current (6 LEDS)

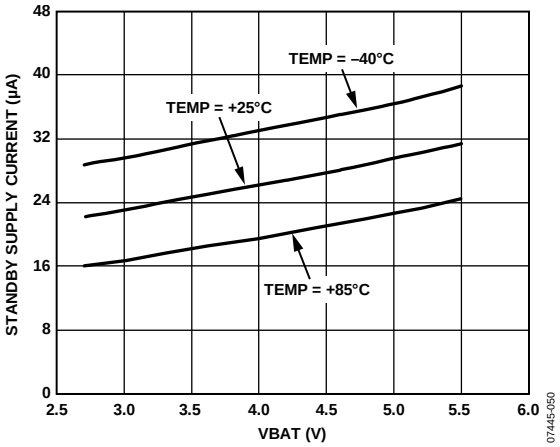

Figure 7. Standby Supply Current vs. VBAT

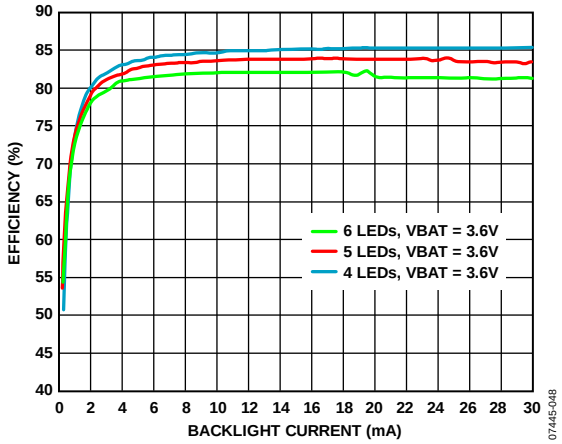

Figure 5. Efficiency vs. Backlight Current (4, 5, and 6 LEDS)

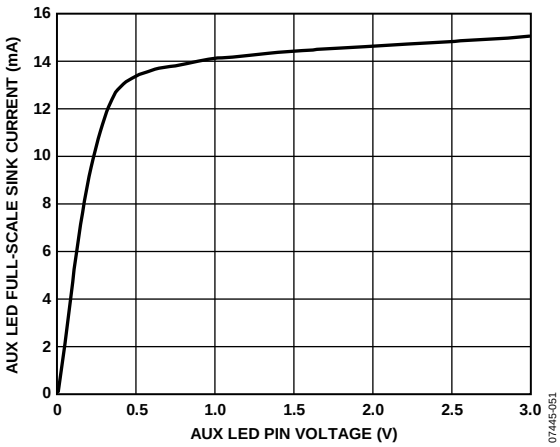

Figure 8. Typical Auxiliary LED Pin (R3, C3, or ILED), Full-Scale Sink Current vs. Applied Pin Voltage

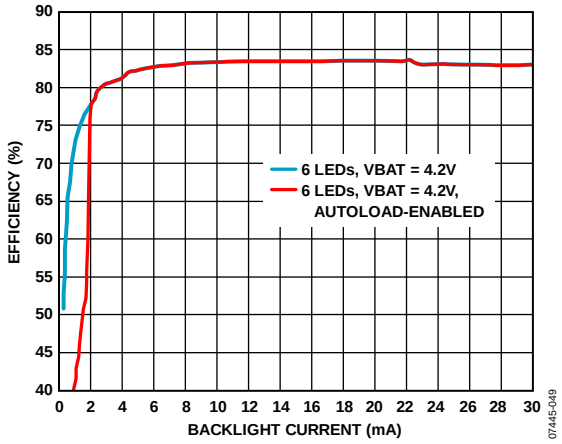

Figure 6. Efficiency vs. Backlight Current (Autoload On/Off)

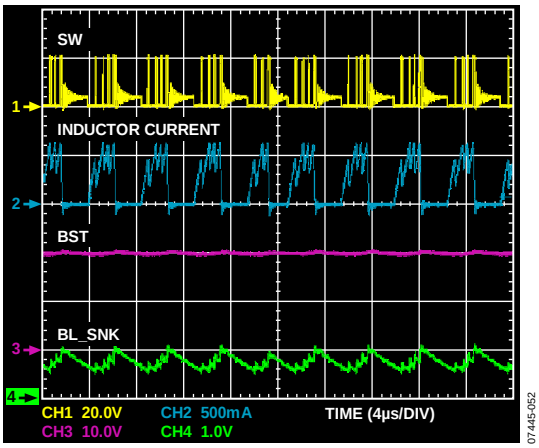

Figure 9. Boost Operation (Backlight = 30 mA)

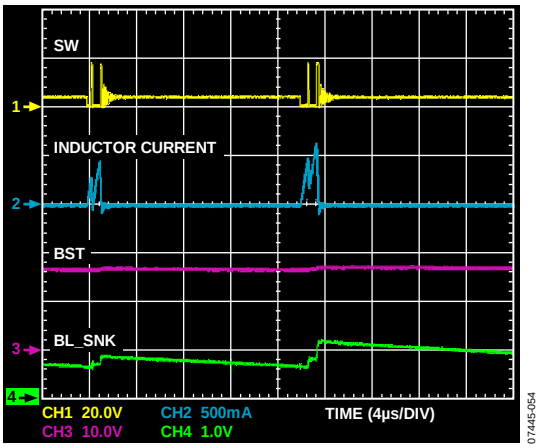

Figure 11. Boost Operation (Backlight = 2 mA)

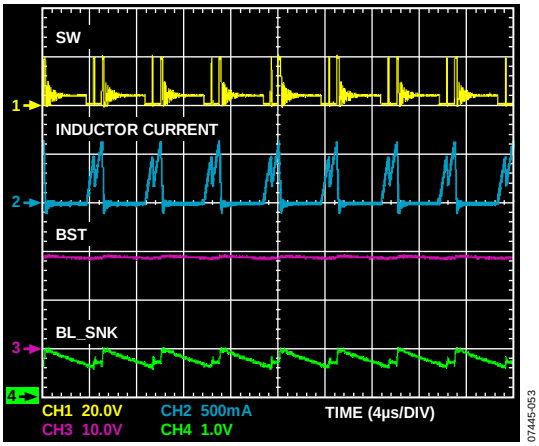

Figure 10. Boost Operation (Backlight = 15 mA)

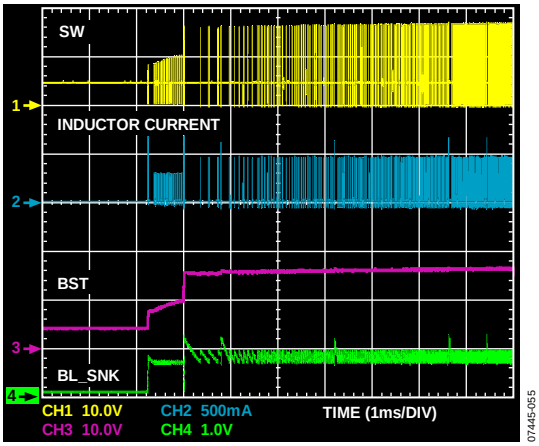

Figure 12. Boost Startup

THEORY OF OPERATION

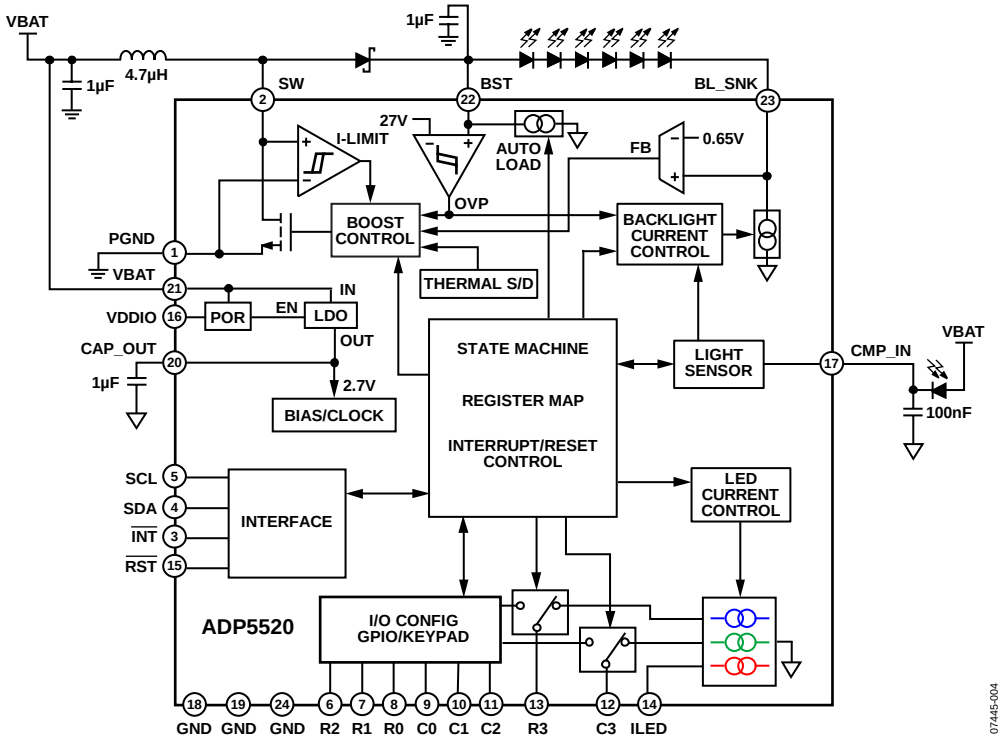

Figure 13. Internal Block Diagram

The ADP5520 is a backlight white LED driver with an I/O port expander. It is ideal for cell phone designs and other portable devices, where keypad and/or extended I/O functionality is needed. Programmable fade-in, fade-out, dim, and off timers provide the backlight with flexible control features. Using an external photodiode, the ADP5520 can perform ambient light sensing, and adjust the backlight brightness according to varying lighting conditions.

The I/O port expander has eight configurable GPIO pins. The I/Os can be configured as a keypad matrix, digital inputs, or digital outputs. Additionally, two of the I/Os (R3 and C3) can be configured as current sink lines and, paired with a dedicated sink line (ILED), can be used to drive up to three auxiliary LEDs. Programmable fading is also available for auxiliary LEDs.

Once programmed through its I²C-compatible interface, the ADP5520 can run autonomously. An interrupt line ($\overline{\text{INT}}$) is available to alert an external microprocessor of the status of its I/Os, keypad presses and releases, ambient light sensor comparator states, and overvoltage conditions.

BACKLIGHT DRIVE AND CONTROL

White LEDs are common in backlighting the displays of modern portable devices such as cell phones. White LEDs require a high forward voltage, V_F, before they conduct current and emit light. Display panels, depending on their size, can be backlit with single or multiple white LEDs. In panels that require multiple LEDs, the LEDs are commonly connected in a series string to achieve uniform brightness in each LED by passing a common current through all of them. The LED string needs to be biased with a voltage greater than the sum of the V_F of each LED before it conducts.

The ADP5520 is an asynchronous boost converter capable of driving an LED string with 24.5 V (minimum). For detailed information about the boost device, see the Applications Information section. With sufficient forward voltage created, the ADP5520 controls the current (and thus the brightness) of the LED string via an adjustable internal current sink. An internal state machine, in conjunction with programmable timers, dynamically adjusts the current sink between 0 mA and 30 mA to achieve impressive backlight control features.

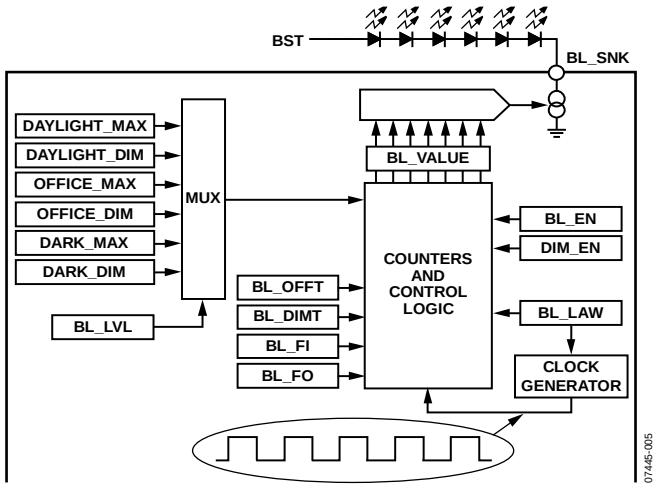

Figure 14. Backlight Brightness Control

BACKLIGHT OPERATING LEVELS

Backlight brightness control can operate in three distinct levels: daylight (L1), office (L2), and dark (L3). The BL_LVL bits in Register 0x02 control the level in which the backlight operates. The BL_LVL bits can be changed manually, or if in automatic mode, by the ambient light sensor (see the Ambient Light Sensing section). By default, the backlight operates at daylight level (BL_LVL = 00), where the maximum brightness is set using Register 0x05 (DAYLIGHT_MAX). A daylight dim setting can also be set using Register 0x06 (DAYLIGHT_DIM). When operating at office level (BL_LVL = 01), the backlight maximum and dim brightness settings are set by Register 0x07 (OFFICE_MAX) and Register 0x08 (OFFICE_DIM). When operating at dark level (BL_LVL = 10), the backlight maximum and dim brightness settings are set by Register 0x09 (DARK_MAX) and Register 0x0A (DARK_DIM).

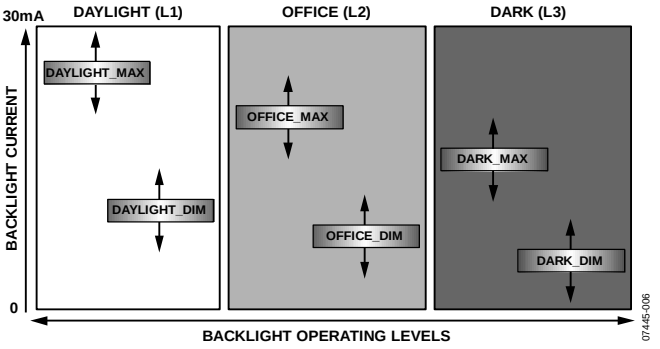

Figure 15. Backlight Operating Levels

BACKLIGHT MAXIMUM AND DIM SETTINGS

The backlight maximum and dim current settings are determined by a 7-bit code programmed by the user into the registers listed in the Backlight Operating Levels section. This 7-bit resolution allows the user to set the backlight to 1 of 128 different levels between 0 mA and 30 mA. The ADP5520 can implement two distinct algorithms to achieve a linear and a nonlinear relationship between input code and backlight current. The BL_LAW bits in Register 0x02 are used to swap between algorithms.

By default, the ADP5520 uses a linear algorithm (BL_LAW = 00), where backlight current increases linearly for a corresponding increase of input code. Backlight current (in mA) is determined by the following equation:

$$Backlight\ Current = Code \times (Fullscale\_Current/127) \quad (1)$$

where:
Code is the input code programmed by the user.
Fullscale_Current is the maximum sink current allowed (typically 30 mA).

The ADP5520 can also implement a nonlinear (square approximation) relationship between input code and backlight current level. In this case (BL_LAW = 01), the backlight current (in mA) is determined by the following equation:

$$Backlight\ Current = \left(Code \times \frac{\sqrt{Fullscale\_Current}}{127} \right)^2 \quad (2)$$

Figure 16 shows the backlight current level vs. input code for both the linear and square law algorithms.

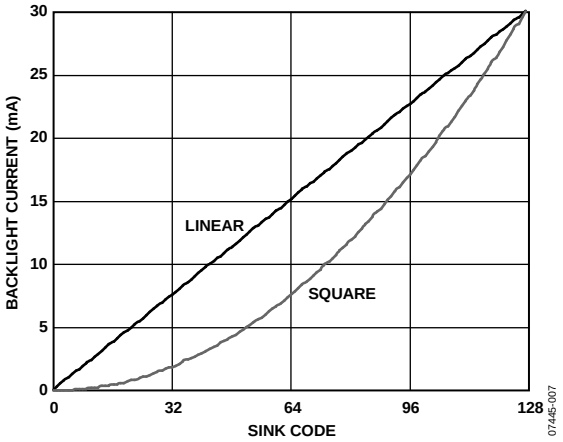

Figure 16. Backlight Current vs. Sink Code

BACKLIGHT TURN ON/OFF/DIM

With the device in operating mode ($\overline{STNBY}$ = 1), the backlight can be turned on using the BL_EN bit in Register 0x00. Before turning on the backlight, choose which level (daylight (L1), office (L2), or dark (L3)) to operate in, and ensure that maximum and dim settings are programmed for that level. The backlight turns on when BL_EN = 1. The backlight turns off when BL_EN = 0.

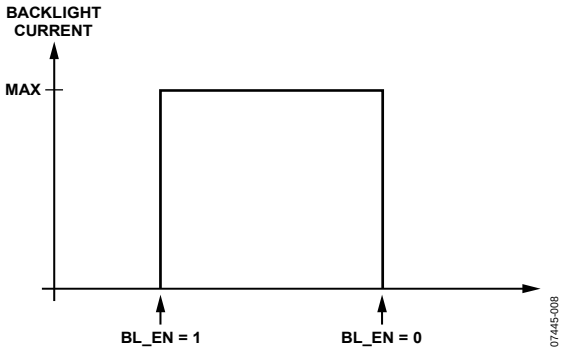

Figure 17. Backlight Turn On/Off

While the backlight is on (BL_EN = 1), the user can make it change to a dim setting by programming DIM_EN = 1 in Register 0x00. If DIM_EN = 0, the backlight reverts to its maximum setting.

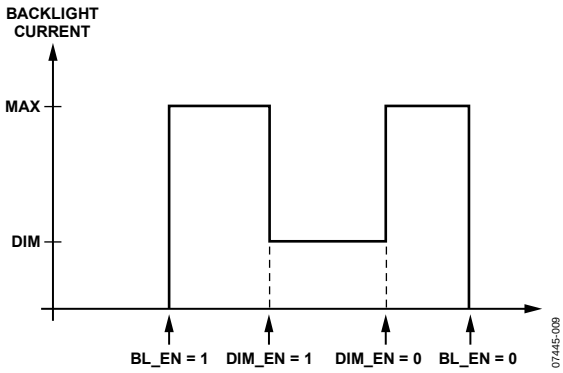

Figure 18. Backlight Turn On/Dim/Off

The maximum and dim settings can be set between 0 mA and 30 mA; therefore, it is possible to program a dim setting that is greater than a maximum setting. For normal expected operation, ensure that the dim setting is programmed to be less than the maximum setting.

It is also possible to activate the backlight automatically when a key press is detected. With the row and column pins configured as a keypad matrix, and the KP_BL_EN bit asserted in Register 0x02, the internal state machine asserts BL_EN and turns on the backlight if a key is pressed. See the I/O Expansion Pins (Keypad Matrix) section for more information on using keypad functionality.

AUTOMATIC DIM AND TURN OFF TIMERS

The user can program the backlight to dim automatically by using the BL_DIMT timer in Register 0x03. The dim timer has 15 settings ranging from 10 sec to 2 min. Program the dim timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting, and the dim timer starts counting. When the dim timer expires, the internal state machine sets DIM_EN = 1, and the backlight goes to its dim setting.

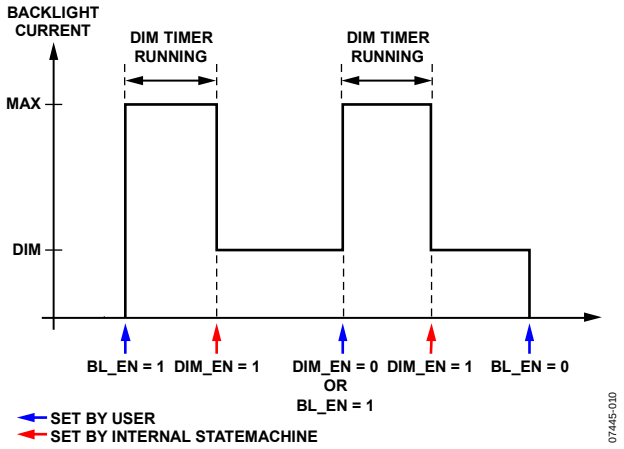

Figure 19. Dim Timer

If the user clears the DIM_EN bit (or reasserts the BL_EN bit), the backlight reverts to its maximum setting and the dim timer begins counting again. When the dim timer expires, the internal state machine again sets DIM_EN = 1, and the backlight goes to its dim setting. Reasserting BL_EN at any point during the dim timer countdown causes the timer to reset and begin counting again. The backlight can be turned off at any point during the dim timer countdown by clearing BL_EN.

The user can also program the backlight to turn off automatically by using the BL_OFFT timer in Register 0x03. The off timer has 15 settings ranging from 10 sec to 2 min. Program the off timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting, and the off timer starts counting. When the off timer expires, the internal state machine clears the BL_EN bit, and the backlight turns off.

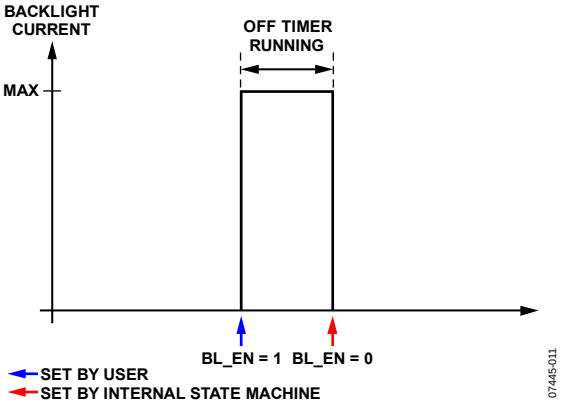

Figure 20. Off Timer

Reasserting BL_EN at any point during the off timer countdown causes the timer to reset and begin counting again. The backlight can be turned off at any point during the off timer countdown by clearing BL_EN.

The dim timer and off timer can be used together for sequential maximum-to-dim-to-off functionality. With both the dim and off timers programmed, if BL_EN is asserted, the backlight turns on to its maximum setting. When the dim timer expires, the backlight changes to its dim setting. When the off timer expires, the backlight turns off.

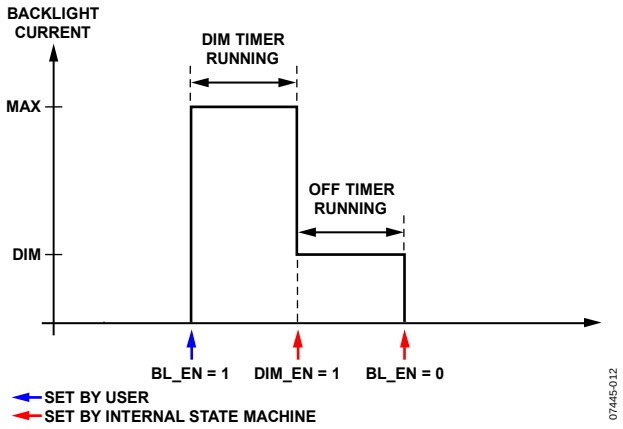

Figure 21. Dim and Off Timers Used Together

LINEAR BACKLIGHT FADE IN AND FADE OUT

To counteract the abrupt visual effect of near instant turn-on and turn-off of the backlight, the ADP5520 contains timers to facilitate the smooth fading between off, on, and dim states. By default (BL_LAW = 00), the ADP5520 implements a fading scheme using the linear backlight code algorithm (see Equation 1).

The BL_FI timer in Register 0x04 can be used for smooth fade-in transitions from low to high backlight settings, such as off-to-dim, off-to-maximum, and dim-to-maximum. The BL_FI timer can be programmed to one of 15 settings ranging from 0.3 sec to 5.5 sec. Program the BL_FI timer before asserting BL_EN.

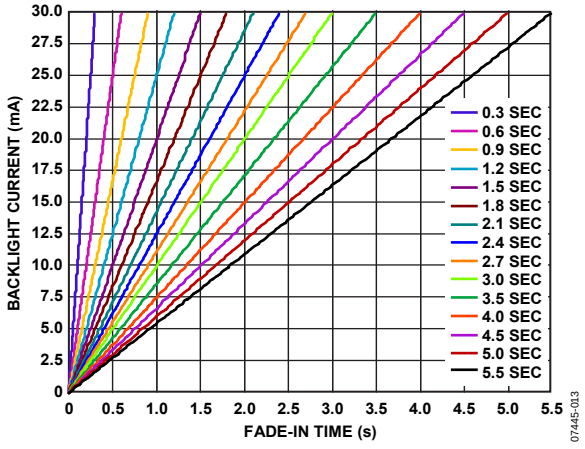

Figure 22. Linear Fade-In Times

The time programmed in BL_FI represents the time it takes the backlight current to go from 0 mA to 30 mA. Fading between intermediate settings is shorter.

The BL_FO timer in Register 0x04 can be used for smooth fade-out transitions from high to low backlight settings such as maximum-to-dim and dim-to-off. The BL_FO timer can be programmed to one of 15 settings ranging from 0.3 sec to 5.5 sec. Program the BL_FO timer before asserting BL_EN.

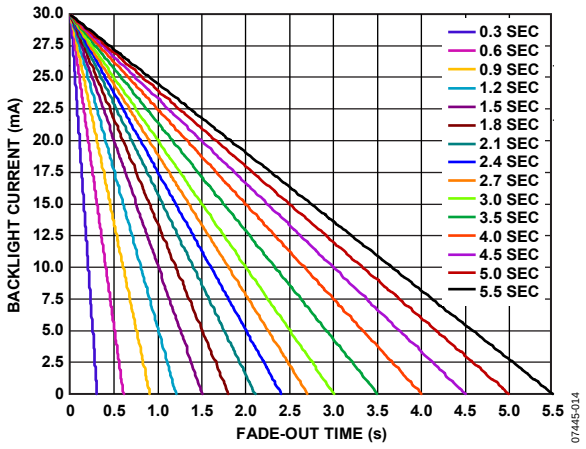

Figure 23. Linear Fade-out Times

The time programmed in BL_FO represents the time it takes the backlight current to go from 30 mA to 0 mA. Fading between intermediate settings is shorter.

Figure 24 shows the fade timers in use. With BL_FI and BL_FO programmed, if BL_EN is asserted, then the backlight fades in to its maximum setting. If DIM_EN is asserted, then the backlight fades out to its dim setting. If BL_EN is cleared, the backlight fades out to off.

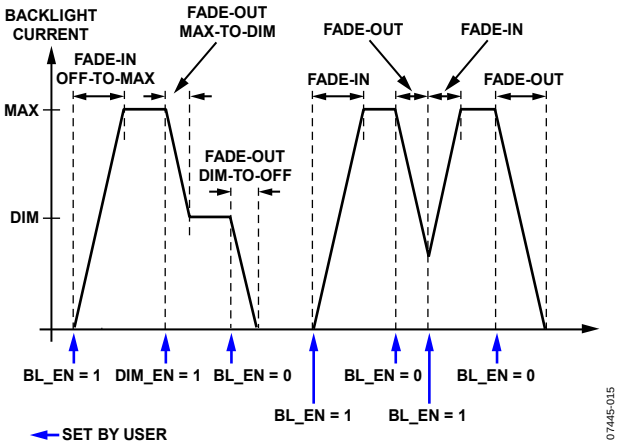

Figure 24. Backlight Turn On/Off/Dim with Fade Timers

During any point in a fade-out, if BL_EN is asserted, then the backlight stops at its current fade-out position and begins fading in.

The fade-in and fade-out timers can be used independently of each other, that is, fade-in can be enabled while fade-out is disabled. The fade timers can also be used with the off and dim timers.

Figure 25 shows the fade timers used with the dim and off timers.

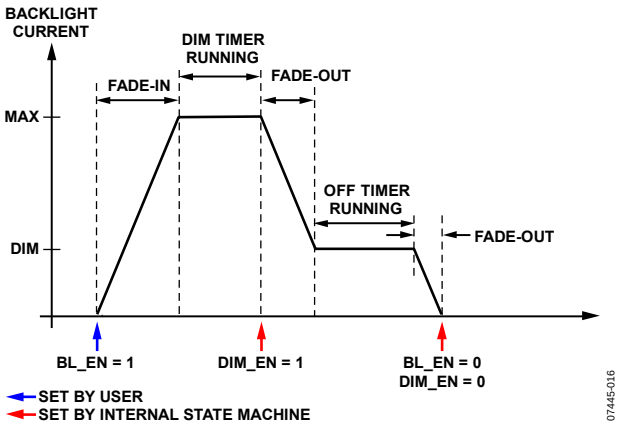

Figure 25. Fade/Dim/Off Timers Used Together

FADE OVERRIDE

A fade override feature allows the BL_FI and BL_FO timers to be overridden if the BL_EN bit is reasserted (either by the user or due to a key press) during a fade-in or fade-out period, and sets the backlight to its maximum setting. Fade override can be activated by setting the FOVR bit in Register 0x02.

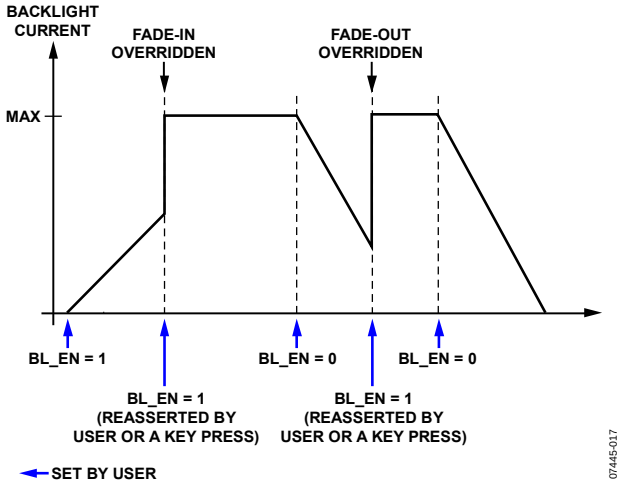

Figure 26. Fade Override

ADVANCED FADING (SQUARE)

Although the default linear fade algorithm gives a smooth increase and decrease in backlight current, the resulting increase and decrease in brightness still appears visually abrupt. For example, for a given fade-in time, the eye can notice an initial increase in brightness as backlight current is increased, but cannot perceive much more of an increase in brightness as backlight current is increased to maximum.

The reason for this is that the eye, like all human senses, perceives changes in light when the brightness of the light source is changed logarithmically (Weber-Fechner law). To achieve a more natural fading experience to the user, the fade timers can be used in conjunction with the square law approximation backlight codes (see Equation 2) by setting BL_LAW = 01.

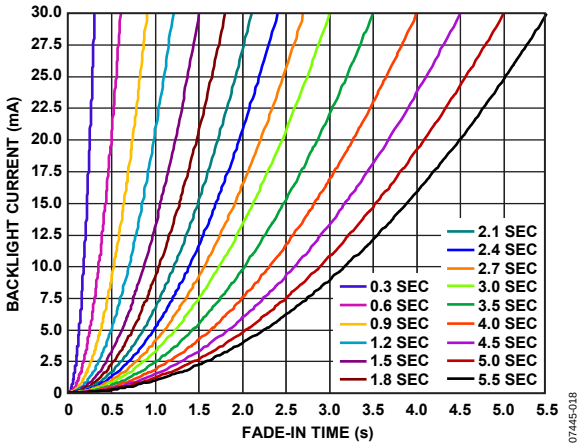

Figure 27. Square Law Fade-In Times

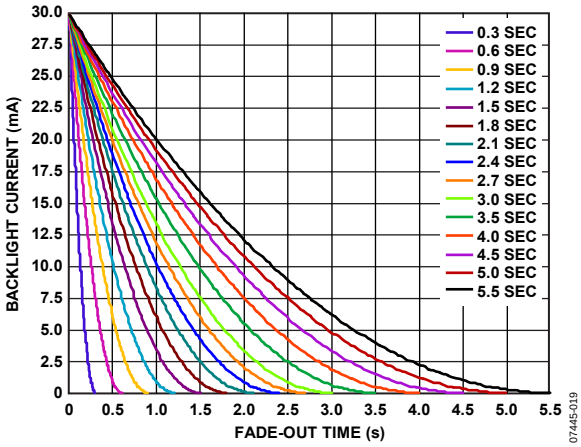

Figure 28. Square Law Fade-Out Times

ADVANCED FADING (CUBIC 1 AND CUBIC 2)

Two additional advanced techniques are available for fading the backlight brightness levels, Cubic 1 (BL_LAW = 10) and Cubic 2 (BL_LAW = 11). Referring to the backlight brightness control block diagram shown in Figure 14, linear and square fading is implemented by ramping the 128 linear/square algorithm codes at a fixed frequency over the duration of a given fade-in/fade-out time.

Cubic fading is implemented by reusing the square algorithm codes, but by ramping them with a clock source whose frequency output increases as the sink current code increases (see Figure 29). Cubic 1 and Cubic 2 differ by having separate frequency vs. code characteristics.

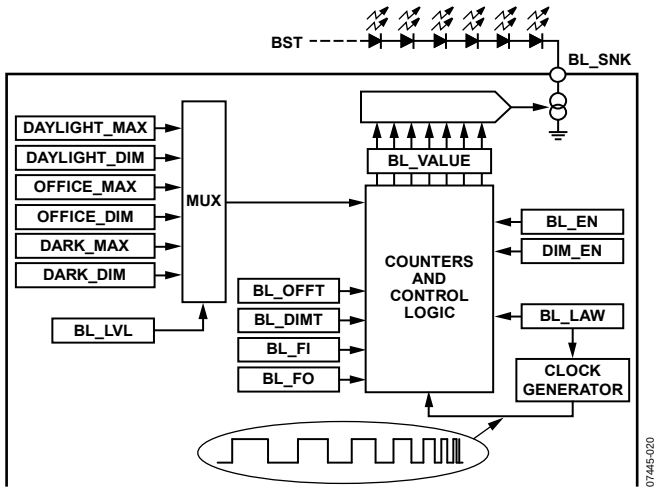

Figure 29. Backlight Brightness Control (Cubic)

Figure 30 shows a comparison of fade law techniques. Cubic fades complete faster than linear or square fades for a given fade time setting. Cubic 1 completes approximately 30% faster, and Cubic 2 completes approximately 10% faster than an equivalent linear or square fade time.

With four fade laws and 15 fade time settings, users have tremendous flexibility to find the right fade experience for their application.

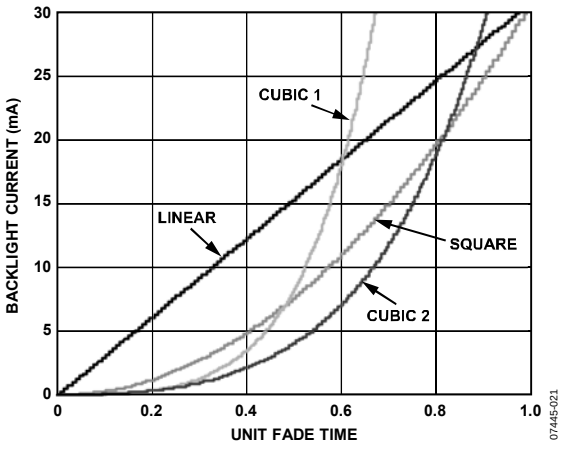

Figure 30. Fade Law Comparison Over a Unit Fade Time

AMBIENT LIGHT SENSING

The ADP5520 can be used in conjunction with an external photosensor to detect when ambient light conditions have dropped below programmable set points. An ADC samples the output of the external photosensor. The ADC result is fed into two programmable trip comparators. The ADC has an input range of 0 µA to 1000 µA (typical).

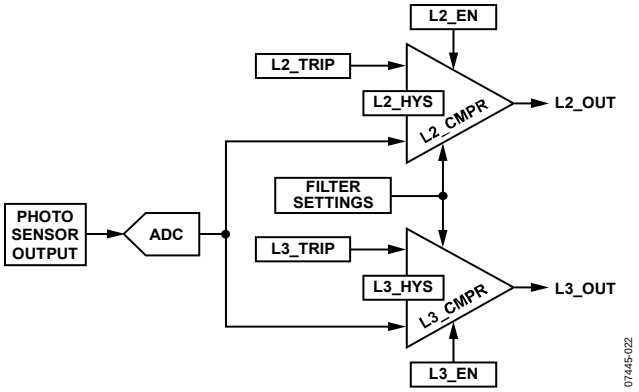

Figure 31. Ambient Light Sensing and Trip Comparators

The Level 2 (office) light sensor comparator, L2_CMPR, is used to detect when the photosensor output has dropped below the programmable L2_TRIP point. If this event occurs, the L2_OUT status signal is set. L2_CMPR contains programmable hysteresis, meaning that the photosensor output must rise above L2_TRIP + L2_HYS before L2_OUT is cleared. L2_CMPR is enabled in Register 0x0C via the L2_EN bit. The L2_TRIP and L2_HYS values of L2_CMPR can be set between 0 µA and 1000 µA (typical) in steps of 4 µA (typical).

L3_CMPR is used to detect when the photosensor output has dropped below the programmable L3_TRIP point. If this event occurs, the L3_OUT status signal is set. L3_CMPR contains programmable hysteresis, meaning that the photosensor output must rise above L3_TRIP + L3_HYS before L3_OUT is cleared. L3_CMPR is enabled in Register 0x0C via the L3_EN bit. The L3_TRIP and L3_HYS values of L3_CMPR can be set between 0 µA and 127 µA (typical) in steps of 0.5 µA (typical).

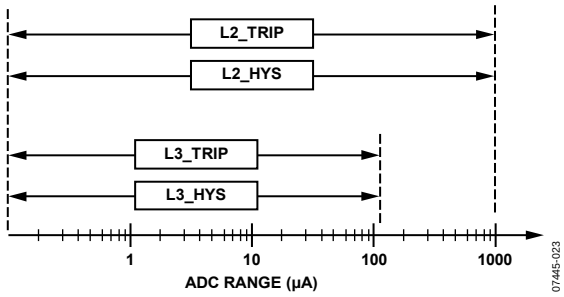

Figure 32. Comparator Ranges

The L2_CMPR and L3_CMPR comparators can be enabled independently of each other. The ADC and comparators run continuously when L2_EN and/or L3_EN are set, during automatic backlight adjustment mode. A single conversion

takes 80 ms (typical). Filter times of between 80 ms and 10 sec can be programmed for the comparators before they change state.

It is also possible to use the light sensor comparators in a single shot mode. After the single shot measurement is completed, the internal state machine clears the FORCE_RD bit.

The interrupt flag, CMPR_INT, is set in Register 0x00 if either of the L2_OUT or L3_OUT status bits change state, meaning interrupts can be generated if ambient light conditions transition between any of the programmed trip points. CMPR_INT can cause the $\overline{\text{INT}}$ pin to be asserted if the CMPR_IEN bit is set in Register 0x00. The CMPR_INT flag can be cleared only by writing a 1 to it.

AUTOMATIC BACKLIGHT ADJUSTMENT

The ambient light sensor comparators can be used to automatically transition the backlight between one of its three operating levels. To enable this mode, the BL_AUTO_ADJ bit is set in Register 0x02.

Once enabled, the internal state machine takes control of the BL_LVL bits and changes them based on the L2_OUT and L3_OUT status bits. The L2_OUT status bit indicates that ambient light conditions have dropped below the L2_TRIP point and the backlight must be moved to its office (L2) level. The L3_OUT status bit indicates that ambient light conditions have dropped below the L3_TRIP point and the backlight must be moved to its dark (L3) level. Table 6 shows the relationship between backlight operation and the ambient light sensor comparator outputs.

The L3_OUT status bit has greater priority, so the backlight operates at L3 (dark) even if L2_OUT is set.

Table 6. Comparator Output Truth Table (X = Don't Care)

BL_AUTO_ADJ	L3_OUT	L2_OUT	Backlight Operation
0	X	X	BL_LVL can be manually set by the user
1	0	0	BL_LVL = 00, backlight operates at L1 (daylight)
1	0	1	BL_LVL = 01, backlight operates at L2 (office)
1	1	0	BL_LVL = 10, backlight operates at L3 (dark)
1	1	1	BL_LVL = 10, backlight operates at L3 (dark)

I/O EXPANSION PINS (GPIOs)

The eight I/O expansion pins (R0, R1, R2, R3, C0, C1, C2, and C3) can be configured as general-purpose digital inputs, digital inputs with pull-up, or digital outputs. Two of the I/O pins (R3 and C3) are LED current sinks by default. To use them as GPIOs, set Bit 4 and Bit 5 in Register 0x11. Register 0x17 to Register 0x1F are used to configure the I/O pins in GPIO mode. Figure 33 shows the typical makeup of a GPIO block, where Rx/Cx represents any one of the eight I/O lines.

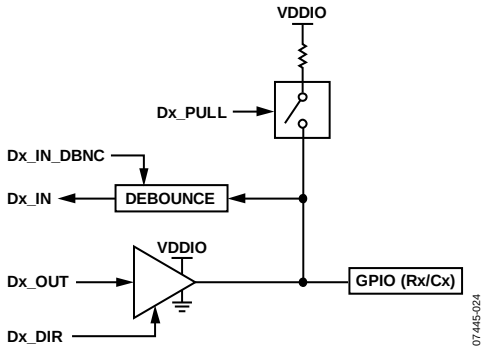

Figure 33. Typical GPIO Block

When configured as an output, a digital buffer drives the GPIO Rx and Cx pins to 0 V for a Logic 0 and to the VDDIO rail for a Logic 1. Output data for each I/O is set using Register 0x1A.

Each I/O has a pull-up resistor that can be enabled when used as an input. This can be useful for interfacing to an external signal that has only pull-down capabilities. Pull-ups can be enabled and disabled using Register 0x1F.

Each I/O has a debounce circuit that effectively filters out glitches and pulses less than 75 µs (typical) to prevent false triggering when configured as an input. By default, debounce is enabled but can be disabled using Register 0x1E.

I/Os configured as inputs store the digital state sensed at each pin in Register 0x19. Interrupts can be generated by digital inputs if enabled in Register 0x1B. The input interrupt level can be selected using Register 0x1D. Interrupts generated are stored in Register 0x1C. The master GPI_INT bit is set if any interrupt bits are set in Register 0x1C, and the $\overline{\text{INT}}$ pin is asserted.

To deassert the $\overline{\text{INT}}$ pin and clear the GPI_INT bit, the 0x1C register must be cleared by reading it twice (assuming the interrupt condition has gone away), and then a 1 must be written to the GPI_INT bit in Register 0x00. Figure 34 shows the interrupt generation scheme, where Dx represents any one of the eight digital input lines.

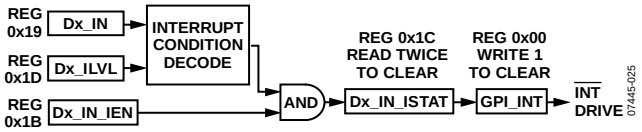

Figure 34. GPIO Interrupt generation

I/O EXPANSION PINS (KEYPAD MATRIX)

The eight I/O expansion pins (R0, R1, R2, R3, C0, C1, C2, and C3) can be configured to decode a keypad matrix, consisting of up to 16 switches (4 × 4 matrix). See the Example Circuits section for other possible matrix configurations.

Two of the I/O pins (R3 and C3) are LED current sinks by default. To use them as keypad decoders, set Bit 4 and Bit 5 in Register 0x11. The R0, R1, R2, and R3 I/O pins make up the rows of the keypad matrix. The C0, C1, C2, and C3 I/O pins make up the columns of the keypad matrix.

To configure the device for key scanning and decoding, the R0, R1, R2, and R3 pull-ups must be enabled in Register 0x1F. Key scanning and decoding is then enabled by programming the row and column bits in Register 0x17. The row pull-ups must be enabled before enabling key scanning.

Figure 35 shows the row and column pins connected to a typical 4 × 4, 16-switch keypad matrix. When key scanning is idle, the row pins are pulled high and the column pins are pulled low. The key scanner operates by checking if the row pins are low. If the A button in the matrix is pressed, the switch connects R0 to C0. The key scan circuit senses that the R0 pin has been pulled low and begins a key scan cycle. To prevent glitches or narrow press times registering as valid key presses, the key scanner requires the key to be pressed for two scan cycles. The key scanner has a sampling period of 25 ms, so the key must be pressed and held for at least 25 ms to register as being pressed. If the key is continuously pressed, the key scanner continues to sample every 25 ms.

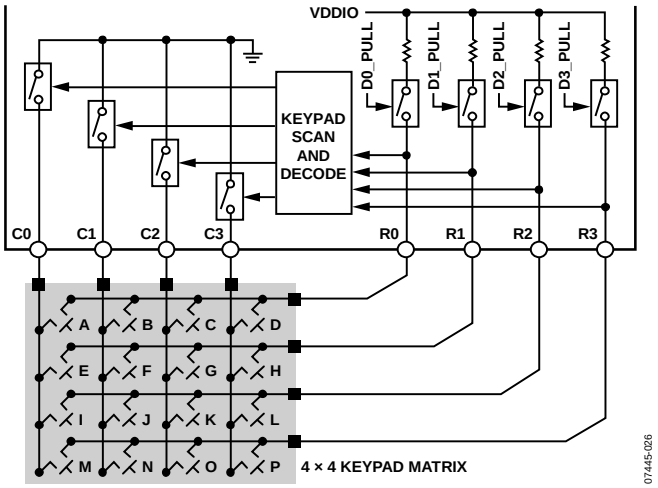

Figure 35. Keypad Decode Configuration

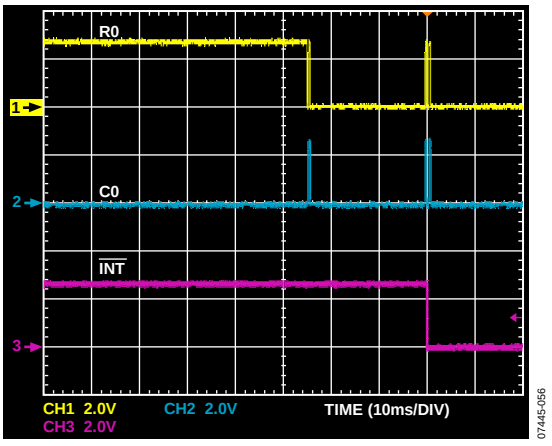

Figure 36. Key Press(R0,C0)

If the A button is released, the switch opens the connection between R0 and C0, and R0 is pulled up high. The key scanner requires that the key be released for two scan cycles. Because the release of a key is not necessarily in sync with the key scanning sampling period, it may take between 25 ms and 50 ms for a key to register as being released. Once the key is registered as being released, the key scanner returns to idle mode.

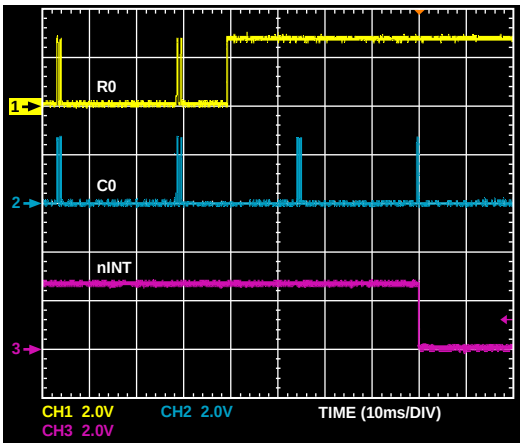

Figure 37. Key Press (R0, C0)

Key press/release status and interrupt information is recorded in Register 0x20 through Register 0x25. When a key is pressed, an interrupt is generated and stored. Key press interrupts for A through H are stored in Register 0x20, and key press interrupts for I through P are stored in Register 0x21. The master KP_INT flag is set if any interrupt bits are set in Register 0x20 or Register 0x21. The $\overline{\text{INT}}$ pin is asserted if KP_INT is set and if KP_IEN is enabled in Register 0x01.

To deassert the $\overline{\text{INT}}$ pin and clear the KP_INT flag, Register 0x20 and Register 0x21 must be cleared by reading them once, and then a 1 must be written to the KP_INT bit in Register 0x00. Figure 38 shows the interrupt generation scheme, where KP_x_ISTAT represents any one of the 16 key press interrupt status bits.

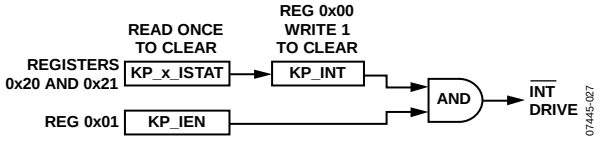

Figure 38. Key Press Interrupt Generation

It is possible to clear key press interrupts (KP_INT = 1) and deassert $\overline{\text{INT}}$ while a key is still pressed.

When a key is released, an interrupt is also generated and stored. Key release interrupts for A through H are stored in Register 0x22, and key release interrupts for I through P are stored in Register 0x23. The master KR_INT flag is set if any interrupt bits are set in Register 0x22 or Register 0x23. The $\overline{\text{INT}}$ pin is asserted if KR_INT is set and if KR_IEN is enabled in Register 0x01.

To deassert the $\overline{\text{INT}}$ pin and clear the KR_INT flag, Register 0x22 and Register 0x23 must be cleared by reading them once, and then a 1 must be written to the KR_INT bit in Register 0x00. Figure 39 shows the interrupt generation scheme, where KR_x_ISTAT represents any one of the 16-key release interrupt status bits.

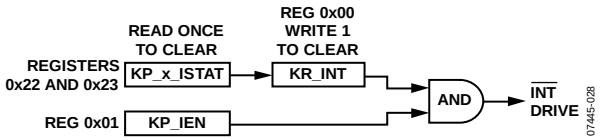

Figure 39. Key Release Interrupt Generation

The backlight can be programmed to turn on as a consequence of a key press, using the KP_BL_EN bit in Register 0x02. To enable this feature, observe the following sequence:

1. Enable the row pull-ups using Register 0x1F.
2. Enable key scanning on rows and columns using Register 0x17.
3. Enable backlight turn-on due to key press by setting KP_BL_EN in Register 0x02.
4. Set device to operating mode ($\overline{\text{STNBY}}$ = 1) in Register 0x00.

When a key is pressed, the backlight turns on. If the off timer is programmed, the backlight turns off, or the user can turn off the backlight by clearing BL_EN.

If the user wants the backlight to turn on again with a subsequent key press, the KP_INT and KR_INT bits in Register 0x00 must be cleared.

I/O EXPANSION PINS AND ILED PIN (AUXILIARY LED CURRENT SINKS)

The ILED pin and two of the I/O expansion pins (R3 and C3) can be used as auxiliary LED current sinks. Each LED current sink is programmable up to 14 mA (typical) and can be independently turned on and off.

The ILED pin is the current sink for LED 1. Its sink current can be set using LED1_CURRENT in Register 0x14. The LED 1 sink can be enabled with LED1_EN in Register 0x11.

The C3 pin is the current sink for LED 2. Its sink current can be set using LED2_CURRENT in Register 0x15. The LED 2 sink can be enabled with LED2_EN in Register 0x11.

The R3 pin is the current sink for LED 3. Its sink current can be set using LED3_CURRENT in Register 0x16. The LED 3 sink can be enabled with LED3_EN in Register 0x11.

The LEDx_CURRENT registers are six bits wide, allowing the user to set the LED sink current to one of 64 different levels between 0 mA and 14 mA. The ADP5520 can implement two distinct algorithms, to achieve a linear and a nonlinear relationship between input code and sink current.

By default, the ADP5520 uses a linear algorithm (LED_LAW = 0), where the LED sink current increases linearly for a corresponding increase of input code. LED sink current (in milliamps) is determined by the following equation:

$$LED\ Sink\ Current = Code \times (Fullscale\_Current/63) \quad (3)$$

where:
Code is the input code programmed by the user.
Fullscale_Current is the maximum sink current allowed (typically 14 mA).

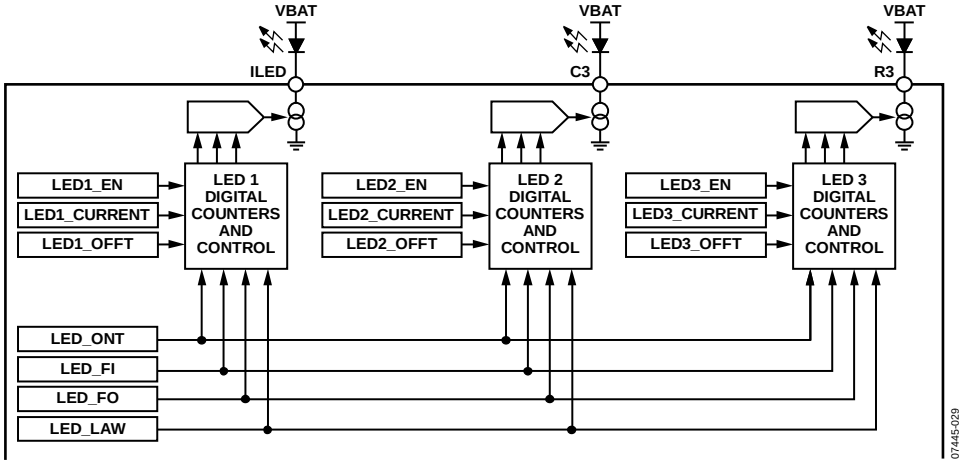

Figure 40. LED Current Sinks

The ADP5520 can also implement a nonlinear (square approximation) relationship between input code and LED sink current level. In this case (LED_LAW = 1), the LED sink current (in milliamps) is determined by the following equation:

$$LED\ Sink\ Current = \left(Code \times \frac{\sqrt{Fullscale\_Current}}{63} \right)^2 \quad (4)$$

Figure 41 shows the auxiliary LED sink current levels vs. input code for both the linear and square law algorithms.

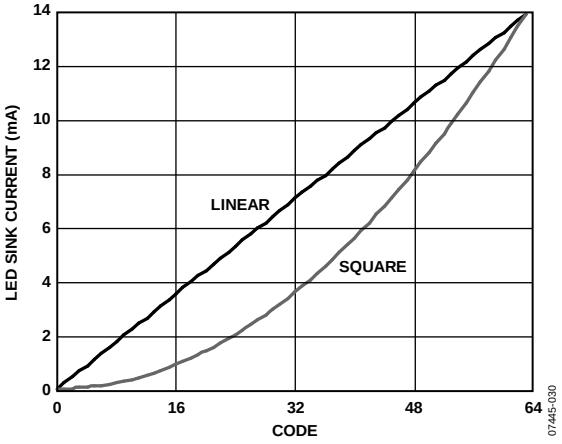

Figure 41. LED Sink Current vs. Code

Similar to the backlight current sink, the ADP5520 contains timers to facilitate the smooth fading between off and on states of the LED current sinks. All three LED sinks share a common fade-in (LED_FI) timer as well as a common fade-out (LED_FO) timer. The fade-in and fade-out timers are located in Register 0x13, and can be programmed to one of 15 settings ranging from 0.3 sec to 5.5 sec. Fade-in times represent the time it takes to fade from 0 mA to 14 mA. Fade-out times represent the time it takes to fade from 14 mA to 0 mA. Fading between intermediate settings is shorter. Program the fade timers before asserting LEDx_EN.

By default (LED_LAW = 0), the ADP5520 implements a fading scheme using the linear algorithm (see Equation 3).

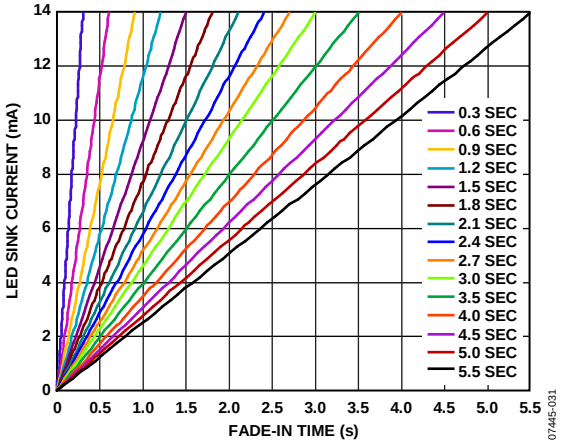

Figure 42. Linear Fade-In Times

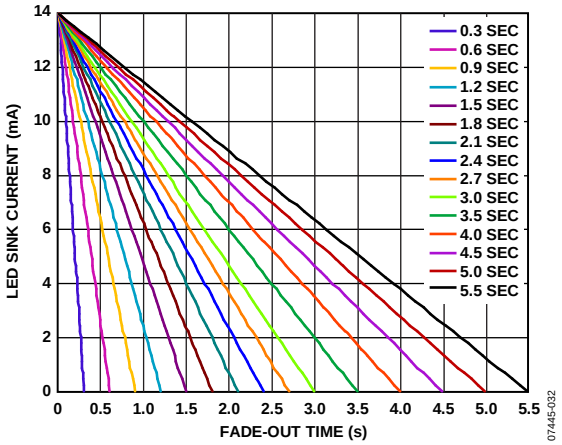

Figure 43. Linear Fade-Out Times

To achieve a more natural fading experience to the eye, the fade timers can be used in conjunction with the square law approximation codes (see Equation 4) by setting LED_LAW = 1.

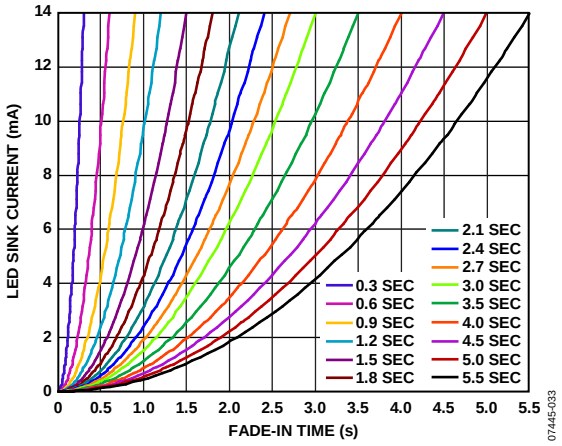

Figure 44. Square Law Fade-In Times

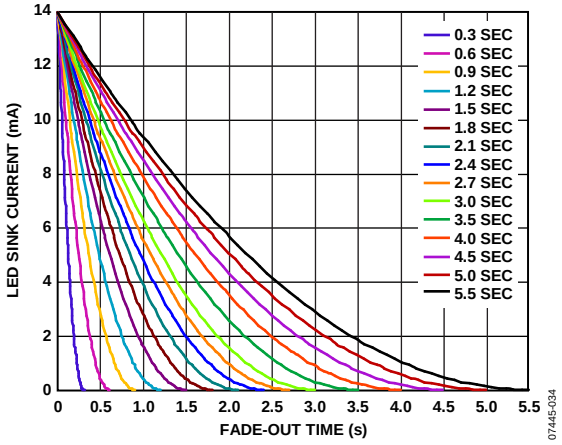

Figure 45. Square Law Fade-Out Times

The LED current sinks have additional timers to facilitate blinking functions. A shared on timer (LED_ONT) used in conjunction with three off timers (LED1_OFFT, LED2_OFFT, and LED3_OFFT) allow the LED current sinks to be configured in various blinking modes. The on timer can be set to four different settings: 0.2 sec, 0.6 sec, 0.8 sec, and 1.2 sec. The off timers have four different settings: disabled, 0.6 sec, 0.8 sec, and 1.2 sec. Blink mode is activated by setting the off timers to any setting other than disabled.

Program all fade, on, and off timers before enabling any of the LED current sinks. If LEDx is on during a blink cycle and LEDx_EN is cleared, it turns off (or fades to off if fade-out is enabled). If LEDx is off during a blink cycle and LEDx_EN is cleared, then it stays off.

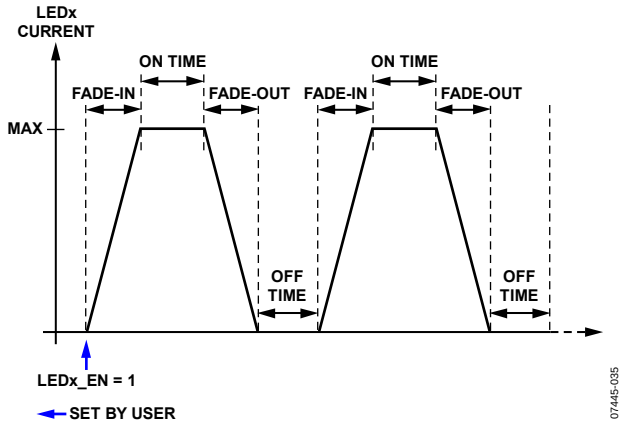

Figure 46. LEDx Blink Mode with Fading

INTERRUPT OUTPUT ($\overline{\text{INT}}$)

The ADP5520 can generate interrupts to an external processor via its interrupt output, $\overline{\text{INT}}$. $\overline{\text{INT}}$ is an active low open-drain pin that must be pulled up to VDDIO. $\overline{\text{INT}}$ can be asserted by one of several internal blocks, as shown in Figure 47.

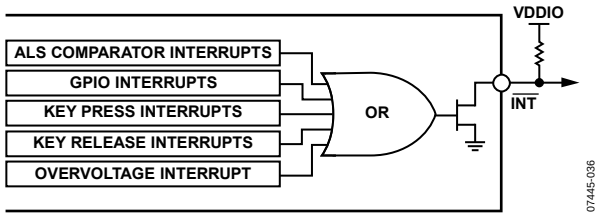

Figure 47. $\overline{\text{INT}}$ Pin Drive

RESET INPUT ($\overline{\text{RST}}$)

The ADP5520 can be restored to a power-on reset state if the $\overline{\text{RST}}$ pin is held low. $\overline{\text{RST}}$ contains a debounce circuit, so the pin must be held low for greater than 75 µs (typical) before a reset occurs.

COMMUNICATION INTERFACE

Communication to the ADP5520 is done via its I²C-compatible serial interface. Figure 48 shows a typical write sequence for programming an internal register.

1. The cycle begins with a start condition, followed by the chip write address (0x64).
2. The ADP5520 acknowledges the chip write address byte by pulling the data line low.
3. The address of the register to which data is to be written is sent next.
4. The ADP5520 acknowledges the register address byte by pulling the data line low.
5. The data byte to be written is sent next.
6. The ADP5520 acknowledges the data byte by pulling the data line low.
7. A stop condition completes the sequence.

Figure 49 shows a typical read sequence for reading back an internal register.

1. The cycle begins with a start condition, followed by the chip write address (0x64).
2. The ADP5520 acknowledges the chip write address byte by pulling the data line low.
3. The address of the register from which data is to be read is sent next.
4. The ADP5520 acknowledges the register address byte by pulling the data line low.
5. The cycle continues with a repeat start, followed by the chip read address (0x65).
6. The ADP5520 acknowledges the chip read address byte by pulling the data line low.
7. The ADP5520 places the contents of the previously addressed register on the bus for readback.
8. There is a no acknowledge following the readback data byte, and the cycle is completed with a stop condition.

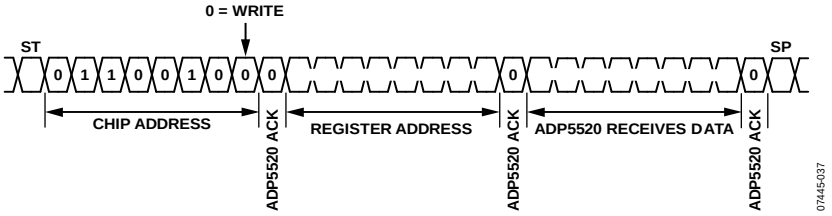

Figure 48. I²C Write Sequence

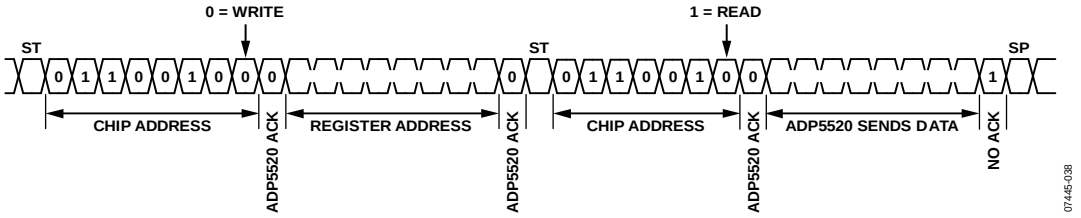

Figure 49. I²C Read Sequence

REGISTER MAP

All registers are 0 on reset. Unused bits are read as 0.

Table 7.

Register Address	Register Name	Register Description
0x00	MODE_STATUS	Sets device operating mode. Contains enables for backlight on/dim. Contains top-level interrupt status bits.
0x01	INTERRUPT_ENABLE	Contains enables for allowing interrupts to assert $\overline{INT}$.
0x02	BL_CONTROL	Sets parameters relating to backlight control.
0x03	BL_TIME	Contains backlight off and dim timers.
0x04	BL_FADE	Contains backlight fade-in and fade-out timers.
0x05	DAYLIGHT_MAX	Sets daylight (L1) maximum current.
0x06	DAYLIGHT_DIM	Sets daylight (L1) dim current.
0x07	OFFICE_MAX	Sets office (L2) maximum current.
0x08	OFFICE_DIM	Sets office (L2) dim current.
0x09	DARK_MAX	Sets dark (L3) maximum current.
0x0A	DARK_DIM	Sets dark (L3) dim current.
0x0B	BL_VALUE	Read-only register of what the backlight is presently set to.
0x0C	ALS_CMPR_CFG	Sets enables and filters for ambient light sensor comparators. Contains comparator output status bits.
0x0D	L2_TRIP	Sets the light sensor comparator (L2_CMPR) threshold point.
0x0E	L2_HYS	Sets the light sensor comparator (L2_CMPR hysteresis.
0x0F	L3_TRIP	Sets the light sensor comparator (L3_CMPR) threshold point.
0x10	L3_HYS	Sets the light sensor comparator (L3_CMPR) hysteresis.
0x11	LED_CONTROL	Contains enables and configuration for the three auxiliary LED current sinks.
0x12	LED_TIME	Contains the on and off timers for the three auxiliary LED current sinks.
0x13	LED_FADE	Contains the fade-in and fade-out timers for the three auxiliary LED current sinks.
0x14	LED1_CURRENT	Sets the LED 1 (ILED) sink current.
0x15	LED2_CURRENT	Sets the LED 2 (C3) sink current.
0x16	LED3_CURRENT	Sets the LED 3 (R3) sink current.
0x17	GPIO_CFG_1	Configuration for I/O pins. (GPIOs or keypad matrix)
0x18	GPIO_CFG_2	Configuration for I/O pins. (GPIO direction, input or output)
0x19	GPIO_IN	Read-only register. Reflects the logic state of GPIO inputs.
0x1A	GPIO_OUT	Sets GPIO output logic drive level.
0x1B	GPIO_INT_EN	GPIO input interrupt enable.
0x1C	GPIO_INT_STAT	GPIO input interrupt status.
0x1D	GPIO_INT_LVL	Configures the GPIO input interrupt level that causes an interrupt (active high or low).
0x1E	GPIO_DEBOUNCE	GPIO input debounce enable/disable.
0x1F	GPIO_PULLUP	GPIO pull-up enable/disable.
0x20	KP_INT_STAT_1	Read only register. Contains interrupt status information for key presses on Key A through Key H.
0x21	KP_INT_STAT_2	Read-only register. Contains interrupt status information for key presses on Key I through Key P.
0x22	KR_INT_STAT_1	Read-only register. Contains interrupt status information for key releases on Key A through Key H.
0x23	KR_INT_STAT_2	Read-only register. Contains interrupt status information for key releases on Key I through Key P.
0x24	KEY_STAT_1	Read-only register. Reflects the present state of Key A through Key H.
0x25	KEY_STAT_2	Read-only register. Reflects the present state of Key I through Key P.

DETAILED REGISTER DESCRIPTIONS

If one of the interrupt bits in Table 8 is cleared and there is a pending interrupt, $\overline{INT}$ deasserts for 50 µs and reasserts, but the status of the pending interrupt stays set.

Table 8. Register 0x00, Device Mode and Status (MODE_STATUS)

Bit	Mnemonic	R/W	Description
7	$\overline{STNBY}$	R/W	0 = device is in standby mode. If 1.8 V ≤ VDDIO ≤ 3.3 V, then I²C, GPIO, and key scanning functions are available. 1 = device is in operating mode. Additional functions, such as backlight driver, auxiliary LED sinks, and ambient light sensor functions, can be enabled.
6	BL_EN	R/W	0 = backlight driver is disabled. 1 = backlight driver is enabled.
5	DIM_EN		0 = dim mode is disabled. 1 = dim mode is enabled. Dim mode can be enabled in two ways. One is by manually setting this bit, in which case the backlight stays at a dim level until this bit is manually cleared. The second method is by setting the BL_DIMT timer, in which case an internal state machine sets this bit when the timer expires.
4	OVP_INT	R/W	0 = no overvoltage protection (OVP) condition. 1 = OVP condition detected. Once set, this bit can be cleared by writing a 1 to it.
3	CMPR_INT		0 = no ambient light sensor comparators have triggered. 1 = One of the ambient light sensor comparators has triggered. Once set, this bit can be cleared by writing a 1 to it.
2	GPI_INT		0 = no GPIO input interrupt detected. 1 = GPIO input interrupt condition has occurred. To clear this interrupt bit, the GPIO interrupt status (Register 0x1C) must be cleared first. Then this bit can be cleared by writing a 1 to it.
1	KR_INT		0 = no key release interrupt present. 1 = key release detected. To clear this interrupt bit, Key Release Interrupt Status 1 (Register 0x22) and Key Release Interrupt Status 2 (Register 0x23) must be cleared first. Then this bit can be cleared by writing a 1 to it.
0	KP_INT		0 = no key press interrupt present. 1 = key press detected. To clear this interrupt bit, Key Press Interrupt Status 1 (Register 0x20) and Key Press Interrupt Status 2 (Register 0x21) must be cleared first. Then this bit can be cleared by writing a 1 to it.

Table 9. Register 0x01, Interrupt Enable (INTERRUPT_ENABLE)

Bit	Mnemonic	R/W	Description
[7:5]			Unused.
4	AUTO_LD_EN	R/W	0 = autoload disabled. 1 = autoload enabled. A 1 mA dummy load turns on when the backlight code is less than 8 (linear law) or less than Code 32 (square law).
3	CMPR_IEN	R/W	0 = ambient light sensor comparators interrupt disabled. 1 = ambient light sensor comparators interrupt enabled.
2	OVP_IEN	R/W	0 = OVP interrupt disabled. 1 = OVP interrupt enabled.
1	KR_IEN	R/W	0 = key release interrupt disabled. 1 = key release interrupt enabled.
0	KP_IEN	R/W	0 = key press interrupt disabled. 1 = key press interrupt enabled.

Table 10. Register 0x02, Backlight Control (BL_CONTROL)

Bit	Mnemonic	R/W	Description
[7:6]	BL_LVL	R/W	Brightness level control for the backlight. 00 = daylight (L1). 01 = office (L2). 10 = dark (L3). See the description for the BL_AUTO_ADJ bit.
[5:4]	BL_LAW	R/W	Backlight fade-on/fade-off transfer characteristic. 00 = linear. 01 = square. 10 = Cubic 1. 11 = Cubic 2.
3	BL_AUTO_ADJ	R/W	0 = ambient light sensor comparators have no effect on the backlight operating level. The user can manually adjust backlight operating level using the BL_LVL bits. 1 = ambient light sensor comparators automatically adjust the backlight operating level. The internal state machine takes control of the BL_LVL bits.
2	OVP_EN	R/W	0 = backlight ramp-down during OVP disabled. 1 = backlight ramp-down during OVP enabled.
1	FOVR	R/W	0 = backlight fade override disabled. 1 = backlight fade override enabled.
0	KP_BL_EN	R/W	0 = key press has no effect on the backlight. 1 = key press causes internal state machine to assert BL_EN and turn on the backlight. If this function is used, assert this bit before asserting $\overline{\text{STNBY}}$ = 1.

Table 11. Register 0x03, Backlight Off and Dim Timers (BL_TIME)

Bit	Mnemonic	R/W	Description
[7:4]	BL_OFFT	R/W	Backlight off timer (set this timer before BL_EN is set). 0000 = timer disabled. 0001 = 10 sec. 0010 = 15 sec. 0011 = 20 sec. 0100 = 25 sec. 0101 = 30 sec. 0110 = 35 sec. 0111 = 40 sec. 1000 = 50 sec. 1001 = 60 sec. 1010 = 70 sec. 1011 = 80 sec. 1100 = 90 sec. 1101 = 100 sec. 1110 = 110 sec. 1111 = 120 sec.
[3:0]	BL_DIMT	R/W	Backlight dim timer (set this timer before BL_EN is set). 0000 = timer disabled. 0001 = 10 sec. 0010 = 15 sec. 0011 = 20 sec. 0100 = 25 sec. 0101 = 30 sec. 0110 = 35 sec. 0111 = 40 sec. 1000 = 50 sec. 1001 = 60 sec.

Bit	Mnemonic	R/W	Description
			1010 = 70 sec. 1011 = 80 sec. 1100 = 90 sec. 1101 = 100 sec. 1110 = 110 sec. 1111 = 120 sec.

Table 12. Register 0x04, Backlight Fade-In and Fade-Out Timers (BL_FADE)

Bit	Mnemonic	R/W	Description
[7:4]	BL_FO	R/W	Backlight fade-out timer (set this timer before BL_EN is set). 0000 = timer disabled. 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.
[3:0]	BL_FI	R/W	Backlight fade-in timer (set this timer before BL_EN is set). 0000 = timer disabled. 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.

Table 13. Register 0x05, Level 1 (Daylight) Maximum Current (DAYLIGHT_MAX)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	DAYLIGHT_MAX	R/W	Maximum current setting for the backlight when BL_LVL is at Level 1 (daylight). See Figure 16 for backlight current vs. sink code relationship.

Table 14. Register 0x06, Level 1 (Daylight) Dim Current (DAYLIGHT_DIM)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	DAYLIGHT_DIM	R/W	Dim current setting for the backlight when BL_LVL is at Level 1 (daylight). See Figure 16 for backlight current vs. sink code relationship.

Table 15. Register 0x07, Level 2 (Office) Maximum Current (OFFICE_MAX)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	OFFICE_MAX	R/W	Maximum current setting for the backlight when BL_LVL is at Level 2 (office). See Figure 16 for backlight current vs. sink code relationship.

Table 16. Register 0x08, Level 2 (Office) Dim Current (OFFICE_DIM)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	OFFICE_DIM	R/W	Dim current setting for the backlight when BL_LVL is at Level 2 (office). See Figure 16 for backlight current vs. sink code relationship.

Table 17. Register 0x09, Level 3 (Dark) Maximum Current (DARK_MAX)

Bit	Mnemonic	R/W	Description
7			Unused.
6 to 0	DARK_MAX	R/W	Maximum current setting for the backlight when BL_LVL is at Level 3 (dark). See Figure 16 for backlight current vs. sink code relationship.

Table 18. Register 0x0A, Level 3 (Dark) Dim Current (DARK_DIM)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	DARK_DIM	R/W	Dim current setting for the backlight when BL_LVL is at Level 3 (dark). See Figure 16 for backlight current vs. sink code relationship.

Table 19. Register 0x0B, Backlight Current Value (BL_VALUE)

Bit	Mnemonic	R/W	Description
7			Unused.
[6:0]	BL_VALUE	R	Read-only register. Contains the present value to which the backlight is programmed.

Table 20. Register 0x0C, Light Sensor Comparator Configuration (ALS_CMPR_CFG)

Bit	Mnemonic	R/W	Description
[7:5]	FILT	R/W	Light sensor filter time. 000 = 0.08 sec. 001 = 0.16 sec. 010 = 0.32 sec. 011 = 0.64 sec. 100 = 1.28 sec. 101 = 2.56 sec. 110 = 5.12 sec. 111 = 10.24 sec.
4	FORCE_RD	R/W	Forces the light sensor comparator to perform a single conversion. This bit is cleared by the internal state machine when the conversion is complete.
3	L3_OUT	R	0 = ambient light is greater than Level 3 (dark). 1 = L3_CMPR comparator has detected a change in ambient light from Level 2 (office) to Level 3 (dark).
2	L2_OUT	R	0 = ambient light is greater than Level 2 (office). 1 = L2_CMPR comparator has detected a change in ambient light from Level 1 (daylight) to Level 2 (office).
1	L3_EN	R/W	0 = disable Comparator L3_CMPR. 1 = enable Comparator L3_CMPR. If automatic backlight adjustment is required, BL_AUTO_ADJ must be set also.

Bit	Mnemonic	R/W	Description
0	L2_EN	R/W	0 = disable Comparator L2_CMPR. 1 = enable Comparator L2_CMPR. If automatic backlight adjustment is required, BL_AUTO_ADJ must be set also.

Table 21. Register 0x0D, Level 2 (Office) Comparator Trip Point (L2_TRIP)

Bit	Mnemonic	R/W	Description
[7:0]	L2_TRIP	R/W	Sets the trip value for Comparator L2_CMPR. If ambient light levels fall below this trip point, L2_OUT is set. Each code is equal to 4 µA (typical). Full scale is 1000 µA (typical).

Table 22. Register 0x0E, Level 2 (Office) Comparator Hysteresis (L2_HYS)

Bit	Mnemonic	R/W	Description
[7:0]	L2_HYS	R/W	Sets the hysteresis value for Comparator L2_CMPR. If ambient light levels increase above L2_TRIP + L2_HYS, then L2_OUT is cleared. Each code is equal to 4 µA (typical). Full scale is 1000 µA (typical).

Table 23. Register 0x0F, Level 3 (Dark) Comparator Trip Point (L3_TRIP)

Bit	Mnemonic	R/W	Description
[7:0]	L3_TRIP	R/W	Sets the trip value for Comparator L3_CMPR. If ambient light levels fall below this trip point, L3_OUT is set. Each code is equal to 0.5 µA (typical). Full scale is 127 µA (typical).

Table 24. Register 0x10, Level 3 (Dark) Comparator Hysteresis (L3_HYS)

Bit	Mnemonic	R/W	Description
[7:0]	L3_HYS	R/W	Sets the hysteresis value for Comparator L3_CMPR. If ambient light levels increase above L3_TRIP + L3_HYS, then L3_OUT is cleared. Each code is equal to 0.5 µA (typical). Full scale is 127 µA (typical).

Table 25. Register 0x11, LED Control (LED_CONTROL)

Bit	Mnemonic	R/W	Description
[7:6]			Unused.
5	R3_MODE	R/W	0 = R3 is configured as a current sink (LED 3). 1 = R3 is configured as a GPIO (D3).
4	C3_MODE	R/W	0 = C3 is configured as a current sink (LED 2). 1 = C3 is configured as a GPIO (D7).
3	LED_LAW	R/W	LED current sink fade-on/fade-off transfer characteristic. 0 = linear. 1 = square.
2	LED3_EN		0 = LED 3 is disabled. 1 = LED 3 is enabled.
1	LED2_EN		0 = LED 2 is disabled. 1 = LED 2 is enabled.
0	LED1_EN		0 = LED 1 is disabled. 1 = LED 1 is enabled.

Table 26. Register 0x12, Auxiliary LED On and Off Timers (LED_TIME)

Bit	Mnemonic	R/W	Description
[7:6]	LED_ONT	R/W	Sets the LED on time when used in conjunction with the LEDx_OFFT timer to perform LED blinking. All three LED sinks share this common timer. 00 = 0.2 sec. 01 = 0.6 sec. 10 = 0.8 sec. 11 = 1.2 sec.
[5:4]	LED3_OFFT	R/W	Sets the LED 3 off time when used in conjunction with the LED_ONT timer to perform LED blinking. LED 3 stays on continuously if the timer is disabled. 00 = LED 3 timer disabled. 01 = 0.6 sec. 10 = 0.8 sec. 11 = 1.2 sec.

Bit	Mnemonic	R/W	Description
[3:2]	LED2_OFFT	R/W	Sets the LED 2 off time when used in conjunction with the LED_ONT timer to perform LED blinking. LED 2 stays on continuously if the timer is disabled. 00 = LED 2 timer disabled. 01 = 0.6 sec. 10 = 0.8 sec. 11 = 1.2 sec.
[1:0]	LED1_OFFT	R/W	Sets the LED 1 off time when used in conjunction with the LED _ONT timer to perform LED blinking. LED 1 stays on continuously if the timer is disabled. 00 = LED 1 timer disabled. 01 = 0.6 sec. 10 = 0.8 sec. 11 = 1.2 sec.

Table 27. Register 0x13, LED Fade-In and Fade-Out Timers (LED_FADE)

Bit	Mnemonic	R/W	Description
[7:4]	LED_FO	R/W	LED fade-out timer (set this timer before LED x_EN is enabled). 0000 = timer disabled. 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.
[3:0]	LED_FI	R/W	LED fade-in timer (set this timer before LED x_EN is enabled). 0000 = timer disabled. 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.

Table 28. Register 0x14, LED 1 Sink Current (LED1_CURRENT)

Bit	Mnemonic	R/W	Description
[7:6]			Unused.
[5:0]	LED1_CURRENT	R/W	Sink current setting for LED 1. See Figure 41 for LED sink current vs. code relationship.

Table 29. Register 0x15, LED 2 Sink Current (LED2_CURRENT)

Bit	Mnemonic	R/W	Description
[7:6]			Unused.
[5:0]	LED2_CURRENT	R/W	Sink current setting for LED 2. See Figure 41 for LED sink current vs. code relationship.

Table 30. Register 0x16, LED 3 Sink Current (LED3_CURRENT)

Bit	Mnemonic	R/W	Description
[7:6]			Unused.
[5:0]	LED3_CURRENT	R/W	Sink current setting for LED 3. See Figure 41 for LED sink current vs. code relationship.

Table 31. Register 0x17, GPIO Configuration 1 (Pin Configuration) (GPIO_CFG_1)

Bit	Mnemonic	R/W	Description
7	C3_CONFIG	R/W	0 = C3 is configured as a GPIO (D7). 1 = C3 is configured as a keypad column (Column 3). Ensure that C3_MODE = 1 when C3 is to be used as a GPIO or a keypad column.
6	C2_CONFIG	R/W	0 = C2 is configured as a GPIO (D6). 1 = C2 is configured as a keypad column (Column 2).
5	C1_CONFIG	R/W	0 = C1 is configured as a GPIO (D5). 1 = C1 is configured as a keypad column (Column 1).
4	C0_CONFIG	R/W	0 = C0 is configured as a GPIO (D4). 1 = C0 is configured as a keypad column (Column 0).
3	R3_CONFIG	R/W	0 = R3 is configured as a GPIO (D3). 1 = R3 is configured as a keypad row (Row 3). Ensure that R3_MODE = 1 when R3 is to be used as a GPIO or a keypad row.
2	R2_CONFIG	R/W	0 = R2 is configured as a GPIO (D2). 1 = R2 is configured as a keypad row (Row 2).
1	R1_CONFIG	R/W	0 = R1 is configured as a GPIO (D1). 1 = R1 is configured as a keypad row (Row 1).
0	R0_CONFIG	R/W	0 = R0 is configured as a GPIO (D0). 1 = R0 is configured as a keypad row (Row 0).

Table 32. Register 0x18, GPIO Configuration 2 (GPIO Direction) (GPIO_CFG_2)

Bit	Mnemonic	R/W	Description
7	D7_DIR	R/W	0 = D7 is configured as an input. 1 = D7 is configured as an output.
6	D6_DIR	R/W	0 = D6 is configured as an input. 1 = D6 is configured as an output.
5	D5_DIR	R/W	0 = D5 is configured as an input. 1 = D5 is configured as an output.
4	D4_DIR	R/W	0 = D4 is configured as an input. 1 = D4 is configured as an output.
3	D3_DIR	R/W	0 = D3 is configured as an input. 1 = D3 is configured as an output.
2	D2_DIR	R/W	0 = D2 is configured as an input. 1 = D2 is configured as an output.
1	D1_DIR	R/W	0 = D1 is configured as an input. 1 = D1 is configured as an output.
0	D0_DIR	R/W	0 = D0 is configured as an input. 1 = D0 is configured as an output.

Table 33. Register 0x19, GPIO Input Status (GPIO_IN)

Bit	Mnemonic	R/W	Description
7	D7_IN	R	0 = D7 input is low. 1 = D7 input is high.
6	D6_IN	R	0 = D6 input is low. 1 = D6 input is high.
5	D5_IN	R	0 = D5 input is low. 1 = D5 input is high.
4	D4_IN	R	0 = D4 input is low. 1 = D4 input is high.
3	D3_IN	R	0 = D3 input is low. 1 = D3 input is high.
2	D2_IN	R	0 = D2 input is low. 1 = D2 input is high.
1	D1_IN	R	0 = D1 input is low. 1 = D1 input is high.
0	D0_IN	R	0 = D0 input is low. 1 = D0 input is high.

Table 34. Register 0x1A, GPIO Output Drive (GPIO_OUT)

Bit	Mnemonic	R/W	Description
7	D7_OUT	R/W	0 = D7 output is driven low. 1 = D7 output is driven high.
6	D6_OUT	R/W	0 = D6 output is driven low. 1 = D6 output is driven high.
5	D5_OUT	R/W	0 = D5 output is driven low. 1 = D5 output is driven high.
4	D4_OUT	R/W	0 = D4 output is driven low. 1 = D4 output is driven high.
3	D3_OUT	R/W	0 = D3 output is driven low. 1 = D3 output is driven high.
2	D2_OUT	R/W	0 = D2 output is driven low. 1 = D2 output is driven high.
1	D1_OUT	R/W	0 = D1 output is driven low. 1 = D1 output is driven high.
0	D0_OUT	R/W	0 = D0 output is driven low. 1 = D0 output is driven high.

Table 35. Register 0x1B, GPIO Interrupt Enable (GPIO_INT_EN)

Bit	Mnemonic	R/W	Description
7	D7_IN_IEN	R/W	0 = prevents D7 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D7 input to generate interrupts on $\overline{\text{INT}}$.
6	D6_IN_IEN	R/W	0 = prevents D6 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D6 input to generate interrupts on $\overline{\text{INT}}$.
5	D5_IN_IEN	R/W	0 = prevents D5 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D5 input to generate interrupts on $\overline{\text{INT}}$.
4	D4_IN_IEN	R/W	0 = prevents D4 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D4 input to generate interrupts on $\overline{\text{INT}}$.
3	D3_IN_IEN	R/W	0 = prevents D3 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D3 input to generate interrupts on $\overline{\text{INT}}$.
2	D2_IN_IEN	R/W	0 = prevents D2 input from generating interrupts on $\overline{\text{INT}}$. 1 = allows D2 input to generate interrupts on $\overline{\text{INT}}$.

Bit	Mnemonic	R/W	Description
1	D1_IN_IEN	R/W	0 = prevents D1 input from generating interrupts on $\overline{INT}$. 1 = allows D1 input to generate interrupts on $\overline{INT}$.
0	D0_IN_IEN	R/W	0 = prevents D0 input from generating interrupts on $\overline{INT}$. 1 = allows D0 input to generate interrupts on $\overline{INT}$.

Table 36. Register 0x1C, GPIO Interrupt Status (GPIO_INT_STAT)

Bit	Mnemonic	R/W	Description
7	D7_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D7_IN. Bit cleared when read twice.
6	D6_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D6_IN. Bit cleared when read twice.
5	D5_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D5_IN. Bit cleared when read twice.
4	D4_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D4_IN. Bit cleared when read twice.
3	D3_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D3_IN. Bit cleared when read twice.
2	D2_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D2_IN. Bit cleared when read twice.
1	D1_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D1_IN. Bit cleared when read twice.
0	D0_IN_ISTAT	R	0 = no interrupt detected. 1 = interrupt condition detected on D0_IN. Bit cleared when read twice.

Table 37. Register 0x1D, GPIO Interrupt Level Configuration (GPIO_INT_LVL)

Bit	Mnemonic	R/W	Description
7	D7_ILVL	R/W	0 = interrupt generated when D7_IN is low. 1 = interrupt generated when D7_IN is high.
6	D6_ILVL	R/W	0 = interrupt generated when D6_IN is low. 1 = interrupt generated when D6_IN is high.
5	D5_ILVL	R/W	0 = interrupt generated when D5_IN is low. 1 = interrupt generated when D5_IN is high.
4	D4_ILVL	R/W	0 = interrupt generated when D4_IN is low. 1 = interrupt generated when D4_IN is high.
3	D3_ILVL	R/W	0 = interrupt generated when D3_IN is low. 1 = interrupt generated when D3_IN is high.
2	D2_ILVL	R/W	0 = interrupt generated when D2_IN is low. 1 = interrupt generated when D2_IN is high.
1	D1_ILVL	R/W	0 = interrupt generated when D1_IN is low. 1 = interrupt generated when D1_IN is high.
0	D0_ILVL	R/W	0 = interrupt generated when D0_IN is low. 1 = interrupt generated when D0_IN is high.

Table 38. Register 0x1E, GPIO Input Debounce Enable/Disable (GPIO_DEBOUNCE)

Bit	Mnemonic	R/W	Description
7	D7_ IN_ DBNC	R/W	0 = D7_IN debounce enabled.
			1 = D7_IN debounce disabled.
6	D6_ IN_ DBNC	R/W	0 = D6_IN debounce enabled.
			1 = D6_IN debounce disabled.
5	D5_ IN_ DBNC	R/W	0 = D5_IN debounce enabled.
			1 = D5_IN debounce disabled.
4	D4_ IN_ DBNC	R/W	0 = D4_IN debounce enabled.
			1 = D4_IN debounce disabled.
3	D3_ IN_ DBNC	R/W	0 = D3_IN debounce enabled.
			1 = D3_IN debounce disabled.
2	D2_ IN_ DBNC	R/W	0 = D2_IN debounce enabled.
			1 = D2_IN debounce disabled.
1	D1_ IN_ DBNC	R/W	0 = D1_IN debounce enabled.
			1 = D1_IN debounce disabled.
0	D0_ IN_ DBNC	R/W	0 = D0_IN debounce enabled.
			1 = D0_IN debounce disabled.

Table 39. Register 0x1F, GPIO Pull-Up Enable/Disable (GPIO_PULLUP)

Bit	Mnemonic	R/W	Description
7	D7_PULL	R/W	0 = D7_IN pull-up disabled.
			1 = D7_IN pull-up enabled.
6	D6_PULL	R/W	0 = D6_IN pull-up disabled.
			1 = D6_IN pull-up enabled.
5	D5_PULL	R/W	0 = D5_IN pull-up disabled.
			1 = D5_IN pull-up enabled.
4	D4_PULL	R/W	0 = D4_IN pull-up disabled.
			1 = D4_IN pull-up enabled.
3	D3_PULL	R/W	0 = D3_IN pull-up disabled.
			1 = D3_IN pull-up enabled.
2	D2_PULL	R/W	0 = D2_IN pull-up disabled.
			1 = D2_IN pull-up enabled.
1	D1_PULL	R/W	0 = D1_IN pull-up disabled.
			1 = D1_IN pull-up enabled.
0	D0_PULL	R/W	0 = D0_IN pull-up disabled.
			1 = D0_IN pull-up enabled.

Table 40. Register 0x20, Key Press Interrupt Status 1 (KP_INT_STAT_1)

Bit	Mnemonic	R/W	Description
7	KP_A_ISTAT	R	0 = no interrupt detected.
			1 = interrupt due to Key A press. Bit cleared on read.
6	KP_B_ISTAT	R	0 = no interrupt detected.
			1 = interrupt due to Key B press. Bit cleared on read.
5	KP_C_ISTAT	R	0 = no interrupt detected.
			1 = interrupt due to Key C press. Bit cleared on read.
4	KP_D_ISTAT	R	0 = no interrupt detected.
			1 = interrupt due to Key D press. Bit cleared on read.
3	KP_E_ISTAT	R	0 = no interrupt detected.
			1 = interrupt due to Key E press. Bit cleared on read.

Bit	Mnemonic	R/W	Description
2	KP_F_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key F press. Bit cleared on read.
1	KP_G_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key G press. Bit cleared on read.
0	KP_H_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key H press. Bit cleared on read.

Table 41. Register 0x21, Key Press Interrupt Status 2 (KP_INT_STAT_2)

Bit	Mnemonic	R/W	Description
7	KP_I_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key I press. Bit cleared on read.
6	KP_J_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key J press. Bit cleared on read.
5	KP_K_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key K press. Bit cleared on read.
4	KP_L_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key L press. Bit cleared on read.
3	KP_M_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key M press. Bit cleared on read.
2	KP_N_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key N press. Bit cleared on read.
1	KP_O_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key O press. Bit cleared on read.
0	KP_P_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key P press. Bit cleared on read.

Table 42. Register 0x22, Key Release Interrupt Status 1 (KR_INT_STAT_1)

Bit	Mnemonic	R/W	Description
7	KR_A_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key A release. Bit cleared on read.
6	KR_B_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key B release. Bit cleared on read.
5	KR_C_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key C release. Bit cleared on read.
4	KR_D_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key D release. Bit cleared on read.
3	KR_E_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key E release. Bit cleared on read.
2	KR_F_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key F release. Bit cleared on read.
1	KR_G_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key G release. Bit cleared on read.
0	KR_H_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key H release. Bit cleared on read.

Table 43. Register 0x23, Key Release Interrupt Status 2 (KR_INT_STAT_2)

Bit	Mnemonic	R/W	Description
7	KR_I_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key I release. Bit cleared on read.
6	KR_J_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key J release. Bit cleared on read.
5	KR_K_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key K release. Bit cleared on read.

Bit	Mnemonic	R/W	Description
4	KR_L_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key L release. Bit cleared on read.
3	KR_M_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key M release. Bit cleared on read.
2	KR_N_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key N release. Bit cleared on read.
1	KR_O_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key O release. Bit cleared on read.
0	KR_P_ISTAT	R	0 = no interrupt detected. 1 = interrupt due to Key P release. Bit cleared on read.

Table 44. Register 0x24, Key Status 1 (KEY_STAT_1)

Bit	Mnemonic	R/W	Description
7	KEY_A_STAT	R	0 = Key A is currently released. 1 = Key A is currently pressed.
6	KEY_B_STAT	R	0 = Key B is currently released. 1 = Key B is currently pressed.
5	KEY_C_STAT	R	0 = Key C is currently released. 1 = Key C is currently pressed.
4	KEY_D_STAT	R	0 = Key D is currently released. 1 = Key D is currently pressed.
3	KEY_E_STAT	R	0 = Key E is currently released. 1 = Key E is currently pressed.
2	KEY_F_STAT	R	0 = Key F is currently released. 1 = Key F is currently pressed.
1	KEY_G_STAT	R	0 = Key G is currently released. 1 = Key G is currently pressed.
0	KEY_H_STAT	R	0 = Key H is currently released. 1 = Key H is currently pressed.

Table 45. Register 0x25, Key Status 2 (KEY_STAT_2)

Bit	Mnemonic	R/W	Description
7	KEY_I_STAT	R	0 = Key I is currently released. 1 = Key I is currently pressed.
6	KEY_J_STAT	R	0 = Key J is currently released. 1 = Key J is currently pressed.
5	KEY_K_STAT	R	0 = Key K is currently released. 1 = Key K is currently pressed.
4	KEY_L_STAT	R	0 = Key L is currently released. 1 = Key L is currently pressed.
3	KEY_M_STAT	R	0 = Key M is currently released. 1 = Key M is currently pressed.
2	KEY_N_STAT	R	0 = Key N is currently released. 1 = Key N is currently pressed.
1	KEY_O_STAT	R	0 = Key O is currently released. 1 = Key O is currently pressed.
0	KEY_P_STAT	R	0 = Key P is currently released. 1 = Key P is currently pressed.

APPLICATIONS INFORMATION

CONVERTER TOPOLOGY

The ADP5520 backlight driver utilizes a dc-to-dc step-up (boost) converter to achieve the high voltage levels required to drive up to six white LEDs in series. Figure 50 shows the basic asynchronous boost converter topology.

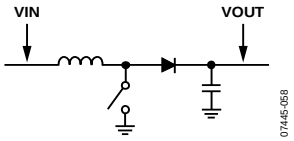

Figure 50. Basic Asynchronous Boost Converter Topology

Assuming an initial steady state condition where the switch has been open for a long time, then the output voltage (VOUT) is equal to the input voltage (VIN), minus a diode drop.

If the switch is closed, the output voltage maintains its value as the diode blocks its path to ground. The inductor, however, has a voltage differential across its terminals. Current in an inductor cannot change instantaneously, so it increases linearly at a rate of

$$di/dt = VIN/L$$

where L is the inductance value in Henrys.

If the switch is kept closed, the current increases until the inductor reaches its saturation limit, at which point the inductor becomes a dc path to ground. Therefore, keep the switch closed only long enough to build some transient energy in the inductor, but not so long that the inductor becomes saturated.

When the switch is opened, the current that has built up in the inductor continues to flow (as previously mentioned, the current in an inductor cannot change instantaneously), so the voltage at the top of the switch increases and forward biases the diode, allowing the inductor current to charge the capacitor, and, therefore, increase the overall output voltage level. If the switch is continuously opened and closed, the output voltage continues to increase.

Figure 51 shows the boost configuration as used in the ADP5520. A Schottky diode is used due to its fast turn-on time and low forward voltage drop. An input capacitor is added to reduce ripple voltage that is generated on the input supply due to charging/discharging of the inductor. An integrated power switch is used to control current levels in the inductor. A control loop consisting of a feedback signal, some safety limiting features, and a switch drive signal complete the boost converter topology.

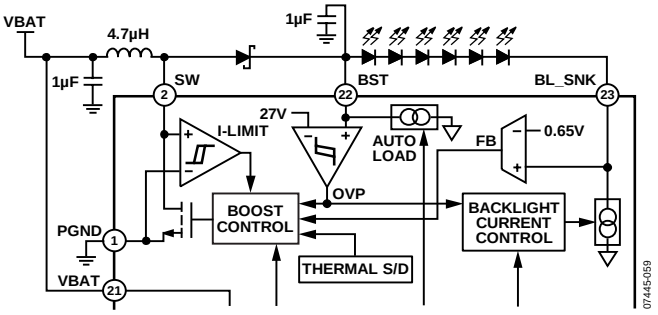

Figure 51. Boost Configuration

The ADP5520 uses a current-limiting PFM control scheme. For medium to large output currents, the converter operates in pseudo continuous conduction mode (CCM). It generates bursts of peak current limited pulses (600 mA typical) in the inductor, as shown in Figure 9.

For light output currents, the converter operates in pseudo discontinuous conduction mode (DCM). It generates bursts of small (200 mA typical) and medium (400 mA typical) current pulses in the inductor, as shown in Figure 11.

To maintain reasonable burst frequencies during very light load conditions, an automatic dummy load feature is available. When enabled, the 1 mA dummy load is activated if the backlight sink current code drops below 8 while in linear law mode, or if the backlight sink current code drops below 32 while in square law mode.

Safety Features

The ADP5520 utilizes an overvoltage protection (OVP) circuit that monitors the boosted voltage on the output capacitor. If the LED string becomes open (due to a broken LED), the control circuit continually commands the boost voltage to increase. If the boost level exceeds the maximum process rating for the ADP5520, damage to the device can occur. The ADP5520 boost converter has an OVP limit of 27 V (typical).

The ADP5520 also has a feature that ramps down the backlight code when an OVP condition is detected. This may be useful in conditions where LEDs with marginally high forward voltages are used in low ambient conditions. The feature can be enabled by setting the OVP_EN bit in Register 0x02.

The ADP5520 also features a thermal shutdown circuit. When the die junction temperature reaches 150°C (typical), the boost converter shuts down. It remains shut down until the die temperature falls by 10°C (typical).

Component Selection

The ADP5520 boost converter is designed for use with a 4.7 µH inductor. Choose an inductor with a sufficient current rating to prevent it from going into saturation. The peak current limit of the ADP5520 is 750 mA (maximum), so choose an inductor with a greater saturation rating. To maximize efficiency, choose an inductor with a low series resistance (DCR).

The ADP5520 is an asynchronous boost and, as such, requires an external Schottky diode to conduct the inductor current to the output capacitor and LED string when the power switch is off. Ensure that the Schottky diode peak current rating is greater than the maximum inductor current. Choose a Schottky diode with an average current rating that is significantly larger than the maximum LED current. To prevent thermal runaway, derate the Schottky diode to ensure reliable operation at high junction temperatures. To maximize efficiency, select a Schottky diode with a low forward voltage. When the power switch is on, the Schottky diode blocks the dc path from the output capacitor to ground. Therefore, choose a Schottky diode with a reverse breakdown greater than the maximum boost voltage. A 40 V, 1 A Schottky diode is recommended.

The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. Use an input capacitor with sufficient ripple current rating to handle the inductor ripple. A 1 µF X5R/X7R ceramic capacitor rated for 16 V dc bias is recommended for the input capacitance.

The output capacitor maintains the output voltage when the Schottky diode is not conducting. Due to the high levels of boost voltage required, a 1 µF X5R/X7R ceramic capacitor rated for 50 V dc bias is recommended for output capacitance.

Note that dc bias characterization data is available from capacitor manufacturers and must be taken into account when selecting input and output capacitors.

PCB LAYOUT

Good PCB layout is important to maximize efficiency and to minimize noise and electromagnetic interference (EMI). To minimize large current loops, place the input capacitor, inductor, Schottky diode, and output capacitor as close as possible to each other and to the ADP5520 using wide tracks (use shapes where possible). For thermal relief, connect the exposed pad of the LFCSP package to ground (GND).

Connect PGND and GND to each other at the bottom of the output capacitor.

Figure 52 shows an example PCB layout with the main power components required for backlight driving.

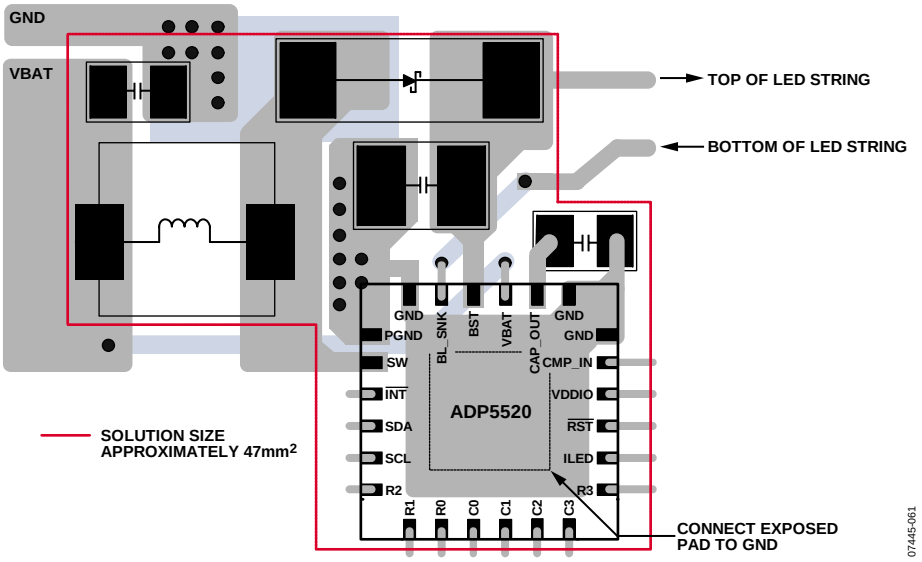

Figure 52. Example PCB Layout

EXAMPLE CIRCUITS

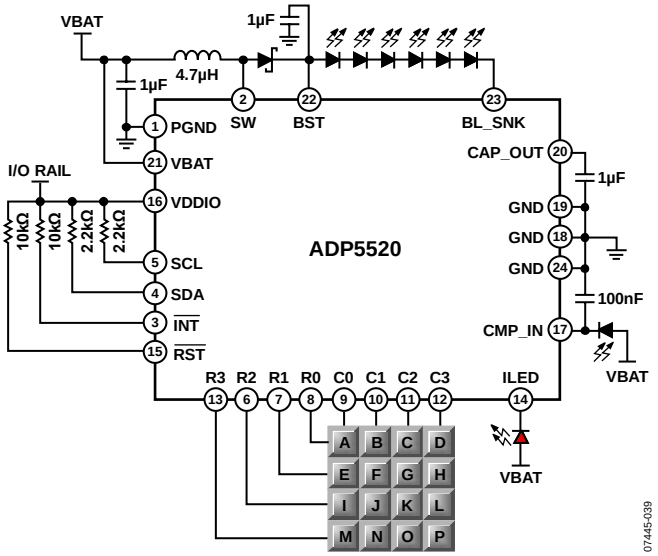

Figure 53. I/O Configuration Example 1

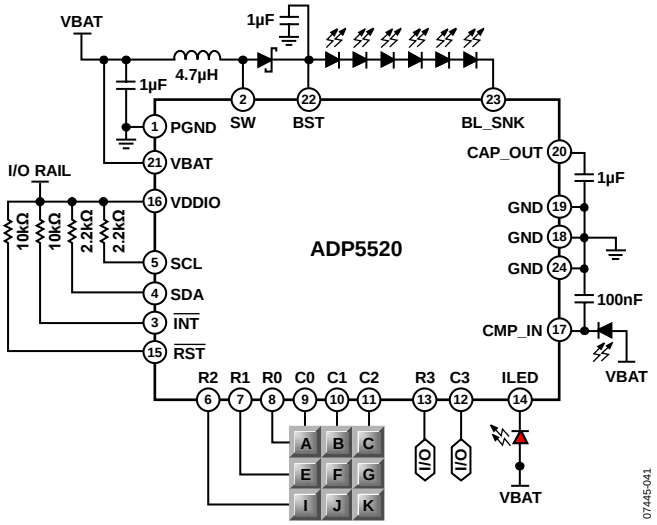

Figure 55. I/O Configuration Example 3

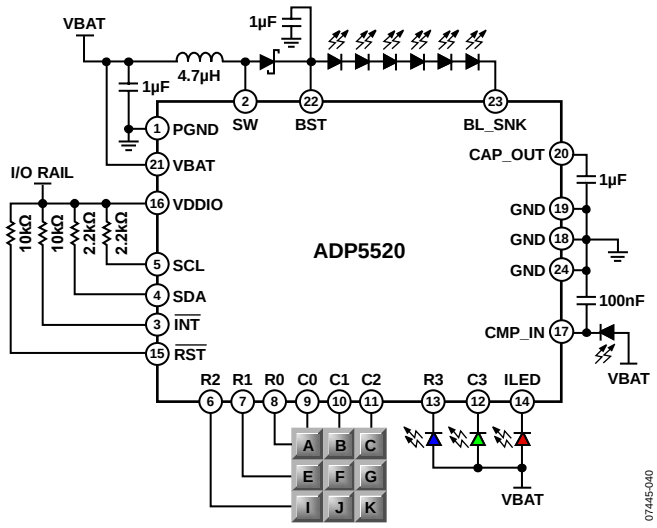

Figure 54. I/O Configuration Example 2

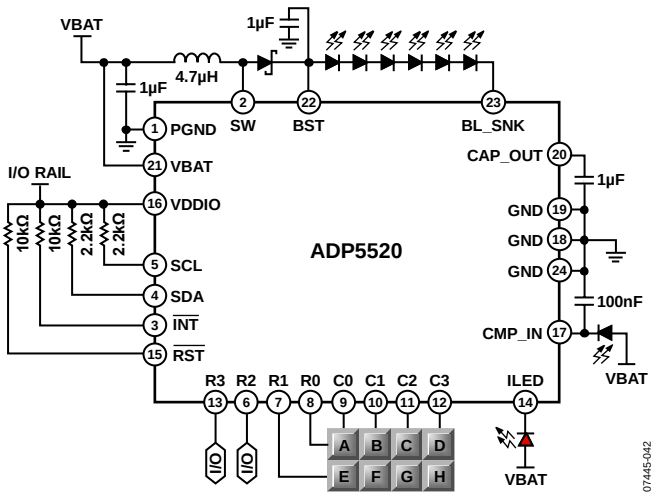

Figure 56. I/O Configuration Example 4

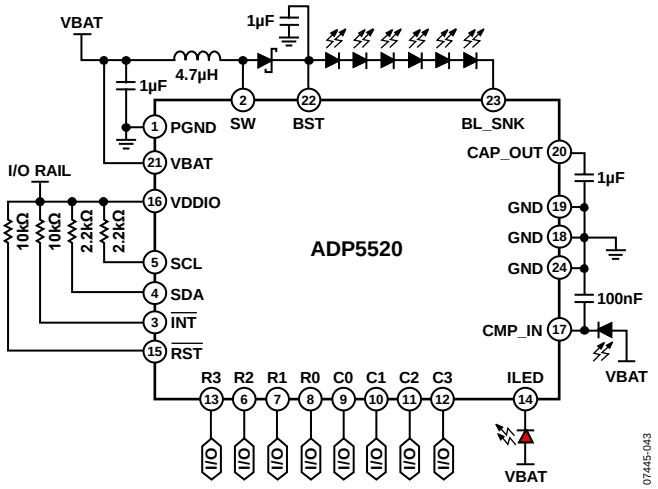

Figure 57. I/O Configuration Example 5

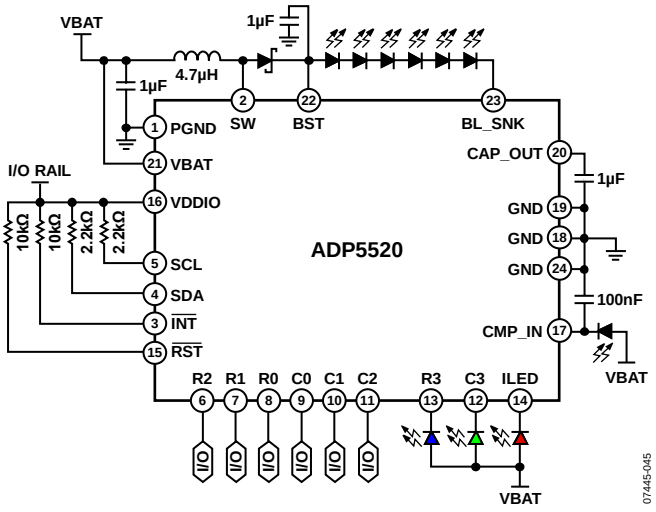

Figure 59. I/O Configuration Example 7

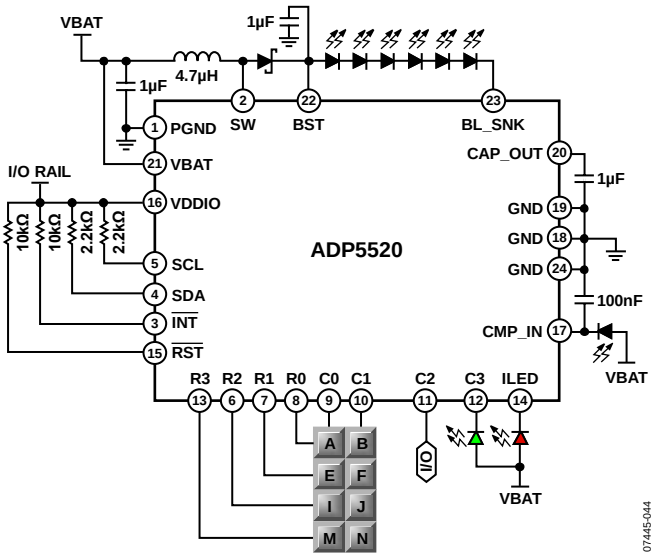

Figure 58. I/O Configuration Example 6

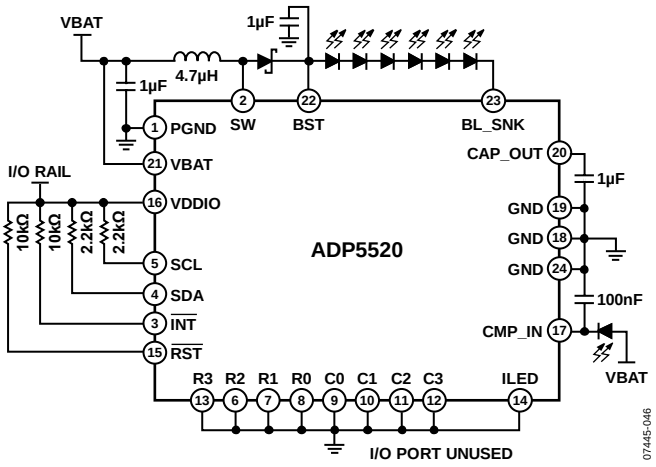

Figure 60. I/O Configuration Example 8

OUTLINE DIMENSIONS

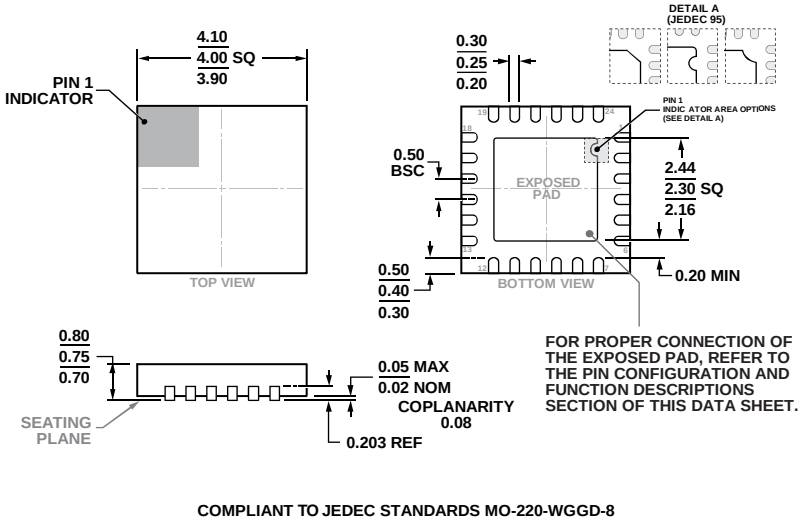

Figure 61. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5520ACPZ-RL	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-14

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D07445-0-10/17(B)