CD54HC4049/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C		-55°C to +125°C		UNITS
			HC		54HC		
		V	Min.	Max.	Min.	Max.	
Propagation Delay nA to n$\overline{Y}$	t_{PLH} t_{PHL}	2	—	85	—	130	ns
		4.5	—	17•	—	26•	
		6	—	14	—	22	
Transition Time	t_{TLH} t_{THL}	2	—	75	—	110	
		4.5	—	15	—	22	
		6	—	13	—	19	
Input Capacitance	C_I	—	—	10	—	10	pF

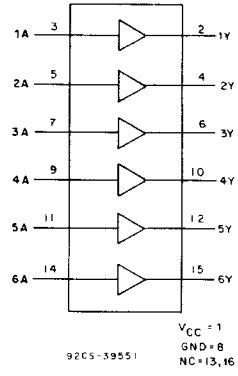
Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC4049	2,4,6,10,12, 13,15,16	3,5,7-9,11,14	1*	2,4,6,10,12, 13,15,16	8	1*,3,5,7,9,11,14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	25 kHz
CD54HC4049	13	8	2,4,6,10,12,15	1*,16	3,5,7,9,11,14	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.
Connect pins marked (*) without using a resistor.

CD54HC4050/3A Hex HIGH-to-LOW Level Shifter

The RCA CD54HC4050 is fabricated with high-speed silicon gate technology. These parts have a modified input protection structure that enables them to be used as logic level translators which will convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 0-V to 15-V input logic levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from both positive and negative electrostatic discharge. These parts can also be used as simple buffers or inverters without level translation. The CD54HC4050 is an enhanced version of an equivalent CMOS type.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	2•	μA
	−55°C / +125°C	6	—	—	6, 0	—	—	—	40•	μA

The complete Static Electrical Test specification consists of the above by-type Static Tests combined with the Standard Static tests in the beginning of this section.

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC} V	25°C HC Min.	25°C HC Max.	−55°C to +125°C 54HC Min.	−55°C to +125°C 54HC Max.	UNITS
Propagation Delay nA to nȲ	t_{PLH} t_{PHL}	2	—	85	—	130	ns
		4.5	—	17•	—	26•	ns
		6	—	14	—	22	ns
Transition Time	t_{TLH} t_{THL}	2	—	75	—	110	ns
		4.5	—	15	—	22	ns
		6	—	13	—	19	ns
Input Capacitance	C_I	—	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I OPEN	STATIC BURN-IN I GROUND	STATIC BURN-IN I V_{CC} (6V)	STATIC BURN-IN II OPEN	STATIC BURN-IN II GROUND	STATIC BURN-IN II V_{CC} (6V)
CD54HC4050	2,4,6,10,12, 13,15,16	3,5,7-9,11,14	1*	2,4,6,10,12, 13,15,16	8	1*,3,5,7,9,11,14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**OSCILLATOR 25 kHz**
CD54HC4050	13	8	2,4,6,10,12,15	1*,16	3,5,7,9,11,14	—

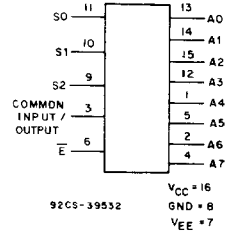
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.
Connect pins marked (*) without using a resistor.

8-Channel Analog Multiplexer/Demultiplexer

CD54HC4051/3A CD54HCT4051/3A

The RCA CD54HC4051 and CD54HCT4051 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which, when high, disables all switches to their "off" state.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11