

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

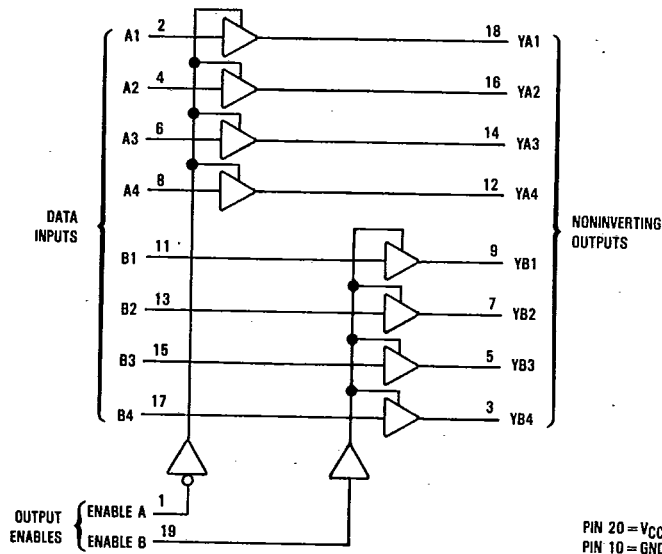
The MC54/74HC241A is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other sub-oriented systems. The device has noninverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

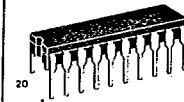
The HC241A is similar in function to the HC244A and HC240A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

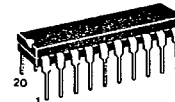
LOGIC DIAGRAM



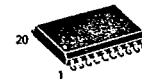
MC54/74HC241A



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74HCXXXAN Plastic
MC54HCXXXAJ Ceramic
MC74HCXXXADW SOIC

T_A = -55° to 125°C for all packages.

PIN ASSIGNMENT

ENABLE A	1	20	V _{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	YB4
YB3	5	16	YA2
A3	6	15	YB3
YB2	7	14	YA3
A4	8	13	YB2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Output	Inputs		Output
Enable A	A	YA	Enable B	B	YB
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC241A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

MC54/74HC241A

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V _{CC} = 5.0 V	pF
		34	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

SWITCHING WAVEFORMS

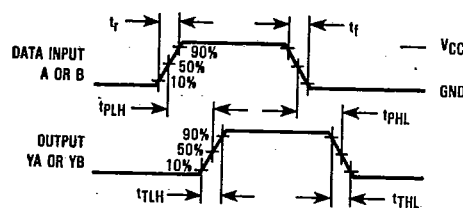


Figure 1

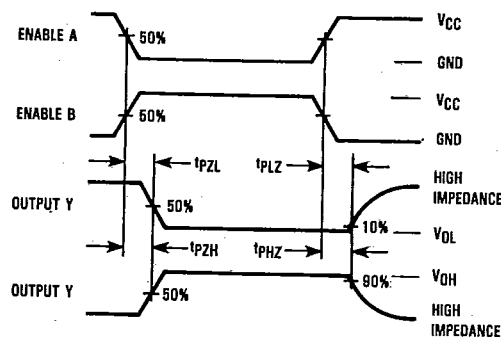
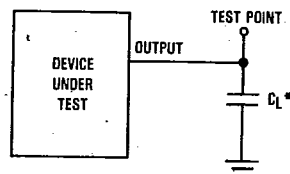
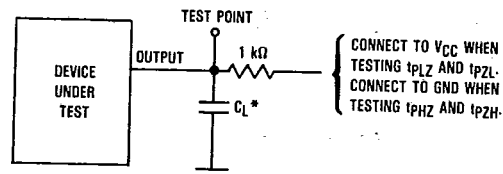


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

MC54/74HC241A

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

CONTROLS

Enable A (PIN 1) — Output enable (active-low). When a low level is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

Enable B (PIN 19) — Output enable (active-high). When a high level is applied to this pin, the outputs of the "B" devices are enabled and the devices function as noninverting buffers. When a low level is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

LOGIC DETAIL

