

Samurai-6I/IX

6 Port 10/100 Mbit/s Single Chip Ethernet Switch
Controller (ADM6996IX-Green Package Version)
ADM6996I/IX, Version AD

Data Sheet

Revision 1.4

Communication Solutions



Never stop thinking

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ADM6996I/IX, 6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996IX-Green Package Version)

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1 Product Overview

1.1 Samurai-6I/6IX (ADM6996I/IX) Overview

The Samurai-6I/6IX (ADM6996I/IX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) five-port 10/100 Mbit/s TX/FX plus one 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbit/s Full/Half duplex. The Samurai-6I/6IX (ADM6996I/IX) is intended for applications such as stand alone bridges for Digital Home Application such as ADSL Router, Wireless Router, EPON/GPON Router, IAD, IP Set Top Box, VOIP and Video application. The Samurai-6IX (ADM6996IX) is the environmentally friendly "green" package version.

Samurai-6I/6IX (ADM6996I/IX) provides advanced functions such as: **802.1p(Q.O.S.), Layer4 Q.O.S, 802.1Q(VLAN), Security, Bandwidth Control, Port Mirror, Hardware IGMP snooping and Easy Management** functions.

The Samurai-6I/6IX (ADM6996I/IX) also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffer full. When Back Pressure is enabled and there is no receive buffer available for the incoming packet, the Samurai-6I/6IX (ADM6996I/IX) will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for packet buffering is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

Samurai-6I/6IX (ADM6996I/IX) also supports priority features by Port-Base, VLAN, UDP/TCP destination port number and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of programmable rate fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN also is supported.

An intelligent address recognition algorithm makes Samurai-6I/6IX (ADM6996I/IX) able to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Security and Port Locking functions are also supported by Samurai-6I/6IX (ADM6996I/IX) to use on Building Internet access to prevent unathourized or multiple users sharing one port traffic.

1.2 Features

- Five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and one MII/GPSI/RMII port
- 2K MAC address tables with 4-ways associative hash algorithm
- 6KX64 bits packet buffers are divided into 192 blocks of 256 bytes each
- Four queues for QoS
- Priority features by Port-Based, 802.1p, IP TOS, Diffserv, TCP/UDP Destination Port Application-Based of packets
- Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Single/Dual color LED mode with Power On auto diagnostic. Collision/Duplex LED can be separated using register setting
- 802.3x Flow Control pause packet for Full Duplex
- Back Pressure function for Half Duplex operation
- Supports packet lengths up to 1518/1522 (Default)/1536/1784 bytes in maximum
- Scalable Per Port Bandwidth Control (Both Ingress and Egress).
- Broadcast/Multicast Storm Suppression
- 802.1Q VLAN. Up to 16 VLAN groups are implemented by full 12 bits VID matching
- MAC clone function to enable multiple WAN application

- TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Interrupt pin, Interrupt Register and Interrupt Mask Register. Programmable interrupt polarity (Default active low)
- Easy Management 32-bit smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count
- Supports 32 hardware IGMP Table (Multicast Table)
- MAC Address Table is accessible
- Supports 802.1x security function
- Supports Spanning Tree Protocol
- Support Port Mirror
- Support special tag for easy packet control.
- Supports internal counter/PHY status output for management system
- 25M Crystal
- 128 QFP package with 0.18 μm technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

1.3 Applications

Samurai-6I/6IX (ADM6996I/IX):

- ADSL, VDSL2, Wireless, Wire, Gateway and IP Set Top Box Router
- Voice and Video applications

1.4 Block Diagram

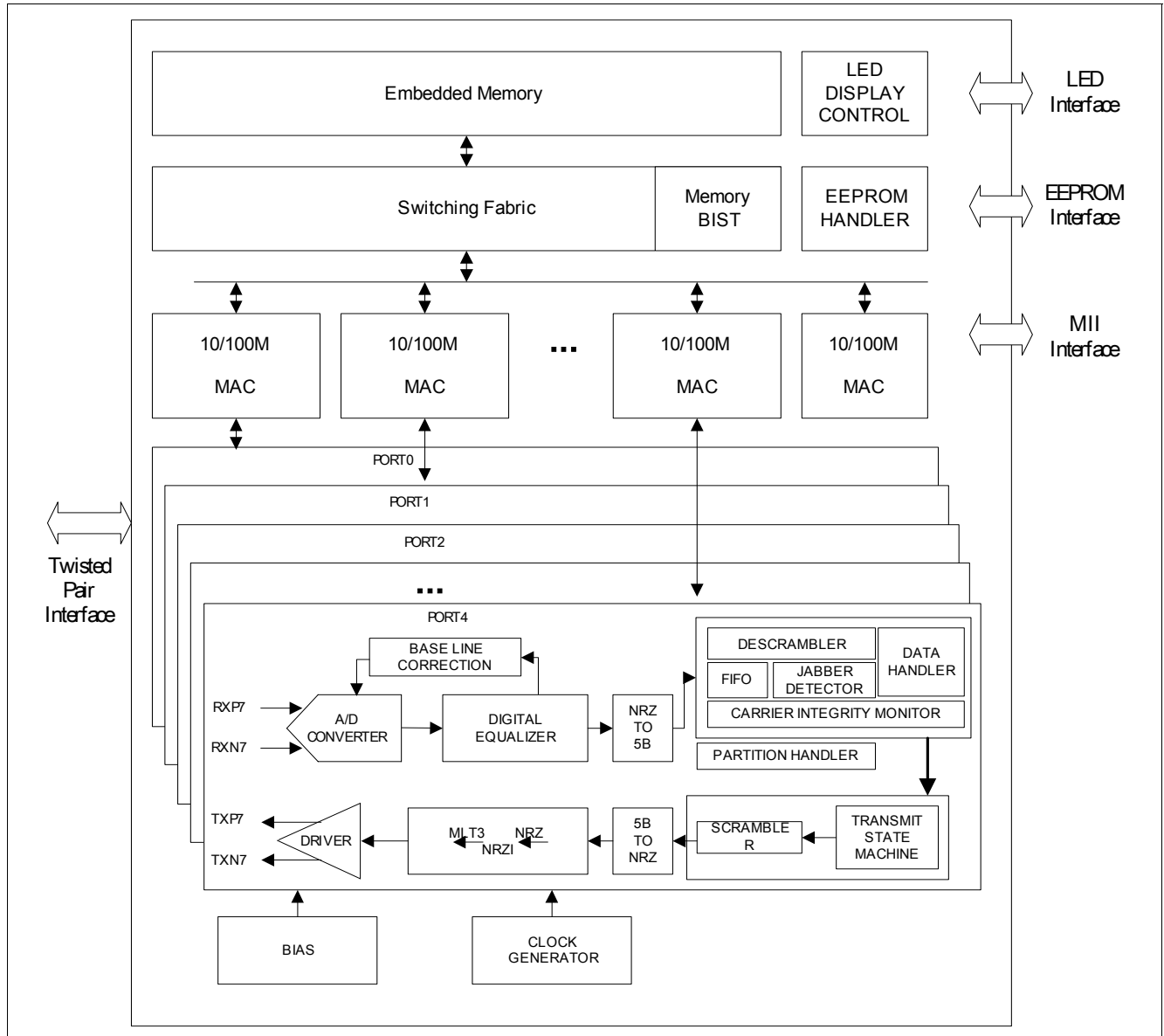


Figure 1 Samurai-6I/6IX (ADM6996I/IX) Block Diagram

1.5 Data Lengths

qword: 64 bits
dword: 32 bits
word: 16 bits
byte: 8 bits
nibble: 4 bits

2 Interface Description

This chapter describes the interface descriptions for the Samurai-6I/6IX (ADM6996I/IX)

- Pin Diagram
- Abbreviations
- Pin Description by Function

2.1 Pin Diagram

Figure 2 shows the pin diagram for the Samurai-6I/6IX (ADM6996I/IX).

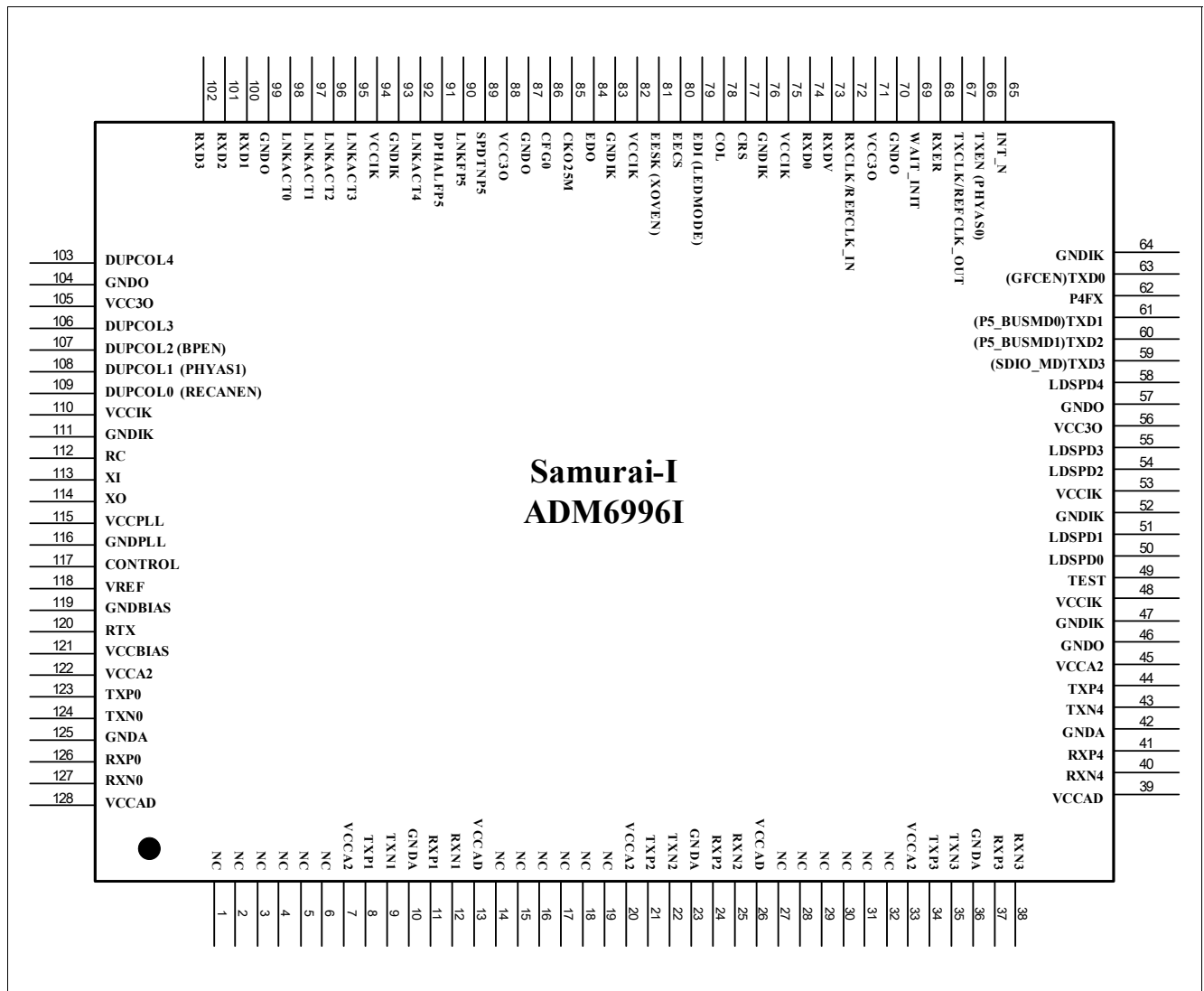


Figure 2 5 TP/FX PORT + 1 MII PORT 128 Pin Diagram

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

| Abbreviations | Description |
|---------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

Table 2 Abbreviations for Buffer Type

| Abbreviations | Description |
|---------------|--|
| Z | High impedance |
| PU | Pull up, 10 k Ω |
| PD | Pull down, 10 k Ω |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

2.3 Pin Description by Function

Samurai-6I/6IX (ADM6996I/IX) pins are categorized into one of the following groups:

- Network Media Connection
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

Note: **Table 1** can be used for reference.

Table 3 IO Signals

| Ball No. | Name | Pin Type | Buffer Type | Function |
|--------------------------|-------|----------|-------------|---|
| Network Media Connection | | | | |
| 41 | RXP_4 | AI/O | ANA | Receive Pair Differential data is received on this pin. |
| 37 | RXP_3 | | | |
| 24 | RXP_2 | | | |
| 11 | RXP_1 | | | |
| 126 | RXP_0 | | | |
| 40 | RXN_4 | AI/O | ANA | |
| 38 | RXN_3 | | | |
| 25 | RXN_2 | | | |
| 12 | RXN_1 | | | |
| 127 | RXN_0 | | | |
| 44 | TXP_4 | AI/O | ANA | Transmit Pair Differential data is transmitted on this pin. |
| 34 | TXP_3 | | | |
| 21 | TXP_2 | | | |
| 8 | TXP_1 | | | |
| 123 | TXP_0 | | | |
| 43 | TXN_4 | AI/O | ANA | |
| 35 | TXN_3 | | | |
| 22 | TXN_2 | | | |
| 9 | TXN_1 | | | |
| 124 | TXN_0 | | | |

Port 5 MII Interface

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|------------------|--|
| 63 | GFCEN | I | PU, LVTTTL | Global Flow Control Enable Value on this pin will be latched by Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL(RC) as Flow control enable. <i>Note: Power On Setting</i> 0 _B Flow Control Capability is dependent upon the register setting in corresponding EEPROM register 1 _B All ports flow control capabilities are enabled |
| | MII_TXD0 | O | 4 mA, PU, LVTTTL | Port 5 Transmit Data Bit 0 in MII Mode Bit[0] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| | GPSI_TXD | O | 4 mA, PU, LVTTTL | Port 5 Transmit Data in GPSI Mode When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_TXCLK. |
| | RMII_TXD0 | O | 4 mA, PU, LVTTTL | Port 5 Transmit Data Bit 0 in RMII Mode When port 5 is operating in RMII mode, this pin acts as RMII Transmit Data Bit [0]. Synchronous to the rising edge of REFCLK_IN. |
| 61 | P5_BUSMD0 | I | PD, LVTTTL | Port 5 Bus Mode Selection Bit 0 Value on this pin will be latched by Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL(RC) as port 5 bus mode selection bit 0. Combined with P5_BUSMD1, Samurai-6I/6IX (ADM6996I/IX) provides 3 bus type for port 5. P5_BUSMD[1:0], Interface <i>Note: Power On Setting</i> 00 _B MII 01 _B GPSI 10 _B RMII 11 _B Reserved and not allowed |
| | MII_TXD1 | O | 4 mA, PD, LVTTTL | Port 5 Transmit Data Bit 1 in MII Mode Bit[1] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| | RMII_TXD1 | O | 4 mA, PD, LVTTTL | Port 5 Transmit Data Bit 1 in RMII Mode Bit[1] of RMII Transmit data of port 5. Synchronous to the rising edge of REFCLK_IN. |

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-----------|----------|------------------|--|
| 60 | P5_BUSMD1 | I | PD, LVTTTL | Port 5 Bus Mode Selection Bit 1 Value on this pin will be latched by Samurai-6I/6IX (ADM6996I) at the rising edge of RESETL as port 5 bus mode selection bit 1. Combined with P5_BUSMD0 , Samurai-6I/6IX (ADM6996I/IX) provides 3 bus types for port 5. <i>Note: Power On Setting</i> |
| | MII_TXD2 | O | 4 mA, PD, LVTTTL | Port 5 Transmit Data Bit 2 in MII Mode Bit[2] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| 59 | SDIO_MD | I | PD, LVTTTL | SDC/SDIO Mode Selection Value on this pin will be latched by the Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL as SDC/SDIO control signal which is used to select 16 bits for advanced features. <i>Note: Power On Setting and also there is a 32-bit mode option. However the 32-bit option does not accomodate the ADM6996I/IX's advanced features.</i> 0_B 16 bits mode, MDC/MDIO timing compatible. |
| | MII_TXD3 | O | 4 mA, PD, LVTTTL | Port 5 Transmit Data Bit 3 in MII Mode Bit[3] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| 66 | PHYAS0 | I | PD, LVTTTL | PHY Address MSB Bit 0 During power on reset, value will be latched by Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL as PHY starts address select. PHYAS[1:0] = 00_B and PHY address starts from 01000_B . <i>Note: Power On Setting</i> |
| | MII_TXEN | O | 8 mA, PD, LVTTTL | Port 5 Transmit Enable TXEN in MII Mode Active high to indicate that the data on MII_TXD[3:0] is valid. Synchronous to the rising edge of MII_TXCLK. |
| | GPSI_TXEN | O | 8 mA, PD, LVTTTL | Port 5 Transmit Enable TXEN in GPSI Mode Active high to indicate that the data on GPSI_TXD is valid. Synchronous to the rising edge of GPSI_TXCLK. |
| | RMII_TXEN | O | 8 mA, PD, LVTTTL | Port 5 R Transmit Enable TXEN in RMII Mode Active high to indicate that the data on RMII_TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN. |

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|------------|----------|-------------|---|
| 74 | MII_RXD0 | I | PD, LVTTTL | Port 5 Receive Data Bit 0 in MII Mode In MII mode, the bit[0] of MII receive data, synchronous to the rising edge of MII_RXCLK. |
| | GPSI_RXD | I | PD, LVTTTL | Port 5 Receive Data in GPSI Mode In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_P5RXCLK. |
| | RMII_RXD0 | I | PD, LVTTTL | Port 5 Receive Data Bit 0 in RMII Mode In RMII mode, bit[0] of RMII receive data, synchronous to the rising edge of REFCLK_IN. |
| 100 | MII_RXD1 | I | PD, LVTTTL | Port 5 Receive Data Bit 1 in MII Mode In MII mode, bit[1] of MII receive data, synchronous to the rising edge of MII_RXCLK. |
| | RMII_RXD1 | I | PD, LVTTTL | Port 5 Receive Data Bit 1 in RMII Mode In RMII mode, bit[1] of RMII receives data, synchronous to the rising edge of REFCLK_IN. |
| 101 | MII_RXD2 | I | PD, LVTTTL | Port 5 Receive Data Bit 2 in MII Mode In MII mode, bit[2] of MII receives data. Synchronous to the rising edge of MII_RXCLK. |
| 102 | MII_RXD3 | I | PD, LVTTTL | Port 5 Receive Data Bit 3 in MII Mode In MII mode, bit[3] of MII receive data. Synchronous to the rising edge of MII_RXCLK. |
| 73 | MII_RXDV | I | PD, LVTTTL | Port 5 Receive Data Valid in MII Mode Active high to indicate that the data on MII_RXD[3:0] is valid. Synchronous to the rising edge of MII_RXCLK. |
| | RMII_CRSDV | I | PD, LVTTTL | Port 5 Carrier Sense and Receive Data Valid in RMII Mode Active high to indicate that the data on RMII_RXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN. |
| 68 | MII_RXER | I | PD, LVTTTL | Port 5 Receive Error in MII Mode Active high to indicate that there is an error on the MII_P5RXD [3:0]. Upon receiving this signal, Samurai-6I (ADM6996I/IX) will send Error Symbol onto the medium. Only valid in 100M operation. |
| | RMII_RXER | I | PD, LVTTTL | Port 5 Receive Error in RMII Mode Active high to indicate that there is error on the RMII_P5 RXD[1:0]. Upon receiving this signal, Samurai-6I/6IX (ADM6996I/IX) will send Error Symbol onto the medium. Only valid in 100M operation. |

Interface Description

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|------------|----------|------------------|--|
| 77 | MII_CRS | I | PD, LVTTTL | Port 5 Carrier Sense in MII Mode In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_P5CRS will be high both in receive and transmit conditions. |
| | GPSI_CRS | I | PD, LVTTTL | Port 5 Carrier Sense in GPSI Mode In full duplex mode, GPSI_P5CRS reflects the receive carrier sense situation only on the medium; In Half Duplex, GPSI_P5CRS will be high both under receive and transmit conditions. |
| 78 | MII_COL | I | PD, LVTTTL | Port 5 Collision Input in MII Mode Active high to indicate that there is collision on the medium. Stays low in full duplex operation. |
| | GPSI_COL | I | PD, LVTTTL | Port 5 Collision Input in GPSI Mode Active high to indicate that there is collision on the medium. Stays low in full duplex operation. |
| 72 | MII_RXCLK | I | PD, LVTTTL | Port 5 Receive Clock Input in MII Mode MII_RXDV and MII_RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25MHz clock in 100M mode and 2.5MHz clock in 10M mode. |
| | GPSI_RXCLK | I | PD, LVTTTL | Port 5 Receive Clock Input in GPSI Mode GPSI_RXD are synchronous to the rising edge of this clock. It is non-continuous 10MHz Clock input. |
| | REFCLK_IN | I | PD, LVTTTL | 50MHz Reference Clock Input in RMII mode RMII_RXD[1:0], RMII_TXD[1:0], RMII_TXEN and RMII_CRSDV are synchronous to the rising edge of this clock. |
| 67 | MII_TXCLK | I | PD, LVTTTL | Port 5 Transmit Clock Input in MII Mode MII_P5TXEN and MII_P5TXD[3:0] are output at the rising edge of this clock. It is free running 25MHz clock in 100M mode and 2.5MHz clock in 10M mode. |
| | GPSI_TXCLK | I | PD, LVTTTL | Port 5 Transmit Clock Input in GPSI Mode GPSI_TXEN and GPSI_TXD are synchronous to the rising edge of this clock. It is a continuous 10MHz Clock input. |
| | REFCLK_OUT | O | 8 mA, PD, LVTTTL | 50MHz Reference Clock Output in RMII mode This pin is used as a 50MHz reference clock signal output pin when port 5 operates in RMII mode. |
| 89 | SPDTNP5 | I | PD, LVTTTL | Port 5 Speed Input 0 _B 100M 1 _B 10M |
| 90 | LNKFP5 | I | PD, LVTTTL | Port 5 Link Fail Status Input 0 _B Link Up 1 _B Link Failed |

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------------------|----------|----------|------------------|---|
| 91 | DPHALFP5 | I | PD, LVTTTL | Port 5 Duplex Status Input 0 _B Full Duplex 1 _B Half Duplex |
| LED Interface | | | | |
| 103 | DUPCOL4 | O | 8 mA, PD, LVTTTL | Port 4 Duplex /Collision LED In Full duplex mode, this pin acts as DUPLEX LED for port 4, respectively; in half duplex mode, it is collision LED for each port. See Chapter 3.1.12 LED Display for more detail. |
| 106 | DUPCOL3 | O | 8 mA, PD, LVTTTL | Port 3 Duplex /Collision LED In Full duplex mode, this pin acts as a DUPLEX LED for port 3, respectively; in half duplex mode, it is the collision LED for each port. See Chapter 3.1.12 LED Display for more detail. |
| 107 | BPEN | I | PU, LVTTTL | Recommended Back-Pressure in Half-Duplex Value on this pin will be latched by Samurai-6I (ADM6996I/IX) during power on reset as the back-pressure enable in half-duplex mode. <i>Note: Power On Setting</i> 0 _B Disable Back-Pressure 1 _B Enable Back-Pressure |
| | DUPCOL2 | O | 8 mA, PU, LVTTTL | Port 2 Duplex-collision LED In Full duplex mode, this pin acts as port 2 DUPLEX LED; in half duplex mode, it is collision LED for port 2. See Chapter 3.1.12 LED Display for more detail. |
| 108 | PHYAS1 | I | PD, LVTTTL | Recommend PHY Address Bit 1 Value on this pin will be latched by Samurai-6I/6IX (ADM6996I/IX) during power on reset as the PHY address recommend value bit 1. See PHYAS0 description for more detail. <i>Note: Power On Setting</i> |
| | DUPCOL1 | O | 8 mA, PD, LVTTTL | Port 1 Duplex-collision LED In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for port 1. See Chapter 3.1.12 LED Display for more detail. |

Interface Description

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|------------------|----------|----------|------------------|---|
| 109 | RECANEN | I | PU, LVTTTL | Recommend Auto Negotiation Enable Only valid for Twisted pair interface. Programming this bit to 1 has no effect on the Fiber port. <i>Note: Power On Setting.</i> 0 _B Disable all TP port auto negotiation capability 1 _B Enable all TP port auto negotiation capability |
| | DUPCOL0 | O | 8 mA, PU, LVTTTL | Port 0 Duplex-collision LED In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is a collision LED for port 0. See Chapter 3.1.12 LED Display for more detail. |
| 92 | LNKACT_4 | O | 8 mA, PD, LVTTTL | LINK/Activity LED of Port 4 to 0 Used to indicate corresponding port's link/activity status, see Chapter 3.1.12 LED Display for more detail. |
| 95 | LNKACT_3 | | | |
| 96 | LNKACT_2 | | | |
| 97 | LNKACT_1 | | | |
| 98 | LNKACT_0 | | | |
| 58 | LDSPD_4 | O | 8 mA, PD, LVTTTL | Port 4 to Port 0 Speed LED Used to indicate corresponding port's speed status, see Chapter 3.1.12 LED Display for more detail. |
| 55 | LDSPD_3 | | | |
| 54 | LDSPD_2 | | | |
| 51 | LDSPD_1 | | | |
| 50 | LDSPD_0 | | | |
| EEPROM Interface | | | | |
| 84 | EDO | I | PU, LVTTTL | EEPROM Data Output This pin is used to input EEPROM data when reading the EEPROM. During Samurai-6I (ADM6996I/IX) initialization, Samurai-6I/6IX (ADM6996I/IX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to the EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See Chapter 3.4.2 EEPROM Interface for more detail. |

Interface Description

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|-------|----------|------------------|--|
| 80 | IFSEL | I | PD, LVTTTL | Interface Selection After Samurai-6I (ADM6996I/IX) initialization process is done, this pin is used to select using the EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0 _B SDC/SDIO interface 1 _B EEPROM interface |
| | EECS | O | 4 mA, PD, LVTTTL | EEPROM Chip Select During Samurai-6I (ADM6996I/IX) initialization, this pin is used as EEPROM chip select signal. During Samurai-6I/6IX (ADM6996I/IX) initialization, Samurai-6I/6IX (ADM6996I/IX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See Chapter 3.4.2 EEPROM Interface for more detail. |
| 81 | XOVEN | I | PD, LVTTTL | Cross Over Enable Value on this pin (active low) will be latched by Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL for port 4~0 crossover auto detect (Only available in TP interface). <i>Note: Power On Setting.</i> 0 _B Disable 1 _B Enable |
| | EESK | I/O | 4 mA, PD, LVTTTL | EEPROM Serial Clock During Samurai-6I/6IX (ADM6996I/IX) initialization, this pin is used to output clock to EEPROM. After Samurai-6I/6IX (ADM6996I/IX) initialization process is done, this pin is used as EEPROM interface clock input if IFSEL = 1. |
| | SDC | I | PD, LVTTTL | Serial Management interface Clock input If IFSEL = 0, this pin is used as serial management interface clock input. SDC timing is the same as MDC when chip set in 16-bit mode. |

Interface Description

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|----------|----------|------------------|--|
| 79 | LED_MODE | I | PD, LVTTTL | Enable Mac to Choose LED Display Mode Value on this pin will be latched by Samurai-6I/6IX (ADM6996I/IX) on the rising edge of RESETL as single/dual color LED mode control signal. See Chapter 3.1.12 LED Display for more detail. <i>Note: Power On Setting.</i> |
| | EDI | I/O | 8 mA, PD, LVTTTL | EEPROM Serial Data Input During Samurai-6I/6IX (ADM6996I/IX) initialization this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if IFSEL = 1. |
| | SDIO | I/O | 8 mA, PD, LVTTTL | Serial Management interface Data input/Output If IFSEL = 0, this pin is used as data input/output pin of serial management interface. SDIO timing is the same as MDIO when chip set in 16 bits mode. |

Power/Ground, 48 Pins

| | | | | |
|-------------------------|---------|-----|---|---|
| 10, 23, 36, 42, 125 | GNDA | GND | – | Ground Used by AD Block |
| 7, 20, 33, 45, 122 | VCCA2 | PWR | – | 1.8 V, Power Used by TX Line Driver |
| 13, 26, 39, 128 | VCCAD | PWR | – | 3.3 V, Power Used by AD Block |
| 119 | GNDBIAS | GND | – | Ground Used by Bias Block |
| 121 | VCCBIAS | PWR | – | 3.3 V, Power Used by Bias Block. |
| 116 | GNDPLL | GND | – | Ground Used by PLL |
| 115 | VCCPLL | PWR | – | 1.8 V, Power Used by PLL |
| 47, 52, 64, 76, 83, 93 | GNDIK | GND | – | Ground Used by Digital Core |
| 48, 53, 75, 82, 94, 110 | VCCIK | PWR | – | 1.8 V, Power Used by Digital Core |
| 46, 57, 70, 87, 99, 104 | GNDO | GND | – | Ground Used by Digital Pad |
| 56, 71, 88, 105 | VCC3O | PWR | – | 3.3 V, Power Used by Digital Pad |

Miscellaneous

Table 3 IO Signals (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|--|-----------|----------|------------------|---|
| 62 | P4FX | I | PD, LVTTTL | Port 4 Fiber Selection During power on reset, value will be latched by Samurai-6I/6IX (ADM6996I/IX) at the rising edge of RESETL as Port 4 Fiber select. 0 _B Twisted Pair Mode 1 _B Fiber Mode |
| 1, 2, 3, 4, 5, 6, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31, 32 | NC | - | - | Not Connected |
| 49 | TEST | I | PD, LVTTTL | Test Mode Reserved and should be kept 0 under normal operation. |
| 86 | CFG0 | I | PU, LVTTTL | Configuration 0 Reserved and should be kept 0 when under normal operation. |
| 69 | WAIT_INIT | I | PD, LVTTTL | Wait Initialization This pin will be used to pause all activities after power up until loading EEPROM is successful and done or CPU initialization is done.. 0 _B pause until loading EEPROM done. 1 _B pause until loading EEPROM successful and done or CPU initialization is done. |
| 65 | INT_N | O | OD, 8 mA | Interrupt Active low interrupt signal to indicate the status change in the interrupt status register. Interrupt signal will be kept active until the host reads the status of the IS register. 0 _B Interrupt 1 _B Not interrupt |
| 85 | CKO25M | O | 8 mA, PD, LVTTTL | 25MHz Clock Output Free Running 25MHz Clock output (Even during power on reset). |
| 112 | RC | I | ST | RC Input For Power On Reset This pin is sampled by using the 25MHz free running clock signal which inputs from XI to generate the low-active reset signal, RESETL. See Chapter 5.3.2 Power On Reset for the timing requirement. |
| 113 | XI | AI | ANA | 25MHz Crystal /Oscillator Input 25MHz Crystal or Oscillator Input. Variation is limited to +/- 50ppm. |
| 114 | XO | AO | ANA | 25M Crystal Output When connected to oscillator, this pin should be left unconnected. |
| 120 | RTX | AI | ANA | Constant Voltage Reference External 1.0 kΩ 1% resistor connection to ground. |

Table 3 **IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|---------|----------|-------------|---|
| 118 | VREF | AI | ANA | Analog Reference Voltage Used by Internal Bias Circuit for voltage reference. External 0.1uF capacitor connection to ground for noise filter. |
| 117 | CONTROL | AI/O | ANA | FET Control Signal The pin is used to control FET for 3.3 V to 1.8 V regulator. External 0.1uF capacitor connection to ground for noise filter, even if the pin is un-connected. |

3 Function Description

3.1 Switch Functional Description

The Samurai-6I/6IX (ADM6996I/IX) uses a “store & forward” switching approach for the following reasons:

1. Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers, especially when bridging between a server on a 100 Mbit/s network and clients on a 10 Mbit/s segment
2. Store & forward switches improve overall network performance by acting as a “network cache”
3. Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port

3.1.1 Basic Operation

The Samurai-6I/6IX (ADM6996I/IX) receives incoming packets from one of its ports, uses the source address (SA) and FID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and FID.

If the DA and FID are not found in the address table, the Samurai-6I/6IX (ADM6996I/IX) treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.

The Samurai-6I/6IX (ADM6996I/IX) can automatically learn the port number of attached network devices together with the SA and FID of all the incoming packets. If the SA and FID are not found in the address table, the Samurai-6I/6IX (ADM6996I/IX) adds it to the table.

3.1.2 Buffers and Queues

The Samurai-6I/6IX (ADM6996I/IX) incorporates 6 transmit queues and receive buffer areas for the 6 Ethernet ports. The receive buffers, as well as the transmit queues, are located within the Samurai-6I/6IX (ADM6996I/IX) along with the switch fabric. The buffers are divided into 192 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

3.1.3 Full Duplex Flow Control

When a full duplex port runs out of its receive buffers, a PAUSE command will be issued by Samurai-6I/6IX (ADM6996I/IX) to notify the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When the flow control hardware pin (**GFCE**) is set to high, during power on reset, and per port PAUSE is enabled, Samurai-6I/6IX (ADM6996I/IX) will output and accept 802.3x flow control packets.

3.1.4 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation. When the Samurai-6I/6IX (ADM6996I/IX) cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

3.1.5 Back-Off Algorithm

The Samurai-6I/6IX (ADM6996I/IX) implements the truncated exponential back off algorithm compliant to the 802.3 standard. Samurai-6I/6IX (ADM6996I/IX) will restart the back off algorithm by choosing 0-9 collision count. After 16 consecutive retransmit trials, the Samurai-6I/6IX (ADM6996I/IX) resets the collision counter. Users can set the Back Off (see 0010_H, **BD**) to disable this function.

3.1.6 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6 μ s for 10 Mbit/s Ethernet and 960 ns for 100 Mbit/s fast Ethernet. For the receive end, Samurai-6I/6IX (ADM6996I/IX) is designed to be able to tolerate IPG gaps greater than 64 bits. For the transmit end, Samurai-6I/6IX (ADM6996I/IX) will always transmit packets with the minimum IPG gap equal to 96 bits. If users want to shorten the transmission IPG gap, they can enable the Short IPG function (see 000B_H, [TSIE](#)). Then Samurai-6I/6IX (ADM6996I/IX) will instruct its output MAC to transmit packets with IPG equal to 88 bits and 96 bits in order.

3.1.7 Trunking Function

Samurai-6I/6IX (ADM6996I/IX) supports only one trunking group. If Port 3 and Port 4 Trunk (see 000B_H, [TE](#)) the function is enabled, Samurai-6I/6IX (ADM6996I/IX) will see Port 3 and Port 4 as the same port to make the bandwidth equal to 200M. When any of these two ports link fail, the Samurai-6I/6IX (ADM6996I/IX) will automatically change the transmit path from the failed link to link good port. Output port based load balancing is implemented in Samurai-6I/6IX (ADM6996I/IX), so users don't set anything.

3.1.8 Illegal Frames

The Samurai-6I/6IX (ADM6996I/IX) will discard all illegal packets. These packets are

1. Undersize packets: The packets received with a length of less than 64 bytes are discarded
2. Oversize packets: The packets received with a length of more than "MAXPKTLEN" bytes are discarded. See (0011_H, [MPL](#)) to see how to decide the MAXPKTLEN value
3. CRC packets: The packets received with a wrong FCS value are discarded
4. Symbol error packets: The packets received with symbol error are discarded
5. Source violation packets: The packets received with a source violation could be discarded in some cases. See ([Source Violation](#)) description.
6. VLAN violation packets: The frames received with a VLAN violation can be discarded in some cases. See ([VLAN Violation](#)) description

3.1.9 Broadcast/Multicast Storm

Samurai-6I/6IX (ADM6996I/IX) allows users to limit the traffic of the broadcast address (DA = FFFFFFFF_H) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets (DA[40] = 1_B), they can set the Multicast Packet Counted into Storming Counter (see 0010_H, [MP](#)) function. Two thresholds and storm enable bits (see 003B_H and 003C_H, [STORM_EN](#), [STORM_100_TH](#), [STORM_10_TH](#)) are used to control the broadcast storm.

1. Time Scale. Samurai-6I/6IX (ADM6996I/IX) uses 50ms as a scale to meter the storm packets.

| Parameter | Rising Threshold | Falling Threshold |
|---------------------------------|---|--------------------|
| All link ports are 100M | 100M Threshold (See 003B _H) | 1/2 100M Threshold |
| All link ports are not all 100M | 10M Threshold (See 003C _H) | 1/2 10M Threshold |

2. Storm keeps on at least 1.6 seconds if any of the ports meets the rising threshold in the 4 consecutive 50 ms intervals. In these 1.6 seconds, the ports meeting the rising threshold will start to discard the broadcast or multicast packets until the 50 ms interval expires. Users could also disable Input Filter (see 000B_H, [IF](#)) function to forward above packets to the un-congested port instead of discarding directly.

3. Storm finishes. After the 1.6-second storm period, Samurai-6I/6IX (ADM6996I/IX) will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50 ms intervals and no other ports satisfy the rising threshold at the same time, the storm will finish.

3.1.10 Bandwidth Control

Samurai-6I/6IX (ADM6996I/IX) supports hardware-based bandwidth control for both ingress and egress traffic. Ingress and egress rate can be limited independently on each port base. The Samurai-6I/6IX (ADM6996I/IX) provides several timer scales corresponding to different the bandwidth control unit, so users can configure the rate equal to $K * (\text{Bandwidth Step})$, $1 \leq K \leq 2048$. Different timer scales can optimize the QoS performance by different bandwidth control unit. Samurai-6I/6IX (ADM6996I/IX) maintains two counters (input and output) for each port. For example, if users want to limit rate equal to 64 kbit/s, they should configure the bandwidth control threshold equal to 1. At each time unit, Samurai-6I/6IX (ADM6996I/IX) will add 64 to the counter and decrease the byte length when receiving a packet in this period. When the counter is decreased to zero, we can divide the control behavior into two parts:

For the ingress control, the ingress port will not receive packets any more. If flow control is enabled, Pause packets will be transmitted, if Back Pressure is enabled, Jam packets will be transmitted, and if the above functions are not enabled, the packets will be discarded.

For the egress control, the egress port will not transmit any packets, so the egress bandwidth is controlled.

Samurai-6I/6IX (ADM6996I/IX) allows users to control the ingress and egress bandwidth at the same time (see 0033_H, [Bandwidth Control Enable Register](#)).

For Example, set P0 receive bandwidth control to 6 Mbit/s.

1. Set the receive bandwidth of P0. $N = \{R0BW_TH3, R0BW_TH2, R0BW_TH1, R0BW_TH0, 6'b0\} = 0x005e$
2. Enable P0 receive bandwidth control. Set 0033_H[0]=1

Table 4 Bandwidth Control Timer Select

| [10:9]0029 _H | Timer Scale | Bandwidth Step | Applied Range |
|-------------------------|-------------|----------------|-----------------|
| 00 | 8ms | 64Kbps | 64Kbps~2.2Mbps |
| 01 | 1ms | 512Kbps | 512Kbps~18Mbps |
| 10 | 40us | 200Kbps | 200Kbps~100Mbps |
| 11 | 500us | 16Kbps | 16Kbps~32Mbps |

3.1.11 Smart Discard

The Samurai-6I/6IX (ADM6996I/IX) supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

Table 5 Smart Disacrd

| Queue | Discard Mode |
|---------|--|
| Queue 3 | Discard Mode of Queue 3 in 0010 _H [15:14] |
| Queue 2 | Discard Mode of Queue 2 in 0010 _H [13:12] |
| Queue 1 | Discard Mode of Queue 1 in 0010 _H [11:10] |
| Queue 0 | Discard Mode of Queue 0 in 0010 _H [9:8] |

Table 6 Discard Ratio

| Discard Mode | 00 | 01 | 10 | 11 |
|----------------|----|-----|-----|-----|
| Utilization 00 | 0% | 0% | 0% | 0% |
| Utilization 01 | 0% | 0% | 25% | 50% |
| Utilization 11 | 0% | 25% | 50% | 75% |

3.1.12 LED Display

Three LEDs per port are provided by Samurai-6I/6IX (ADM6996I/IX): Link/Act, Duplex/Col and Speed. The dual-color LED mode is also supported by Samurai-6I/6IX (ADM6996I/IX). For ease of production purposes, the test signal is sent to each LED at power on reset stage. The LED display mode is controlled by:

1. **DUAL-COLOR-EE** (see 0012_H): It is an EEPROM register to control the dual or single color mode. It is useless when the value (wait_init) on the pin **WAIT_INIT** is low.
2. **LED_MODE**: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value wait_init is high.
3. **LED-ENABLE** (see 0012_H): When CPU is attached and this CPU has no ability to pull the EDI to high or low, users can set the wait_init to high to delay the LED test, write the correct value to the **DUAL-COLOR-EE**, write 1_B into register **LED-ENABLE**, and then the LED test starts.
4. **DUP_COL_SEP** (see 0012_H): Dupcol LEDs indicate the duplex status only.
5. **DHCOL_LED_EN** (See 0030_H): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

3.1.12.1 Single Color LED Display

Table 7 Single Color LED Display

| Pin Name | Status |
|---|---|
| LNKACT4/LNKACT3/ LNKACT2/LNKACT1/ LNKACT0 | <p>These pins have no power on reset values on them, and Samurai-6I/6IX (ADM6996I/IX) uses active low value to drive the LED. So the output values of these pins after the power on reset are shown as follows:</p> <ol style="list-style-type: none"> 1. First period: This period lasts 1.28s for LED on test. Samurai-6I/6IX (ADM6996I/IX) drives value 0 to open the LED. 2. Second period: This period lasts 0.48s for LED off test. Samurai-6I/6IX (ADM6996I/IX) drives value 1 to close the LED. 3. Normal Period: This period indicates the link status. <p>0_B Port links up and LED is ON. 1_B Port links down and LED is OFF. 0/1_B Port links up and is transmitting or receiving. The LED flashes at 10 Hz.</p> |
| LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0 | <p>The behavior of these pins is the same as the LNKACT, except during normal period.</p> <p>Normal period: This period indicates the speed status.</p> <p>0_B Port links up and its speed is 100M. LED is ON. 1_B Port links down or its speed is 10M. LED is OFF.</p> |

Table 7 **Single Color LED Display (cont'd)**

| Pin Name | Status |
|---------------------------------|---|
| DUPCOL2/ DUPCOL1/ DUPCOL0 | <p>These 3 pins have power on reset values on them. Samurai-6I/6IX (ADM6996I/IX) needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows:</p> <ol style="list-style-type: none"> 1. First period: This period lasts 1.28s for LED on test. Samurai-6I/6IX (ADM6996I/IX) drives ~value_power_on to open the LED. 2. Second period: This period lasts 0.48s for LED off test. Samurai-6I/6IX (ADM6996I/IX) drives value_power_on to close the LED. 3. Normal Period: This period indicates the duplex/collision status. <p>~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED flashes at 10 Hz. 0/1_B Port links up and collision is detected. The LED flashes at 10 Hz. If DUP_COL_SEP is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1_B This value is cancelled. LED doesn't blink. If DHCOL_LED_EN is enabled, the display in the normal period is as follows: DUPCOL0: 10m collision indicator. 0/1_B One of the ports links up in 10M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = When the above event is not satisfied, the LED is OFF. DUPCOL1: 100 m collision indicator. 0/1_B One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = The above event is not satisfied. LED is OFF.</p> |
| DUPCOL4/ DUPCOL3 | <p>The behavior of these pins is the same as the LNKACT, except during normal period.</p> <p>Normal period: This period indicates the duplex/collision status.</p> <p>~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF. 0/1_B Port links up and collision is detected. The LED flashes at 10 Hz. If DUP_COL_SEP is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1_B This value is cancelled. LED doesn't blink.</p> |

3.1.12.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

Table 8 Dual Color LED Display

| Pin Name | Status |
|--|---|
| (LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACT2, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0) | <p>First Period: Test LED on with green color. It lasts 1.28 s. 01_B LED is on with green color.</p> <p>Second Period: Test LED on with yellow color. It lasts 1.28 s. 10_B LED is on with yellow color.</p> <p>Third period: Test LED off. 00_B LED is off.</p> <p>Normal Period: This period shows the status of the link and speed at the same time.</p> <p>00_B Port links down. LED is off.</p> <p>11_B Port links down. LED is off.</p> <p>01_B Port links up in 100M. LED glows green.</p> <p>10_B Port links up in 10M. LED glows yellow.</p> <p>0/1,1_B Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10 Hz.</p> <p>0/1,0_B Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10 Hz.</p> |
| DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0 | The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56 s instead of 1.28 s. |

3.1.12.3 Circuit for Single LED Mode

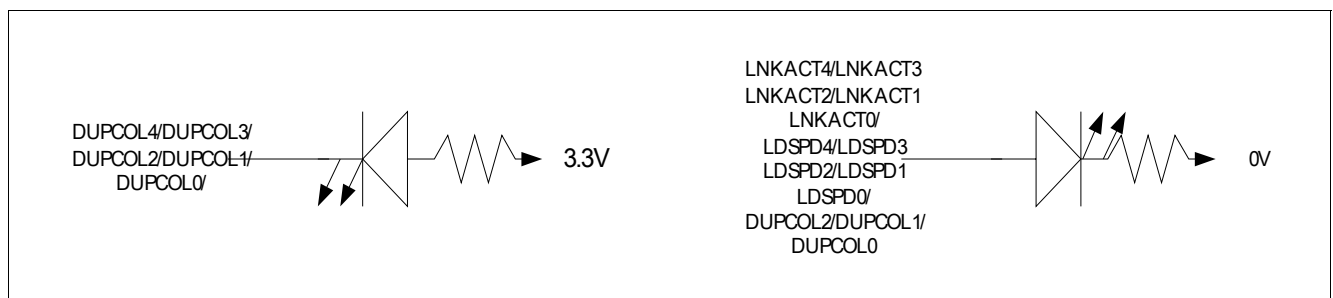


Figure 3 Circuit for Single Color LED Mode

3.1.12.4 Circuit for Dual LED Mode

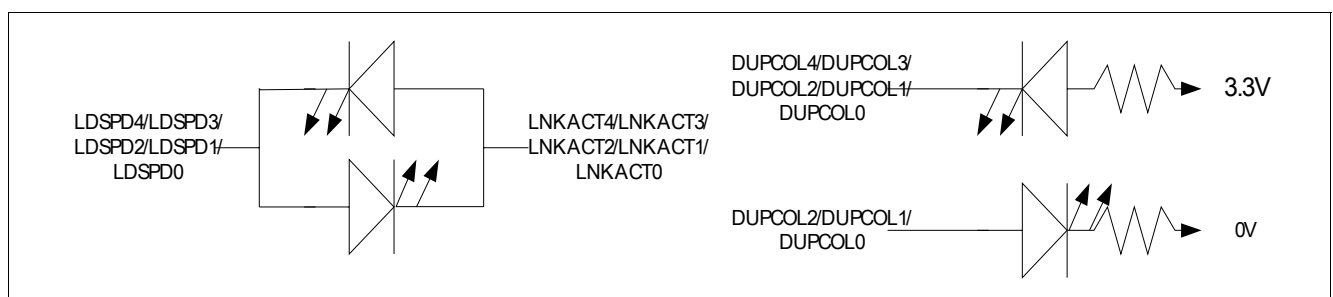


Figure 4 Circuit for Dual Color LED Mode

3.1.13 Packet Identification

Packets are classified to determine if they should be passed to the CPU port or another entity for special handling.

Table 9 Packet Identification

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | | Comments |
|--|----------|--|
| BPDU | | The Ethernet destination address is 01 80 C2 00 00 00 _H . |
| PAUSE | | The Ethernet destination address is 01 80 C2 00 00 01 _H . Ether-Type field is 8808 _H . OPCODE is 0001 _H . |
| SLOW | | The Ethernet destination address is 01 80 C2 00 00 02 _H . |
| PAE | | The Ethernet destination address is 01 80 C2 00 00 03 _H . |
| RESER_R0 | | The Ethernet destination address ranges between 01 80 C2 00 00 04 _H and 01 80 C2 00 00 0F _H . |
| RESER_R1 | | The Ethernet destination address ranges between 01 80 C2 00 00 10 _H and 01 80 C2 00 00 1F _H . |
| GXRP | | The Ethernet destination address ranges between 01 80 C2 00 00 20 _H and 01 80 C2 00 00 22 _H . |
| RESER_R2 | | The Ethernet destination address ranges between 01 80 C2 00 00 23 _H and 01 80 C2 00 00 2F _H . |
| RESER_R3 | | The Ethernet destination address ranges between 01 80 C2 00 00 30 _H and 01 80 C2 00 00 FF _H . |
| RARP | | The Ethernet destination address is FF FF FF FF FF FF _H and the Ether-Type field is 8035 _H . |
| ARP | | The Ethernet destination address is FF FF FF FF FF FF _H and the Ether-Type field is 8036 _H . |
| IGMP_IP | | The Ethernet destination address is 01 00 5E xx xx xx _H . Ether-Type field is 0800 _H (IP). IP Version is 4 and the Protocol field is 02 _H (IGMP). |
| MLD_IP | | Ethernet destination address is 33 33 xx xx xx xx _H . The Ether-Type field is 0800 _H (IP). IP Version is 6 and the Protocol field is 3A _H (ICMP). |
| MLD_IPV6 | | Ethernet destination address is 33 33 xx xx xx xx _H . The Ether-Type field is 86DD _H (IP). IP Version is 6 and the Protocol field is 3A _H (ICMP). |
| Others | TYPE | The Ether-Type field matches one of the type filters. |
| | PROTOCOL | The Protocol field matches one of the protocol filters. |
| | TCPUDP | The TCP/UDP port number matches one of the TCP/UDP filters. |
| | MAC_CTRL | The Ether-Type field is 8808 _H , but OPCODE is not 0001 _H . |

For learning purpose, Samurai-6I/6IX (ADM6996I/IX) sometimes divide Ethernet address into three groups.

Table 10 Packet Identification Groups

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | | Comments |
|--|--|--|
| MULTICAST | | The first bit of the Ethernet destination address is 1, but not all 1. |
| BROADCAST | | The Ethernet destination address is FF FF FF FF FF FF _H . |
| UNICAST | | The first bit of the Ethernet destination address is 0. |

3.1.13.1 Span Packet

Samurai-6I/6IX (ADM6996I/IX) supports 4 Spanning Tree Port State (Disable, Blocking/Listening, Learning and Forwarding state) for every port to enable Spanning Tree Protocol functions when co-operating with an external CPU. These port states are defined in **STPS** of EEPROM register 0013_H ~ 0018_H.

Samurai-6I/6IX (ADM6996I/IX) supports a function to specify a packet to be treated as a Span Packet. Besides the Disable state, the Span Packets will not be dropped by Spanning Tree Port State settings.

Table 11 Span Packet

| Packet Type | Description |
|---|--|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit defined in the learning table when there is a match for DA+FID. 3. Span bit defined in the control table when there is a match for DA. 4. Span bit in register 003E _H . |
| ARP/RARP | The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit in register 000D _H . |
| IGMP_IP/MLD_IP/MLD_IPV6 | The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit in register 000C _H . |
| Others | The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-span packets. |

3.1.13.2 Management Packet

Samurai-6I/6IX (ADM6996I/IX) reserves some buffers for Management packets, so they are not dropped because of traffic congestion. Management packets are never limited by the bandwidth control, stormed by the storming control, or dropped due to **Smart Discard** function.

Table 12 Management Packet

| Packet Type | Description |
|---|--|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit defined in the learning table when there is a match for DA+FID. 3. Management bit defined in the control table when there is a match for DA. 4. Management bit in register 003E _H . |
| ARP/RARP | The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit in register 000D _H . |

Function Description

Table 12 Management Packet (cont'd)

| Packet Type | Description |
|-------------------------|--|
| IGMP_IP/MLD_IP/MLD_IPV6 | The management packet is determined in priority order by: <ol style="list-style-type: none"> 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit in register 000C_H. |
| Others | The management packet is determined in priority order by: <ol style="list-style-type: none"> 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit defined in the learning table when there is a match for DA+FID.If the first and second conditions are not satisfied, the frame is classified as non-management packets. |

3.1.13.3 Cross_VLAN Packet

Cross-VLAN packets are defined to cross VLAN boundary or bypass the VLAN violation.

Table 13 Cross_VLAN Packet

| Packet Type | Description |
|--|---|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | The cross-VLAN packet is determined in priority order by: <ol style="list-style-type: none"> 1. Cross_VALN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID. 3. Cross_VLAN bit defined in the control table when there is a match for DA. 4. Cross_VLAN bit in register 003E_H. |
| ARP/RARP | The cross_VLAN packet is determined in priority order by: <ol style="list-style-type: none"> 1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross-VLAN bit in register 000D_H. |
| IGMP_IP/MLD_IP/MLD_IPV6 | The cross_VLAN packet is determined in priority order by: <ol style="list-style-type: none"> 1. Cross-VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross-VLAN bit in register 000C_H. |
| Others | The Cross_VLAN packet is determined in priority order by: <ol style="list-style-type: none"> 1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID.If the first and second conditions are not satisfied, the frame is classified as non-cross_VLAN packets. |

3.1.14 Tagged VLAN or Port VLAN

The difference between two VLAN rules allows searching of the VLAN boundary. Users can enable the “TAG Based VLAN” (see 0011_H, [TBV](#)) bit to instruct Samurai-6I/6IX (ADM6996I/IX) to operate in the Tagged VLAN mode.

3.1.14.1 VLAN Filters

Samurai-6I/6IX (ADM6996I/IX) supports 16 VLAN filters, each specifying a Valid bit, a TAG PRI, a VID, a FID, a Tagged Member, and a Member.

Table 14 VLAN Filters

| VLAN Filter 0 | VLAN_Valid | VLAN_PRI[2:0] | VID[11:0] | FID[3:0] | Tagged Member[5:0] | Member[5:0] |
|----------------|------------|---------------|-----------|----------|--------------------|-------------|
| ~ | | | | | | |
| VLAN Filter 15 | | | | | | |

3.1.14.2 Port VLAN

Port VLANs are created by grouping individual physical ports together. In this mode, only 6 VLAN filters (VLAN filter 0 ~5) are used. During the time examining the received frame, the source port is used as an index to search the VLAN filter. If the source port is port 0, then Member in the filter 0 is the VLAN group that port 0 joins.

3.1.14.3 Tagged VLAN

Tagged VLAN is created with the aids of the VID in the packet or VID assigned by the source port. This VID is compared with 16 VIDs in the VLAN filters to check if any match exists. The Member in this matched filter is the VLAN boundary for the packet.

3.1.14.4 VID for Comparison and Carried through Samurai-6I/6IX (ADM6996I/IX)

VID for comparison and carried through Samurai-6I/6IX (ADM6996I/IX) (as egress VID) depends on the VLAN configuration.

VID0: The incoming packet is tagged with VID = 000_H. Enable “Replace VID0” (see 000A_H, [RVID0](#)) to replace the Null VID with PVID (see basic control registers) if necessary.

VID1: The incoming packet is tagged with VID = 001_H. Enable “Replace VID1” (see 000A_H, [RVID1](#)) to replace VID1 with PVID (see basic control registers) if necessary.

VIDFFF: The incoming packet is tagged with VID = FFF_H. Enable “Replace VIDFFF” (see 000A_H, [RVIDFFF](#)) to replace VIDFFF with PVID (see basic control registers) if necessary.

VLAN Security Samurai-6I/6IX (ADM6996I/IX) ignores a packet’s VID and always uses PVID to see if there is a match and transfers it to the output ports. Disable the “VLAN Security Disable” (See 0022_H, [VSD](#)) to achieve this goal.

Input Force No Tag When enabled (see 0020_H, [IFNTE](#)), Samurai-6I/6IX (ADM6996I/IX) assumes all the packets are untagged and PVID is used. Input Force No Tag and VLAN Security are different in some situations.

Table 15 VID Comparison

| Parameter | Tagged Frame with VID = 12'hfff | Packet Transmitted Tagged |
|---------------------------|--|--|
| VLAN Security | The frame is recorded as a VLAN violation and discarded if VIDFFF is not replaced. | Output packets have only one VLAN tag. |
| Input Force No Tag | The frame is recognized as an untagged frame. PVID is carried with this packet to the output port. | Output packets may have double tags, because the packet is transmitted with an additional tag with PVID. |

3.1.14.5 Admit Only VLAN-Tagged Packets

Samurai-6I/6IX (ADM6996I/IX) supports a function to check if the packet is VLAN-Tagged, and any packets received on that port that carries no VID (untagged packets or packets with VID = 0) are discarded and recorded as a VLAN violation. This feature is implemented by programming the “Admit Only VLAN-Tagged” (see 0027_H, [AOVTP](#)).

Samurai-6I/6IX (ADM6996I/IX) assumes all the packets are untagged in the “Input Force No Tag” mode and users should care that in this situation, “Admit Only VLAN Tagged” is of no effect.

3.1.14.6 VID Check

In Tagged VLAN, the VID for comparison must be contained in the VLAN filters, or the packet received on the port will be dropped and recorded as a VLAN violation. This feature is disabled by programming the “VID CHECK” bit to 0 (see 0026_H, [VC](#)) to forward these packets instead of dropping them.

3.1.14.7 FID and VLAN Boundary

In Samurai-6I/IX (ADM6996I/IX), every incoming packet is associated with an FID group. Samurai-6I/IX (ADM6996I/IX) searches the learning table for the FID + DA, FID + SA. VLAN boundary restricts the allowable destination ports.

Table 16 FID Search Algorithm

| | | | |
|-------------|--|---|--|
| Port VLAN | The source port number is the VLAN filter index. We can find FID in this filter. | | |
| Tagged VLAN | VID match | Fid is contained in the matched filter. We can find FID in this filter. | |
| | VID un-match | VID check | The frame is dropped. |
| | | VID uncheck | Default FID is the FID (see 000A _H , DFID). If users configure Samurai-6I/IX (ADM6996I/IX) back to port VLAN (see 0027 _H , BPV), we can find the FID in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~15 are for VID comparison. |

Table 17 VLAN Boundary Search Algorithm

| | | | |
|-------------|---|--|---|
| Port VLAN | The source port number is the VLAN filter index. We can find the boundary in this filter. | | |
| Tagged VLAN | VID match | Member is contained in the matched filter. We can find the boundary in this filter | |
| | VID un-match | VID check | The frame is dropped. |
| | | VID uncheck | Samurai-6I/IX (ADM6996I/IX) uses Default VLAN Portmap as the boundary (see 003A _H , DVM). If users configure Samurai-6I/IX (ADM6996I/IX) to “Back to Port VLAN” (see 0027 _H , BPV), boundary can be found in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~15 are for VID comparison. |

3.1.14.8 Ingress Filter

If the source port is not contained in the VLAN boundary associated with the incoming packet, then this frame is dropped and recorded as a VLAN violation. This feature is disabled by setting the “Ingress Filter” (see 0021_H, [IFE](#)) bit to 0_B.

3.1.14.9 VLAN Violation

When packets are recorded as a VLAN violation packet, Samurai-6I/IX (ADM6996I/IX) will drop them. The only way to ignore these violations is to classify these packets as cross_VLAN packets.

3.1.14.10 TXTAG Carried through Samurai-6I/IX (ADM6996I/IX)

Each packet during receive is assigned a 2-bit TXTAG value. This value is carried by Samurai-6I/IX (ADM6996I/IX) to the output ports to help to determine if egress tagged is necessary.

Table 18 **TXTAG Carried through Samurai-6I/6IX (ADM6996I/IX)**

| Packet Type | Description |
|--|--|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG in the learning table when there is a match for DA+FID in the learning table. 3. TXTAG in the control table when there is a match for DA in the control table. 4. TXTAG defined in register 003E _H . |
| ARP/RARP | The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 000D _H . |
| IGMP_IP/MLD_IP/MLD_IPV6 | The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 000C _H . |
| Other | The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. The DA + FID matches an entry in the learning table with TXTAG defined. If the first and second conditions are not satisfied, TXTAG is 2'b00. |

3.1.14.11 Tagged Member Carried through Samurai-6I/6IX (ADM6996I/IX)

If the output port is a tagged port it is determined by the port or the VID. Ports in the tagged members should egress packets tagged.

First Way: New Transmit Tag Disable (see 0x000ah)

The “Output Packet Tagging” bit in the basic control registers determines the tagged members.

Second Way: New Transmit Tag Enable (see 0x000ah)

| | | | |
|-------------|--|--|--|
| Port VLAN | The source port number is the VLAN filter index. We can find the tagged member in this filter. | | |
| Tagged VLAN | VID match | Tagged members are contained in the matched VLAN filter. We can find the tagged members in this filter | |
| | VID un-match | VID check | The frame is dropped. |
| | | VID uncheck | Samurai-6I/6IX (ADM6996I/IX) uses the first way to determine the tagged members. If users configure Samurai-6I/6IX (ADM6996I/IX) to “Back to Port VLAN” (see 0027 _H , BPV), we can back to find the tagged members in the same way as the Port VLAN. |

Users should note that when the Special Tag with Tagged Member Valid = 1_B is incoming, the Samurai-6I/6IX (ADM6996I/IX) always uses Tagged Member in the Special Tag as the Tagged Member.

3.1.14.12 Egress Tag Rule

On the receiving port, Samurai-6I/6IX (ADM6996I/IX) will attach each packet with the tagged members by the Ingress rule. When the packet reaches the destination port, Samurai-6I/6IX (ADM6996I/IX) will check if the destination port is a tagged member, if yes, the packet will be transmitted tagged.

Function Description

Table 19 Egress Tag Result

| | | |
|---|--|---|
| Untagged packets are received (If Input Force No Tag is enabled, Samurai-6I/6IX (ADM6996I/IX) assumes all the received packets are untagged.) | Output port is in the tagged members carried with the packet. | TXTAG Description 00 _B System Default Tag. Packets are transmitted tagged. 01 _B Unmodified. Packets are transmitted untagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |
| | Output port is not in the tagged members carried with the packet. | TXTAG Description 00 _B System Default Tag. Packets are transmitted untagged. 01 _B Unmodified. Packets are transmitted untagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |
| | Output port is configured to operate in the bypass mode. See 002A _H . | TXTAG Description 00 _B System Default Tag. Packets are transmitted untagged. 01 _B Unmodified. Packets are transmitted untagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |
| Tagged packets are received. | Output port is in the tagged members carried with the packet. | TXTAG Description 00 _B System Default Tag. Packets are transmitted tagged. 01 _B Unmodified. Packets are transmitted tagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |
| | Output port is not in the tagged members carried with the packet. | TXTAG Description 00 _B System Default Tag. Packets are transmitted untagged. 01 _B Unmodified. Packets are transmitted tagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |
| | Output port is configured to operate in the bypass mode. See 002A _H . | TXTAG Description 00 _B System Default Tag. Packets are transmitted tagged. 01 _B Unmodified. Packets are transmitted tagged. 10 _B Always Tagged. Packets are transmitted tagged. 11 _B Always Untagged. Packets are transmitted untagged. |

3.1.14.13 Tagged PRI Carried through Samurai-6I/6IX (ADM6996I/IX)

Table 20 Tagged PRI Carried

| | | | |
|---|-------------|---|---|
| Untagged packets are received (If Input Force No Tag is enabled, Samurai-6I/6IX (ADM6996I/IX) assumes all the received packets are untagged.) | Port VLAN | [Change Priority Enable, Change Rule] (see 000A _H , PCE&PCR) 0x _B Reverse PRI. 10 _B VLAN_PRI field in the matched VLAN filter. 11 _B Reverse PRI | |
| | Tagged VLAN | VID unmatch | Reverse PRI |
| | | VID match | [Change Priority Enable, Change Rule] (see 000A _H , PCE&PCR) 0x _B Reverse PRI. 10 _B VLAN_PRI field in the matched VLAN filter. 11 _B Reverse PRI |
| | | | |
| Tagged packets are received. | Port VLAN | [Change Priority Enable, Change Rule] (see 000A _H , PCE&PCR) 0x _B Tagged PRI = The 3-bit user priority in the tag header. 10 _B VLAN_PRI field in the matched VLAN filter. 11 _B Reverse PRI | |
| | Tagged VLAN | VID un-match | Change Priority Enable (see 000A _H , PCE) 0 _B Tagged PRI = The 3-bit user priority in the tag header. 1 _B Reverse PRI. |
| | | VID match | [Change Priority Enable, Change Rule] (see 000A _H , PCE&PCR) 0x _B Tagged PRI = The 3-bit user priority in the tag header. 10 _B VLAN_PRI field in the matched VLAN filter. 11 _B Reverse PRI |
| | | | |

Reverse PRI is reversed from the priority queue the packet is switched through.

Compare = {queue, queue, queue, queue, queue, queue, queue, queue} XOR VLAN Priority MAP in 000E_H.

Then we get Tagged PRI.

Compare Tagged PRI

XXXX_XXX0_B = 000_B

XXXX_XX01_B = 001_B

XXXX_X011_B = 010_B

XXXX_0111_B = 011_B

XXX0_1111_B = 100_B

XX01_1111_B = 101_B

X011_1111_B = 110_B

0111_1111_B = 111_B

1111_1111_B = 000_B

3.1.14.14 CFI Carried through Samurai-6I/6IX (ADM6996I/IX)

Table 21 CFI Carried

| CFI Carried | |
|--|---|
| Untagged frames received (If Input Force No Tag is enabled, Samurai-6I/6IX (ADM6996I/IX) assumes all the received packets are untagged.) | CFI Carried = 0 _B |
| Tagged frame received | CFI Carried = Original CFI in the tag header. |

3.1.14.15 Egress TAG

Egress tag contains Egress PRI, Egress CFI, and Egress VID. When packets are transmitted tagged, this egress tag associated with Ethernet-Type = 8100_H is inserted following the Ethernet source address.

Egress PRI: Egress PRI is Tagged PRI carried through Samurai-6I/6IX (ADM6996I/IX) from the source port.

Egress CFI: Egress CFI is CFI carried through Samurai-6I/6IX (ADM6996I/IX) from the source port.

Egress VID: Egress VID is VID carried through Samurai-6I/6IX (ADM6996I/IX) from the source port.

3.1.15 Priority Queue

Samurai-6I/6IX (ADM6996I/IX) supports 4 priority queues and each is assigned a weight.

Table 22 Priority Queue

| Queue | Weight |
|---------|---|
| Queue 0 | Weight = 1 |
| Queue 1 | Weight = "Queue 1 Weight" bits in 0025 _H |
| Queue 2 | Weight = "Queue 2 Weight" bits in 0026 _H |
| Queue 3 | Weight = "Queue 3 Weight" bits in 0027 _H |

3.1.15.1 System PRI

The system PRI is determined in the order as follows:

1. (DA+FID) was found in the learning table, then LRN_PRI field (when LRN_PRIEN is set) in this entry indicates the priority queue.
2. Port PRI in basic control register indicates the priority queue, when Port_PRIEN is enabled on that port.
3. The user priority field in the tag header is used for a tagged packet ("Input Force No Tag" doesn't effect Samurai-6I/6IX (ADM6996I/IX) to extract the PRI in the tag header), when "VLAN Priority" is enabled. The user priority in the tag header is a 3-bits field, Samurai-6I/6IX (ADM6996I/IX) uses "VLAN Priority MAP" to map the priority queue.
4. For IP packets with no tag header, IP PRI is used when "Service Priority" (see 001F_H) is enabled. Even for a tagged packet with IP header, we can set "IP over VLAN" (see basic control registers) bit to 1 to force using IP PRI. Three kinds of IP PRI are available.
 - a) For IPV6 packets with IP Version = 6_H, the most significant 6 bits of the traffic class in the IPV6 header is used to map the priority queue by the service mapping registers.
 - b) For IPV4 packets with IP Version = 4_H, the most significant 3 bits of the TOS field in the IPV4 header is used to map the priority queue by the TOS Priority Map register.
 - c) If "TOS Using" (see 000A_H) is disabled, even for IPV4 packets, Samurai-6I/6IX (ADM6996I/IX) uses the most significant 6 bits of the TOS field to map the priority queue by the service mapping registers.
5. If the packet matches the TCP/UDP filters, the PRI associated with this filter indicates the priority queue when "TCP/UDP PRIEN" is set to 1 (see 0098_H). Users could enable "TCPUDP over IP" to force using the TCPUDP PRI when there is a match.

3.1.15.2 Queue Assigned

Table 23 Queue Assigned

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | The Order of Priority Assigned |
|--|--|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | <ol style="list-style-type: none"> 1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. If (DA+FID) matches an entry in the learning table, then LRN_PRI field with LRN_PRIEN enabled in this entry indicates the priority queue. 3. Use PRI in 003D_H to indicate the queue the frame was switched. |
| ARP/RARP | <ol style="list-style-type: none"> 1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use PRI in 000D_H to indicate the priority queue when enabled. 3. Use System PRI. |
| IGMP_IP/MLD_IP/MLD_IPV6 | <ol style="list-style-type: none"> 1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use PRI in 000C_H to indicate the priority queue when enabled. 3. Use System PRI. |
| Others | <ol style="list-style-type: none"> 1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use System PRI. |

3.1.15.3 Configure Samurai QoS Function

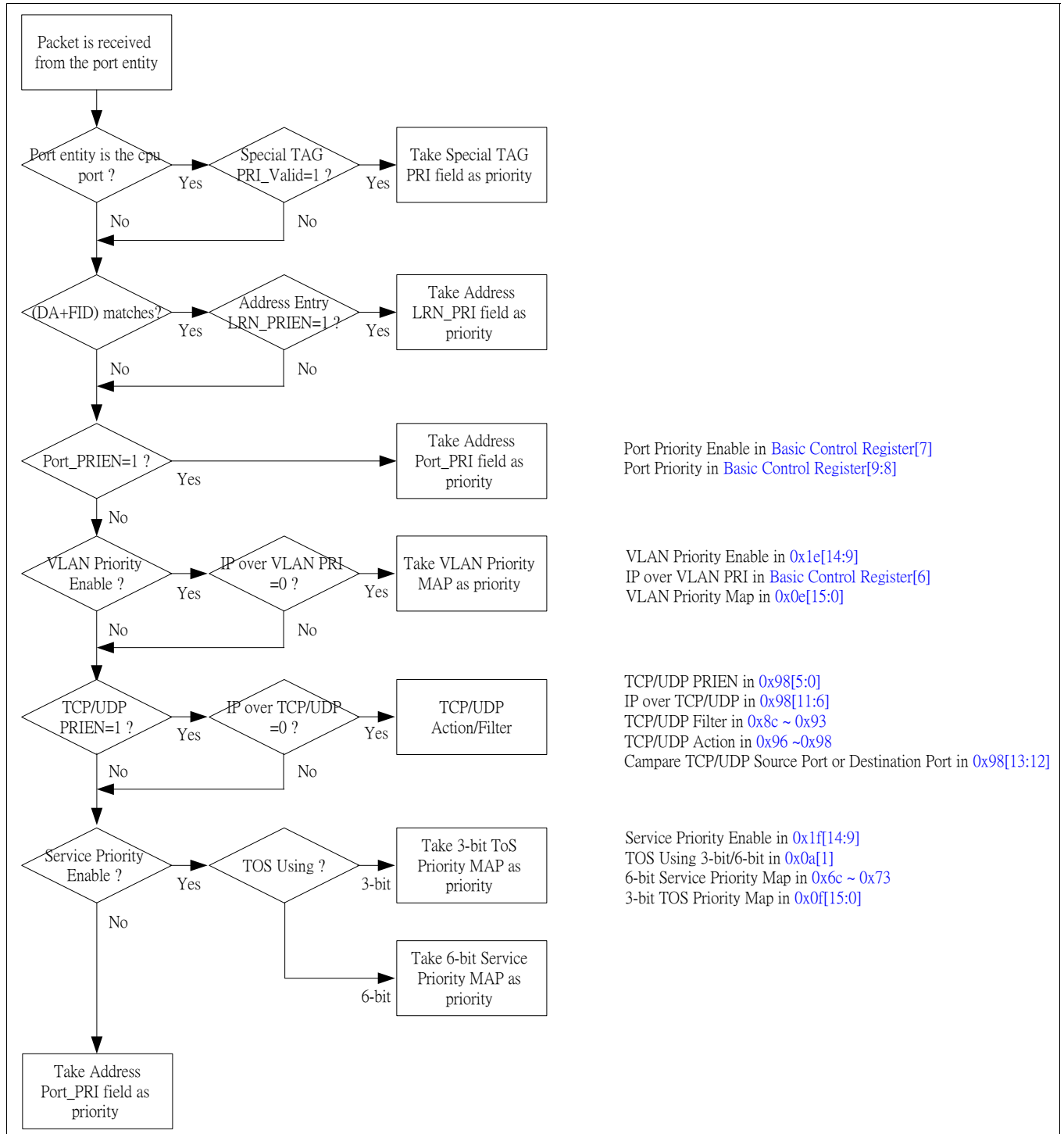


Figure 5 To Configure Samurai QoS function

3.1.16 Address Learning

Samurai-6I/6IX (ADM6996I/IX) provides two ways to create an entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow the maximum of 4 different addresses with

the same hash key to be stored at the same time. Up to 2k entries can be created and all entries are stored in the internal SSRAM. Samurai-6I/6IX (ADM6996I/IX) searches the learning table for the SA+FID of the incoming packet or the instruction from CPU. When both fields (a single SA may exist in different FID) are matched, there is a match.

3.1.16.1 Dynamic Learning

The Samurai-6I/6IX (ADM6996I/IX) searches for SA and FID of an incoming packet in the address table and takes dynamic learning action as follows:

1. If (SA+FID) was not found in the learning table, create a new entry with SA, FID, and the incoming port.
2. If (SA+FID) was found in the learning table, and the incoming port and the Portmap don't match, create a new entry with SA, FID, and the incoming port.

Dynamic learning will be disabled in the following condition:

1. Security violation exists on the port.
2. VLAN violation exists on the port.
3. The packet is a PAUSE packet.
4. The number of the addresses that port has learned has reached its maximum.
5. The port disables its learning function (see extended control registers).
6. The packet is an illegal packet (too long, too short or FCS error).
7. A packet with Special Tag is received and the LRN bit is 0 and LRN_Valid = 1_B.
8. The port is in the Disabled state in the Spanning Tree Protocol.
9. The port is in the Blocking/Listening state in the Spanning Tree Protocol.
10. All the four entries in the same hash address are occupied and all of them are static addresses.

3.1.16.2 Manual Learning

The Samurai-6I/6IX (ADM6996I/IX) implements the manual learning with the CPU's help. The CPU can create or remove any entry in the address table. Each entry could be static or not. "Static" means the entry will not be aged forever. When the entry is static, then the definition in some fields is modified to make Samurai-6I/6IX (ADM6996I/IX) work more flexibly.

3.1.16.3 Learning Table

3.1.16.3.1 Entry Format in the Learning Table

| 69 | 68 | 67 | 66 ... 58 | 57 ... 52 | 51 ... 48 | 47 ... 0 |
|-----|-----------|--------|---------------------|-----------|-----------|----------|
| Bad | Info_Type | Occupy | Info_Ctrl/Age Timer | Portmap | FID | Address |

| Field | Description |
|-----------|---|
| Bad | The entry is marked to show if it is failed during the learning table memory bist time. 0 _B Doesn't fail 1 _B Fail |
| Info_Type | Static Address. 0 _B The entry is not static 1 _B The entry is static |

Function Description

| Field | Description | | | | | | | | | | | | | | | | | | | | |
|---------------------|---|-----|-------------|---|---|---|--|---|--|---|---|-----|--|---|---|-----|--|-----|-------------|-----|---|
| Occupy | The entry is marked to show the status if the entry is occupied. 0 _B Don't occupy 1 _B Occupy | | | | | | | | | | | | | | | | | | | | |
| Info_Ctrl/Age Timer | Info_Ctrl is used when the entry is static. <table> <tr> <th>Bit</th><th>Description</th></tr> <tr> <td>8</td><td>Source Intrusion 0_B It isn't a violated source address 1_B It is a violated source address</td></tr> <tr> <td>7</td><td>Span 0_B Not span packet 1_B A span packet</td></tr> <tr> <td>6</td><td>Management 0_B Not a management packet 1_B A management packet</td></tr> <tr> <td>5</td><td>Cross_VLAN 0 = Not a cross_VLAN packet. 1 = A cross_VLAN packet.</td></tr> <tr> <td>4:3</td><td>TXTAG It is used as an option for inserting Tag on the transmission port. 00_B System Default Tag 01_B Unmodified 10_B Always Tagged 11_B Always Untagged</td></tr> <tr> <td>2</td><td>LRN_PRIEN 0_B LRN_PRI is not used 1_B LRN_PRI is used</td></tr> <tr> <td>1:0</td><td>LRN_PRI It identified the address priority. 00_B Queue 0 01_B Queue 1 10_B Queue 2 11_B Queue 3</td></tr> </table> <p>Age Timer is used when the entry is not static.</p> <table> <tr> <th>Bit</th><th>Description</th></tr> <tr> <td>8:0</td><td>Age Timer This timer is used to control the ageing time.</td></tr> </table> | Bit | Description | 8 | Source Intrusion 0 _B It isn't a violated source address 1 _B It is a violated source address | 7 | Span 0 _B Not span packet 1 _B A span packet | 6 | Management 0 _B Not a management packet 1 _B A management packet | 5 | Cross_VLAN 0 = Not a cross_VLAN packet. 1 = A cross_VLAN packet. | 4:3 | TXTAG It is used as an option for inserting Tag on the transmission port. 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged | 2 | LRN_PRIEN 0 _B LRN_PRI is not used 1 _B LRN_PRI is used | 1:0 | LRN_PRI It identified the address priority. 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 | Bit | Description | 8:0 | Age Timer This timer is used to control the ageing time. |
| Bit | Description | | | | | | | | | | | | | | | | | | | | |
| 8 | Source Intrusion 0 _B It isn't a violated source address 1 _B It is a violated source address | | | | | | | | | | | | | | | | | | | | |
| 7 | Span 0 _B Not span packet 1 _B A span packet | | | | | | | | | | | | | | | | | | | | |
| 6 | Management 0 _B Not a management packet 1 _B A management packet | | | | | | | | | | | | | | | | | | | | |
| 5 | Cross_VLAN 0 = Not a cross_VLAN packet. 1 = A cross_VLAN packet. | | | | | | | | | | | | | | | | | | | | |
| 4:3 | TXTAG It is used as an option for inserting Tag on the transmission port. 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged | | | | | | | | | | | | | | | | | | | | |
| 2 | LRN_PRIEN 0 _B LRN_PRI is not used 1 _B LRN_PRI is used | | | | | | | | | | | | | | | | | | | | |
| 1:0 | LRN_PRI It identified the address priority. 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 | | | | | | | | | | | | | | | | | | | | |
| Bit | Description | | | | | | | | | | | | | | | | | | | | |
| 8:0 | Age Timer This timer is used to control the ageing time. | | | | | | | | | | | | | | | | | | | | |
| Portmap | The field is used as the output ports associated with the FID+MAC Address. | | | | | | | | | | | | | | | | | | | | |
| FID | The field is used as the FID group associated with the MAC address. | | | | | | | | | | | | | | | | | | | | |
| Address | The MAC Address in the learning table. | | | | | | | | | | | | | | | | | | | | |

3.1.16.3.2 The Registers Accessing the Learning Table

12 registers are provided by Samurai-6I/6IX (ADM6996I/IX) to support access to the address table. These 12 registers are Address Table Control Register 0 ~ 5 and Address Table Status Register 0 ~ 5 in 011A_H ~ 0125_H.

Function Description

Table 24 Control Register Description for accessing the address table

| Command | Access Control | Info_Type | Info_Ctrl/Age Timer | Portmap | FID | Address |
|----------------|----------------|---------------|---------------------|----------------|----------------|-----------------------------------|
| Control 5[6:4] | Control 5[3:0] | Control 4[12] | Control 4[8:0] | Control 3[9:4] | Control 3[3:0] | {Control 2, Control 1, Control 0} |

The Address, FID, Portmap, Info_Ctrl/Age Timer and Info_Type in the Control Register have the same meaning as those in the entry format. The Command and Access Control is described as follows:

Table 25 Description for Command and Access Control

| Command | Access Control | Description |
|------------------|-------------------|--|
| 000 _B | 0111 _B | Create a new address |
| 000 _B | 1111 _B | Overwrite an existed address |
| 001 _B | 1111 _B | Erase an existed address |
| 010 _B | 0000 _B | Search an empty address |
| 010 _B | 1001 _B | Search by the port in the Output Port field |
| 010 _B | 1010 _B | Search by the forwarding group specified in the Forwarding Group field |
| 010 _B | 1100 _B | Search by the address specified in the MAC Address field |
| 010 _B | 1110 _B | Search by the address and forwarding group |
| 010 _B | 1101 _B | Search by the address and output port |
| 010 _B | 1011 _B | Search by the forwarding group and the output port |
| 010 _B | 1111 _B | Search by the address, the forwarding group and the output port |
| 011 _B | 0100 _B | Initial to location by the address field |
| 011 _B | 0000 _B | Initial to the first address |

Table 26 Status Register Description

| Busy | Result | Bad | Occupy | Info_Type | Info_Ctrl/Age_Time | Portmap | FID | Address |
|---------------|------------------|--------------|--------------|--------------|--------------------|----------------|----------------|--------------------------------|
| Status 5 [15] | Status 5 [14:12] | Status 5 [2] | Status 5 [1] | Status 5 [0] | Status 4 [8:0] | Status 3 [9:4] | Status 3 [3:0] | {Status 2, Status 1, Status 0} |

Table 27 Description for the Status Register

| | |
|--------------------|--|
| Address | After the search operation is successful, the switch will return the MAC address in this field. If the search fails, this field doesn't mean anything. |
| FID | After the search operation is successful, the switch will return FID in the matched entry. |
| Portmap | After the search operation is successful, the switch will return Portmap in the entry. |
| Info_Ctrl/Age Time | After the search operation is successful, the switch will return Info_Ctrl/Age Timer in the entry. |
| Info_Type | After the search operation is successful, the switch will return Info_Type in the entry |
| Occupy | After the search operation is successful, the switch will return Occupy in the entry |
| Bad | After the search operation is successful, the switch will return Bad in the entry |

Table 27 Description for the Status Register (cont'd)

| | |
|--------|---|
| Result | <p>This field tells us the status for not only the search operation but also the creating operation.</p> <p>000_B Command OK</p> <p>001_B All Entries Used. This result happens only for the create operation. Samurai-6I/6IX (ADM6996I/IX) uses the 4-way address lookup engine so it allows 4 different addresses stored at each hash location. If these 4 entries are all static, then CPU will not successfully create the 5th different address hashed to the same location and 001 will be returned. The only way to create 5th different address is to remove one of early addresses.</p> <p>101_B Command Error</p> |
| Busy | <p>This bit indicates if the table engine for access is available.</p> <p>1_B The engine is busy and it will not accept the command from the CPU.</p> <p>0_B The engine is available.</p> |

3.1.16.3.3 Rules to Access the Learning Table

1. Check the Busy Bit in the status register to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write the MAC address[15:0] into the control register 0.
3. Write the MAC address[31:16] into the control register 1.
4. Write the MAC address[47:32] into the control register 2.
5. Write the Portmap and FID into the control register 3.
6. Write the Info_Ctrl/Age Timer and Info_Type into the control register 4.
7. Write the Access Control and Command into the control register 5 to define the operation.
8. Wait for the engine to complete (Check the Busy Bit).
9. Read the desired result returned in the status register.

Note: Before a new search starts, the CPU should execute the "Initial command" to initialise the search pointer. The search engine can search the aim from the top to bottom. The search engine has the ability to automatically move the pointer to an associated location (The result will be returned). Because more than one entry may match the search condition (by port, by address, etc) at the same time, the CPU should continue to restart the search engine until the Command Result = Entry Not is found to confirm that no other matching entries exist and at this time a new search can start.

3.1.16.3.4 Example

| Example | Rule |
|--|---|
| The user needs Samurai-6I/6IX (ADM6996I/IX) to forward the specified unicast packet (DA = 0012-3456-789A _H and FID = 2) to port 3 forever. | <ol style="list-style-type: none"> 1. Check the Busy bit. If Busy = 0_B, go to the next step. If Busy = 1_B, wait. 2. Write 789A_H into control register 0. 3. Write 3456_H into control register 1. 4. Write 0012_H into control register 2. 5. Write 0082_H into control register 3. 6. Write 1000_H into control register 4. 7. Write 0007_H into control register 5. 8. Read the status register 5 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait |
| The user needs Samurai-6I/6IX (ADM6996I/IX) to forward the specified multicast packet (DA = 0123-4567-89AB _H and FID = 3) to port 0, and port 1 both. This address could be aged. | <ol style="list-style-type: none"> 1. Check the Busy bit. If Busy = 0_B, go to the next step. If Busy = 1_B, wait. 2. Write 89AB_H into control register 0. 3. Write 3456_H into control register 1. 4. Write 0123_H into control register 2. 5. Write 0033_H into control register 3. 6. Write 0000_H into control register 4. 7. Write 0007_H into control register 5. 8. Read the status register 5 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait |
| The user wants to know how many stations attached to port 4 | <ol style="list-style-type: none"> 1. Check the Busy bit. If Busy = 0_B, go to the next step. If Busy = 1_B, wait. 2. Write 0030_H into control register 5 to initial the search pointer to the first address. 3. Wait until the Busy bit changes to 0_B. 4. Write 0100_H into the control register 3. 5. Write 0029_H into the control register 5 to start the operation of the search by port. 6. Read the status register 5 to check the busy bit. If Busy = 0_B, check the Command Result to see if the search operation is successful (the Mac address attached to port 4 could be derived from the MAC address in the status register). If Busy = 1_B, wait for completion. 7. If Command Result = "Command OK", it means some other MAC addresses attached to port 4 may exist. We should restart the "Search by port" command again to let the search engine to look another addresses. 8. If the Command Result = "Entry Not Found", it means no other addresses attached to port 4 exist. |

3.1.17 Address Aging

Samurai-6I/6IX (ADM6996I/IX) maintains an age timer for each address. The aging timer is reset to 0 when the packet is received. When aging time counts up to 300 seconds, it means that this station didn't transmit packets for this period and the address can be removed from the table. This could help to prevent a station leaves the network and occupies a table space for a long time. Aging function can be disabled from the EEPROM (see extend control registers). If the address is static, Samurai-6I/6IX (ADM6996I/IX) doesn't age it out also. The default aging timer is 300 seconds. User could change Aging Timer Select (0011_H, **ATS**) to shorten the aging time.

3.1.18 Hardware Based IGMP Snooping

Samurai-6I/6IX (ADM6996I/IX) supports IGMP v1/v2 Snooping without any software effort. Samurai-6I/6IX (ADM6996I/IX) will monitor the IGMP traffic and update its embedded IGMP membership table if the hardware based IGMP snooping function is enabled. IP multicast frames can be forwarded according to the Port-Map

information of the membership table. The data of the membership can also be accessed by the CPU via SDC/SDIO interface. The following registers could be used to configure the IGMP Snooping behavior.

1. EEPROM register 00B_H bit [13:12], Additional Snooping Control register.ports.
2. EEPROM register 00B_H bit [2], Source Violation Over Snooping.
3. EEPROM register 00B_H bit [1], Source Violation Over Default.
4. EEPROM register 00C_H bit [13:6], various Snooping Control registers.
5. EEPROM register 00C_H bit [2], Hardware IGMP Packet Ignore CPU Port.
6. EEPROM register 00C_H bit [1], Hardware IGMP Snooping Enable.
7. EEPROM register 00C_H bit [0], Hardware IGMP Default Router Enable.
8. EEPROM register 00D_H bit [14], IP Multicast Packet Treated as Cross VLAN packet.
9. EEPROM register 01B_H bit [14:9], Multicast Port-Map.
10. EEPROM register 03F_H bit [15:8], Query Interval.
11. EEPROM register 03F_H bit [7:6], Robust Variable.
12. EEPROM register 03F_H bit [5:0], Default Router Port-Map.

3.1.18.1 Entry Format of IGMP Membership Table

| 57 | 56 | 55 ... 48 | 47 ... 42 | 41 ... 30 | 29 | 28... 23 | 22 ... 0 |
|-----|--------|-----------|-----------|-----------|----------|----------|----------|
| Bad | Occupy | Reserved | Reserved | Reserved | Reserved | Portmap | Group ID |

| Field | Description |
|----------|--|
| Bad | The entry is marked to show if it is failed during the memory BIST time of IGMP membership table. 0 _B Doesn't fail 1 _B Fail |
| Occupy | The entry is marked to show the status if the entry is occupied. 0 _B Empty Entry 1 _B Occupied Entry |
| Reserved | Reserved. Ignore the content in reading and fill in 0 in writing. |
| Reserved | Reserved. Ignore the content in reading and fill in 0 in writing. |
| Reserved | Reserved. Ignore the content in reading and fill in 0 in writing. |
| Reserved | Reserved. Ignore the content in reading and fill in 0 in writing. |
| Portmap | This flag is used to denote whether the port is the member of this Group or not. 0 _B The port is not the member of this Group. 1 _B The port is the member of this Group. |
| Group ID | IP Multicast Group ID. |

3.1.18.2 The Registers Accessing the IGMP Membership Table

The registers for accessing the IGMP membership table are the same with accessing MAC address filtering table, but the data format are re-defined as below.

Table 28 Control Register Description for Accessing the IGMP Membership Table

| Command | Entry Address | Entry Data |
|----------------|----------------|---|
| Control 5[6:4] | Control 4[4:0] | {Control 3[9:0], Control 2, Control 1, Control 0} |

The Command used to access IGMP membership table is defined as below.:

Table 29 Description for Command and Access Control

| Command | Description |
|------------------|-------------------------------------|
| 100 _B | Write data into internal IGMP table |
| 101 _B | Read data from internal IGMP table |

Table 30 Entry Format of IGMP Membership Table

| Busy | Result | Entry Address | Entry Data |
|--------------|-----------------|---------------|---|
| Status 5[15] | Status 5[14:12] | Status 4[4:0] | {Status 3[9:0], Status 2, Status 1, Status 0} |

3.1.18.3 IGMP Snooping Introduction

IGMP snooping is a feature that allows the switch to “listen in” on the IGMP conversation between hosts and routers. When a switch hears an IGMP report from a host for a given multicast group, the switch adds the host's port number to the GDA (Group Destination Addresses) list for that group. And, when the switch hears an IGMP leave, it removes the host's port from the Multicast table entry.

Multicast Address

1. Multicast IP addresses are Class D IP addresses. Therefore, all IP addresses from 224.0.0.0 to 239.255.255.255 are multicast IP addresses. They are also referred to as Group Destination Addresses (GDA).

2. For each GDA there is an associated MAC address. This MAC address is formed by 01-00-5e, followed by the last 23 bits of the GDA translated in hex. Therefore:

- 230.20.20.20 corresponds to MAC 01-00-5e-14-14-14
- 224.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a

Consequently, this is not a one-to-one mapping, but a one-to-many mapping:

- 224.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a
- 226.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a, as well

3. Some Multicast IP addresses are reserved for special use. For example:

- 224.0.0.1 - All multicast-capable hosts.
- 224.0.0.2 - All multicast-capable routers
- 224.0.0.5 and 224.0.0.6 is used by: Open Shortest Path First (OSPF).

In general, addresses from 224.0.0.1 to 224.0.0.255 are reserved and used by various protocols.

IGMP

IGMP is a standard defined in RFC1112 for IGMPv1 and in RFC2236 for IGMPv2. It specifies how a host can register a router to receive specific multicast traffic.

IGMPv1

- **Membership Query** are issued by router at regular intervals to check whether there is still a host interested in the GDA in that segment.

Table 31 IPV4/IGMP/General Query

| | | | | | | | | | |
|----------------------------|---------------|-------------------|-------------|---------------|---------------|-------------------|-------------------|-------------------|------------------|
| DA 01005e000001 | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 224.0.0.1 |
| Unused (Len*4-20) bytes | TP 8'h11 | Unused 3 bytes | GA 32'b0 | | | | | | |

Function Description

- **Membership Report** is issued by hosts that want to receive a specific multicast group (GDA). Host membership reports are issued either unsolicited (when the host wants to receive GDA traffic first) or in response to a membership query.

Table 32 IPV4/IGMP/V1 Report

| | | | | | | | | | |
|----------------------------|---------------|-------------------|---------------|---------------|---------------|-------------------|-------------------|-------------------|----------------|
| DA 01005exxxxxx | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 4 bytes |
| Unused (Len*4-20) bytes | TP 8'h12 | Unused 3 bytes | GA 4 bytes | | | | | | |

Host membership queries are sent by router to the all multicast address: 224.0.0.1. These queries use 0.0.0.0 in the IGMP GDA field. A host for each group must respond to that query or the router will stop forwarding the traffic for that GDA to that segment (after 3 attempts). The router simply keeps a multicast routing entry for each source and links it to a list of outgoing interfaces (interface from where the IGMP report came). After three IGMP query attempts with no answer, this interface is erased from outgoing interface list for all entries linked to that GDA.

Note: IGMPv1 has no leave mechanism. If a host no longer wants to receive the traffic, it simply quits. If it is the last, the router will not have any answers to its query and will delete the GDA for that subnet.

IGMPv2

- Membership Query

Table 33 IPV4/IGMP/General Query

| | | | | | | | | | |
|----------------------------|---------------|-------------------|-------------|---------------|---------------|-------------------|-------------------|-------------------|------------------|
| DA 01005e000001 | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 224.0.0.1 |
| Unused (Len*4-20) bytes | TP 8'h11 | Unused 3 bytes | GA 32'b0 | | | | | | |

- IGMPv1 Membership Report

Table 34 IPV4/IGMP/V1 Report

| | | | | | | | | | |
|----------------------------|---------------|-------------------|---------------|---------------|---------------|-------------------|-------------------|-------------------|----------------|
| DA 01005exxxxxx | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 4 bytes |
| Unused (Len*4-20) bytes | TP 8'h12 | Unused 3 bytes | GA 4 bytes | | | | | | |

- IGMPv2 Membership Report

Table 35 IPV4/IGMP/V2 Report

| | | | | | | | | | |
|----------------------------|---------------|-------------------|---------------|---------------|---------------|-------------------|-------------------|-------------------|----------------|
| DA 01005exxxxxx | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 4 bytes |
| Unused (Len*4-20) bytes | TP 8'h16 | Unused 3 bytes | GA 4 bytes | | | | | | |

- **Leave Group** when a host wants to leave a group, it should send a Leave Group IGMP message to destination 224.0.0.2 (instead of leaving silently like in IGMPv1)

Function Description

Table 36 IPV4/IGMP/V2 Leave

| | | | | | | | | | |
|----------------------------|---------------|-------------------|---------------|---------------|---------------|-------------------|-------------------|-------------------|------------------|
| DA 01005000002 | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 224.0.0.2 |
| Unused (Len*4-20) bytes | TP 8'h17 | Unused 3 bytes | GA 4 bytes | | | | | | |

- **Group-specific Query** a router can now send a group-specific query by sending a Membership Query to the group GDA instead of sending it to 0.0.0.0

Table 37 IPV4/IGMP/Group-Specific Query

| | | | | | | | | | |
|----------------------------|---------------|-------------------|---------------|---------------|---------------|-------------------|-------------------|-------------------|----------------|
| DA 01005exxxxxx | SA 6 bytes | Type 16'h0800 | Ver 4'h4 | Len 4 bits | TOS 1 byte | Unused 7 bytes | Protocol 8'h02 | Unused 6 bytes | DIP 4 bytes |
| Unused (Len*4-20) bytes | TP 8'h11 | Unused 3 bytes | GA 4 bytes | | | | | | |

Learning the Router Port

The switch listens to the following messages in order to detect router ports with IGMP snooping

- IGMP Membership query send to 01-00-5e-00-00-01

Once a router port is detected, it is added to the port list of all GDAs in that VLAN.

[Hardware IGMP Snooping]

1. Enable Hardware IGMP Snooping, set EEPROM register 0C_H[1]=1

2. Hardware IGMP Default Router

- If EEPROM register 0C_H[0]=0, Samurai will learn the router port automatically.

Note: The presence of the router port is configured by Query Interval (EEPROM register 3F_H[15:8]) defined as the length of time that must pass before the Router Port decides there is no longer another multicast router which should be the querier.

- If EEPROM register 0C_H[0]=1, Samurai will learn the router port according to the Default Router Port-map.
- If EEPROM register 3F_H[5:0], Default Router Port-map

Note: The router port always exists even no IGMP query is received. The group membership is maintained by Robust Variable (EEPROM register 3F_H[7:6]) defined as the amount of query that must pass before the Default Router decides there are no members of a group on a network.

Joining a Group with IGMP Snooping

Below are two joining scenarios.

Scenario A: Host A is the first host to join a group in the segment.

- Host A sends an unsolicited IGMP Membership report.
- The switch intercepts the IGMP membership report that sent by the host that wanted to join the group.
- The switch creates a multicast entry for that group and links it to the port on which it has received the report and to all router ports.
- The switch forwards the IGMP report on to all router ports. This is so that the router will also receive the IGMP report and will update its multicast routing table accordingly.

[Hardware IGMP Snooping]

Function Description

Samurai supports 32 IGMP membership table. Samurai will maintain IGMP membership table according to IGMPv1/v2 protocol. If 32 IGMP membership table is full, the later incoming IGMP packets will follow "Multicast Port-map".

User can use Address Table Control Register command and Address Table Status Register command to access 32 IGMP membership table.

Table 38 IGMP Membership Table

| | | | |
|-------------------------|----------------------------------|------------------------|----------------------------------|
| Address Table Control 0 | EEPROM register 11A _H | Address Table Status 0 | EEPROM register 120 _H |
| Address Table Control 1 | EEPROM register 11B _H | Address Table Status 1 | EEPROM register 121 _H |
| Address Table Control 2 | EEPROM register 11C _H | Address Table Status 2 | EEPROM register 122 _H |
| Address Table Control 3 | EEPROM register 11D _H | Address Table Status 3 | EEPROM register 123 _H |
| Address Table Control 4 | EEPROM register 11E _H | Address Table Status 4 | EEPROM register 124 _H |
| Address Table Control 5 | EEPROM register 11F _H | Address Table Status 5 | EEPROM register 125 _H |

- IGMP membership table Read Command
 - (1) Check the **Busy** Bit in the **Status Register 5 [15]** to see if the access engine is available. If **Busy = 1_B**, wait until the engine is free. If **Busy = 0_B**, go to the following step.
 - (2) Write **Control Register 4 [4:0]** to assign the entry numbers you want to access.
 - (3) Write **Control Register 5 [6:4] = 101_B** to start the operation of Read command.
 - (4) Read the **Busy Bit** in the **Status Register 5 [15]** to see if the operation is successful. If **Busy = 1_B**, wait until the operation is completed. If **Busy = 0_B**, read **Status Register 5 ~ 0** to get the IGMP membership table entry.
- IGMP membership table Write Command
 - (1) Check the **Busy** Bit in the **Status Register 5 [15]** to see if the access engine is available. If **Busy = 1_B**, wait until the engine is free. If **Busy = 0_B**, go to the following step.
 - (2) Write **Control Register 0 ~ 4** to assign the entry numbers you want to access.
 - (3) Write **Control Register 5 [6:4] = 100_B** to start the operation of Write command.
 - (4) Read the **Busy Bit** in the **Status Register 5 [15]** to see if the operation is successful. If **Busy = 1_B**, wait until the operation is completed. If **Busy = 0_B**, read **Status Register 5 ~ 0** to get the IGMP membership table entry.

3.1.19 Source Violation

Source violation is defined in Samurai-6I/6IX (ADM6996I/IX) to support flexible security modes. See Security Option in the EEPROM Basic Register and the Src_Violation bit in the Learning Table.

Function Description

| Security Mode | Description |
|------------------|--|
| First Lock | <p>Samurai-6I/6IX (ADM6996I/IX) locks the first SA+FID of packets received on the port. After the first (SA+FID) is locked, Samurai-6I/6IX (ADM6996I/IX) starts to check packets with different (SA+FID).</p> <ol style="list-style-type: none"> 1. If the packets are not assigned as management, drop them (modify the forwarding algorithm) and record as a source violation. 2. If the packets are management packets, and Source Violation (see 000B_H, System Control Register 1) is configured to 1_B for different kinds of packets, then Samurai-6I/6IX (ADM6996I/IX) modifies the forwarding algorithm to drop these packets. They are also recorded as a source violation. 3. If the packets are management packets and Source Violation is configured to 0_B, then Samurai-6I/6IX (ADM6996I/IX) doesn't modify the forwarding algorithm. In this situation, we don't record this case as a source violation. |
| First Link Lock | <p>The first received packets will be locked as First Lock. The difference is that the receiving port will not receive and learn packets any more after the port links down even if it links up again. A source violation is recorded as the First Lock. If Samurai-6I/6IX (ADM6996I/IX) modifies the forwarding algorithm is still as the First Lock.</p> |
| Assign Lock | <p>Samurai-6I/6IX (ADM6996I/IX) allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. A source violation is recorded as the First Lock. If Samurai-6I/6IX (ADM6996I/IX) modifies the forwarding algorithm is still as the First Lock.</p> |
| Assign Link Lock | <p>Samurai-6I/6IX (ADM6996I/IX) allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. The others are the same as First Link Lock.</p> |
| Discard Unknown | <p>The "unknown source address" means that (SA+FID) is not found in the learning table or even is found but Portmap doesn't match the incoming port. If "unknown" packets are received, Samurai-6I/6IX (ADM6996I/IX) records the source violation as the First Lock. The rule to modify the forwarding algorithm is still as the First Lock.</p> |
| Unknown to CPU | <p>This option is the same as "Discard Unknown" except that if Samurai-6I/6IX (ADM6996I/IX) decides to modify the forwarding algorithm, it will forward the packets to the CPU port instead of dropping them.</p> |
| Source Intrusion | <p>If the incoming port receives the packets with SA is marked as Source Intrusion, we handle these packets in the following rule:</p> <ol style="list-style-type: none"> 1. Enable Source Intrusion Must (see 000B_H, SIM) to instruct Samurai-6I/6IX (ADM6996I/IX) to modify the forwarding algorithm and record the source violation always. 2. If Source Intrusion Must is not enabled, Samurai-6I/6IX (ADM6996I/IX) also modifies the forwarding algorithm and records the source violation when any non-management packets are received. 3. If Source Intrusion Must is not enabled, Samurai-6I/6IX (ADM6996I/IX) also modifies the forwarding algorithm and records the source violation when a management packets are received but Source Violation is configured to 1_B. 4. If Source Intrusion Must is not enabled, Samurai-6I/6IX (ADM6996I/IX) doesn't modify the forwarding algorithm and records the source violation when management packets are received and Source Violation is configured to 0_B. <p>Samurai-6I/6IX (ADM6996I/IX) allows the users to redirect the packets to the CPU port instead of dropping it when they violate the source intrusion (see Source Intrusion Action in 000B_H, SIA).</p> |

Samurai-6I/6IX (ADM6996I/IX) supports stricter security protection. The port is disabled when there is a source violation. Enable Security Option[3] to enable this feature.

3.1.20 Packet Forwarding

Samurai-6I/6IX (ADM6996I/IX) identifies a packet header and transfers it from the incoming port to the destination ports.

3.1.20.1 Control Table

Samurai-6I/6IX (ADM6996I/IX) provides a control table for users to control the forwarding algorithm of the DA = 01 80 C2 00 00 00_H ~ DA = 01 80 C2 00 00 2F_H easily. This control table is defined in 0074_H ~ 008B_H.

3.1.20.2 Default Output Ports

The default output ports that a packet is transferred to are determined in the following order.

1. The Portmap in the Special Tag with Portmap_Valid = 1 is used as the output ports.
2. The Portmap in the learning table is used as the output ports, when (DA+FID) matches an entry in the learning table.
3. The Portmap in the hardware IGMP table is used as the output ports, when DA matches an entry in the hardware IGMP table and "Hardware IGMP Snooping" (see 000C_H, [HISE](#)) is enabled.
4. "Broadcast Portmap" (see 001A_H, [BP](#)) is used as the output ports, when the incoming packet is a broadcast packet.
5. "Multicast Portmap" (see 001B_H, [MP](#)) is used as the output ports, when the incoming packet is a multicast packet.
6. "Unicast Portmap" (see 0019_H, [UP](#)) is used as the output ports, when the incoming packet is a unicast packet.

3.1.20.3 Forwarding Algorithm

Table 39 Forwarding Algorithm

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | Algorithm |
|--|--|
| BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3 | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF ((DA+FID) matches an entry in the learning table), THEN use the Portmap in the learning table as the output ports. ELSE IF (DA matches an entry in the control table), THEN the output ports are the Portmap in the table. ELSE the output ports are the intersection of the Pass Portmap (see 003D _H New Reserve Address Control Register 0 and 003E _H New Reserve Address Control Register 1) and the "Reserve Portmap" in the EEPROM (see 001C _H , RP) |
| ARP/RARP | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF (ARP/RARP is trapped), THEN use ARP/RARP Portmap as the output ports. ELSE use "Default Output Ports" as the output ports. |

Table 39 Forwarding Algorithm (cont'd)

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | Algorithm |
|---|---|
| IGMP_IP/MLD_IP/MLD_IPV6 | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF (Hardware IGMP Snooping is enabled), IF (Hardware IGMP Packet Ignore CPU Port is enabled), THEN forwards packets to Multicast Portmap but doesn't forward to the CPU port. Else forwards packets to Multicast Portmap. ELSE IF (IGMP_IP/MLD_IP/MLD_IPV6 is trapped), THEN use IGMP/IGMP_IP/MLD_IP/MLD_IPV6 Portmap as the output ports. ELSE use "Default Output Ports" as the output ports. |
| TYPE | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use Type Portmap as the output ports. |
| PROTOCOL | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use Protocol Portmap as the output ports. |
| TCPUDP | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use TCPUDP Portmap as the output ports. |
| MAC_CTRL | IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use MAC CTRL Portmap as the output ports. |
| Others | Use "Default Output Ports" as the output ports |

3.1.21 Special TAG

Special Tag is inserted after the Ethernet SA field to allow the CPU to tell the switch how to handle the packets it sends or to know the source port when the CPU receives a packet.

| | |
|---------|---------------|
| 8 Bytes | Preamble |
| 6 Bytes | DA |
| 6 Bytes | SA |
| Byte 0 | Special Tag 0 |
| Byte 1 | Special Tag 1 |
| Byte 2 | Special Tag 2 |
| Byte 3 | Special Tag 3 |
| Byte 4 | Special Tag 4 |
| Byte 5 | Special Tag 5 |
| 4 Bytes | VLAN Tag |
| 6 Bytes | SNAP |
| 2 Bytes | Type/Length |
| | Data |
| 4 Bytes | CRC |

3.1.21.1 Special Tag for the Receive

Users are allowed to enable Special TAG Receive (0011_H, **STRE**) function to instruct Samurai-6I/6IX (ADM6996I/IX) to check the Special Tag to see if this field contains any commands when packets are received on the CPU port.

Table 40 Special Tag for the Receive

| Special TAG | Description |
|-------------|--|
| Byte 0 | ADM Prefix 0. |
| Byte 1 | ADM Prefix 1. When Special TAG Receive is enabled, Samurai-6I/6IX (ADM6996I/IX) will compare {ADM Prefix -, ADM Prefix 1} with ADM TAG Ether Type (see 002E _H , ATET). If they are different, Special Tag is ignored. If they are the same, Samurai-6I/6IX (ADM6996I/IX) uses the Special Tag to make switching decisions. |
| Byte 2 | Bit [7]: Don't care Bit [6]: Portmap_Valid 1 _B Valid 0 _B Not Valid Bit [5:0]: Portmap in the Special Tag |
| Byte 3 | Bit [7]: Span_Valid 1 _B Valid 0 _B Not Valid Bit [6]: Span 1 _B Span packet 0 _B Not span packet Bit [5]: Management_Valid 1 _B Valid 0 _B Not Valid Bit [4]: Management 1 _B Management packet 0 _B Not management packet Bit [3]: Cross_VLAN_Valid 1 _B Valid 0 _B Not Valid Bit [2]: Cross_VLAN 1 _B Cross_Vlan packet 0 _B Not Cross_VLAN packet Bit [1]: LRN_Valid 1 _B Valid 0 _B Not Valid Bit [0]: LRN 1 _B Learn 0 _B Not Learn |

Table 40 Special Tag for the Receive (cont'd)

| Special TAG | Description |
|-------------|---|
| Byte 4 | Bit[7]: Ignore Bit[6]: PRI_Valid 1 _B Valid 0 _B Not Valid Bit[5:4]: PRI 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 Bit [3]: Ignore Bit [2]: TXTAG_Valid 1 _B Valid 0 _B Not Valid Bit [1:0]: TXTAG |
| Byte 5 | Bit [6]: Tagged Member Valid 1 _B Valid 0 _B Not Valid Bit [5:0]: Tagged Member, Bit[X] = 1: Port is in the tagged member |

3.1.21.2 Special Tag for the Transmit

Users are allowed to enable Special TAG Transmit (0011_H, **STTE**) functions to instruct Samurai-6I/6IX (ADM6996I/IX) to insert the Special Tag followed SA in the packets transmitted from the CPU port. Samurai-6I/6IX (ADM6996I/IX) also allows users to choose what kinds of packets they don't want to insert this Special Tag even when Special TAG Transmit (0011_H, **STTE**) function is enabled.

Table 41 Option for Special Tag Transmit

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | Condition | Result |
|--|--|---|
| BPDU/SLOW/PAE/RESER_R0/RESER_R1/GXRP/RESER_R2/RESER_R3 | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert Reserve} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Reserve} = 11 _B . | Insert Special Tag on the CPU port. |
| ARP/RARP | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert ARP/RARP} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert ARP/RARP} = 11 _B . | Insert Special Tag on the CPU port. |
| IGMP_IP/MLD_IP/MLD_IPV6 | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert Snoop} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Snoop} = 11 _B . | Insert Special Tag on the CPU port. |
| TYPE | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert Type} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Type} = 11 _B . | Insert Special Tag on the CPU port. |
| PROTOCOL | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert Protocol} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Protocol} = 11 _B . | Insert Special Tag on the CPU port. |
| TCPUDP | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert TCP/UDP} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert TCP/UDP} = 11 _B . | Insert Special Tag on the CPU port. |
| MAC_CTRL | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert MAC CTRL} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert MAC CTRL} = 11 _B . | Insert Special Tag on the CPU port. |

Function Description

Table 41 Option for Special Tag Transmit (cont'd)

| Packets Identified by Samurai-6I/6IX (ADM6996I/IX) | Condition | Result |
|--|---|---|
| Others | Special TAG Transmit = 0 _B . or{Special TAG Transmit, Insert Default, Source Violation} = 100 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Default, Source Violation} = 110 _B . or{Special TAG Transmit, Insert Default, Source Violation} = 101 _B . . {Special TAG Transmit, Insert Default, Source Violation} = 111 _B . | Insert Special Tag |

Table 42 Special Tag for the Transmit

| Special TAG | Description |
|-------------|--|
| Byte 0 | ADM Prefix 0. |
| Byte 1 | ADM Prefix 1. |
| Byte 2 | Bit [7]: Source Violation. 1 = This packet is a source violated packet and it modified its forwarding algorithm to the CPU port. 0 = This packet is not a source violated packet.Bit [6]: Mirror. 1 = This is a mirrored packet. 0 = This is not a mirrored packet.Bit [5]: Span. 1 = This is a span packet. 0 = This is not a span packet.Bit [4]: Management. 1 = This is a management packet. 0 = This is not a management packet. Bit [3]: Ignore. Bit [2:0]: Source Port. 000 _B = Port 0. 001 _B = Port 1. 010 _B = Port 2. 011 _B = Port 3. 100 _B = Port 4. 101 _B = Port 5. |
| Byte 3 | Egress TAG[15:8]. |
| Byte 4 | Egress TAG[7:0]. |
| Byte 5 | Ignore. |

3.2 MAC Clone and Port5 MII Connection

In ADM6996I/IX, there are three different configurations (MAC type MII mode, GPSI mode and RMII, **P5_BUSMD0**) for Port5 to connect the CPU's MII/GPSI or RMII interface.

Here we show a general router application of ADM6996I/IX, connected to the CPU with a single MII. In **Figure 6**, we can see either LAN to WAN or WAN to LAN, the packets will go through the same MII port. Because the CPU needs to send out the packets with the registered MAC ID to the WAN port, this MAC ID may also come in from the LAN ports. We know the switch learning scheme can't permit the packets with the same MAC ID input from different ports. In the ADM6996I/IX design, we use the MAC clone and VLAN group to solve this problem. From **Figure 9**, users can have more details for this implementation.

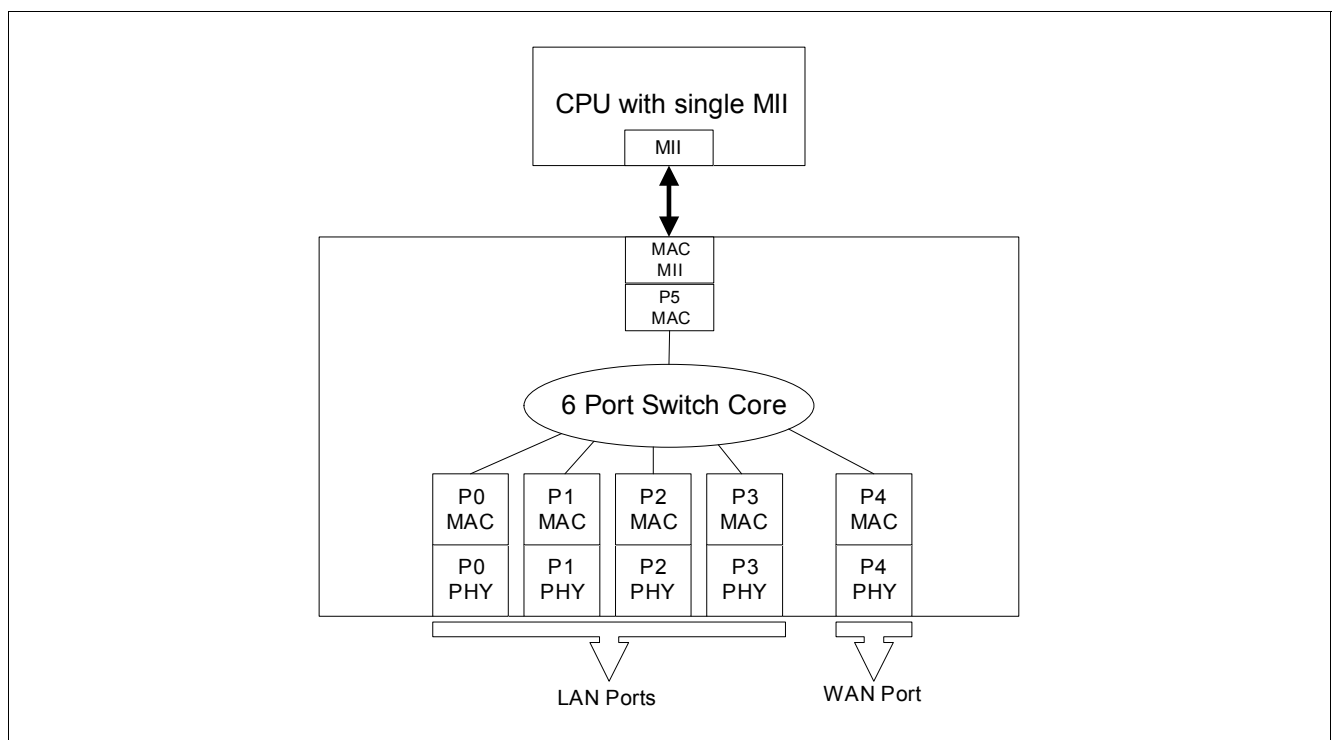


Figure 6 ADM6996I/IX to CPU with single MII Connection

Implementation of WAN/LAN applications on Samurai

ADM6996I/IX implements WAN/LAN application by ADM6996I/IX Special TAG functions.

Special Tag is inserted after the Ethernet SA field to allow the CPU to tell the switch how to handle the packets it sends or to know the source port when the CPU receives a packet.

Table 43 Special Tag

| Pream- ble | DA | SA | Special TAG 0 | Special TAG 1 | Special TAG 2 | Special TAG 3 | Special TAG 4 | Special TAG 5 | VLAN Tag | SNAP | Type/ Length | Data | CRC |
|---------------|----|----|------------------|------------------|------------------|------------------|------------------|------------------|-------------|------|-----------------|------|-----|
| 8B | 6B | 6B | Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | 4B | 6B | 2B | | 4B |

Step 1: Set EEPROM 11_H[12]=1 to enable Special TAG Receive (CPU to ADM6996I/IX).

Step 2: Set EEPROM 11_H[11]=1 to enable Special TAG Transmit (ADM6996I/IX to CPU).

Set EEPROM 11_H[15:13] to assign CPU Port Number. Default CPU Port is "101 - Port5".

Function Description

Set EEPROM 0B_H[5] to set the option whether ADM6996I/IX CPU Port checks CRC for the packet with Special TAG Receive.

Set EEPROM 11_H[10] to set the option whether ADM6996I/IX adds Special TAG Transmit to Pause frame.

The configurations are as follows.

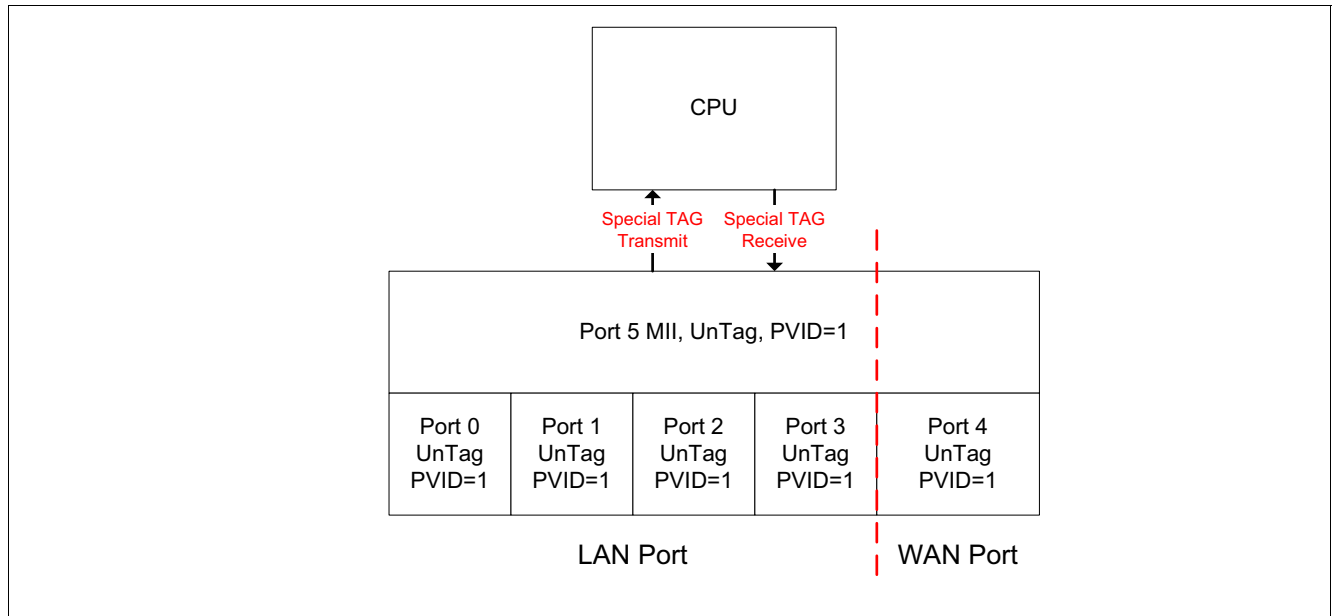


Figure 7 The configurations of the implementation by ADM6996I/IX Special TAG functions

- Step 1: Set ADM6996I/IX to port-based VLAN mode (default)
- Step 2: Set WAN/LAN group

Table 44 Set WAN/LAN Group

| EEPROM | Received Port | Forwarding Group | | | | | |
|-----------------|------------------|------------------|--------|--------|--------|--------|--------|
| | Port-based Group | Port 0 | Port 1 | Port 2 | Port 3 | Port 4 | Port 5 |
| 40 _H | Port 0 | ✓ | O | O | O | | ✓ |
| 42 _H | Port 1 | O | ✓ | O | O | | ✓ |
| 44 _H | Port 2 | O | O | ✓ | O | | ✓ |
| 46 _H | Port 3 | O | O | O | ✓ | | ✓ |
| 48 _H | Port 4(WAN Port) | | | | | ✓ | ✓ |
| 4A _H | Port 5(CPU Port) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: "✓" is necessary and "O" is optional to implement Port-based VLAN function of LAN group.

Port 0, Port 0/1/2/3/5, set REG 40_H to 002F_H

Port 1, Port 0/1/2/3/5, set REG 42_H to 002F_H

Port 2, Port 0/1/2/3/5, set REG 44_H to 002F_H

Port 3, Port 0/1/2/3/5, set REG 46_H to 002F_H

Port 4, Port 4/5, set REG 48_H to 0030_H

Port 5, Port 0/1/2/3/4/5, set REG 4A_H to 003F_H

- Step 3: Set EEPROM 11_H[12:11]="11" to enable Special TAG Receive/Transmit Enable

Software Operation:

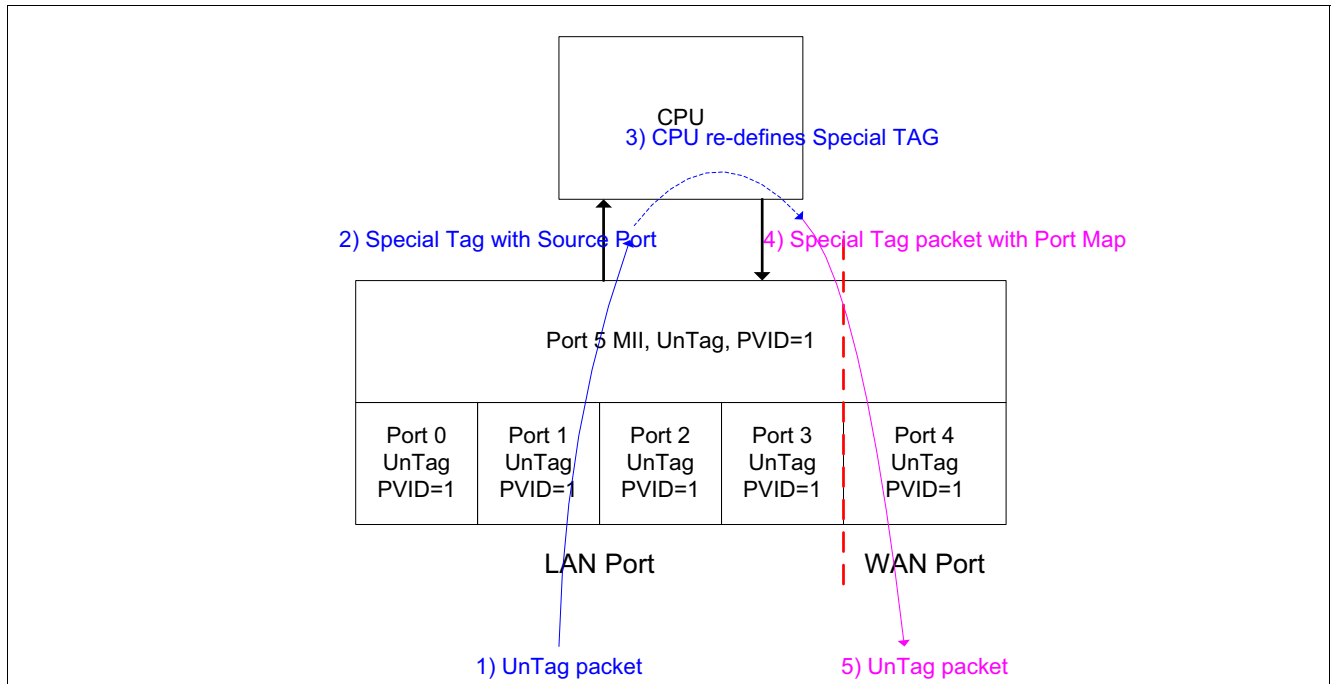


Figure 8 Software Operation

- Step 1:
 - If Untagged packet received from LAN Port forwards to CPU Port, ADM6996I/IX will insert Special TAG followed SA in the packets transmitted from the CPU port. ADM6996I/IX also allows users to choose what kinds of packets they don't want to insert this Special TAG in.

Table 45 Packets Identified by ADM6996I/IX

| Packets Identified by ADM6996I/IX | Condition (EEPROM 0x11h[11] and 0x99h[8:0]) | Result |
|--|--|---|
| BPDU/SLOW/PAE/RESER_R0/RESER_R1/GXRP/RESER_R2/RESER_R3 | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert Reserve} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Reserve} = 11 _B | Insert Special Tag on the CPU port. |
| ARP/RARP | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert ARP/RARP} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert ARP/RARP} = 11 _B . | Insert Special Tag on the CPU port. |
| IGMP_IP/MLD_IP/MLD_IPV6 | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert Snoop} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Snoop} = 11 _B . | Insert Special Tag on the CPU port. |
| TYPE | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert Type} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Type} = 11 _B . | Insert Special Tag on the CPU port. |

Function Description

Table 45 Packets Identified by ADM6996I/IX

| Packets Identified by ADM6996I/IX | Condition (EEPROM 0x11h[11] and 0x99h[8:0]) | Result |
|-----------------------------------|---|---|
| PROTOCOL | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert Protocol} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Protocol} = 11 _B . | Insert Special Tag on the CPU port. |
| TCPUDP | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert TCP/UDP} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert TCP/UDP} = 11 _B . | Insert Special Tag on the CPU port. |
| MAC_CTRL | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert MAC CTRL} = 10 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert MAC CTRL} = 11 _B . | Insert Special Tag on the CPU port. |
| Others | Special TAG Transmit = 0 _B . or {Special TAG Transmit, Insert Default, Source Violation} = 100 _B . | Don't insert Special Tag on the CPU port. |
| | {Special TAG Transmit, Insert Default, Source Violation} = 110 _B . or {Special TAG Transmit, Insert Default, Source Violation} = 101 _B . or {Special TAG Transmit, Insert Default, Source Violation} = 111 _B . | Insert Special Tag |

- Step 2: CPU must re-define the Special TAG for the Receive to determine the destination group.
- Step 3: If **MAC_CLONE** function is enabled, CPU must set **LRN** parameter to disable learning mechanism for specific packet.

Normally, the MAC mode MII should be connected to the PHY mode MII. But in some applications, we need to connect both MAC mode MII's to each other as shown. In [Figure 9](#), due to most of the CPU's MII being in MAC mode, Port5 is MAC to MAC connection.

Through the hardware setting, it is easy to set ADM6996I/IX Port5 MII to operate in 100M Full duplex mode. As this mode (100M Full) is normally the operation mode to be with CPU, the interface connection is described in the following diagram.

(1) CKO25M is the 25M clock driven out by ADM6996I/IX to fit 100M MII operation. This clock output provides 8mA driving capability and it can be directly connected to TXCLK/RXCLK.

(2) Due to it's operation in Full duplex mode, COL is tied to GND.

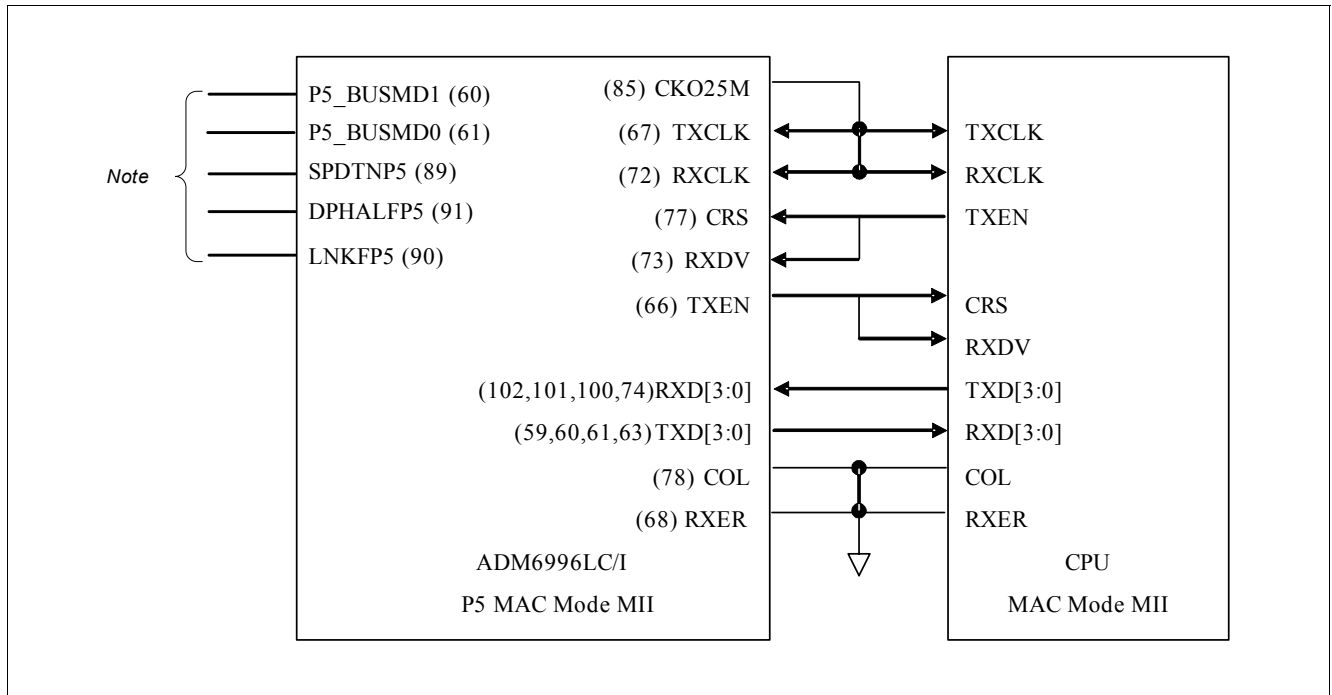


Figure 9 100M Full duplex MAC to MAC MII connection

Note:

1. Pin 60 and pin 61 should be pull low to let P5_BUSMD be latched as "00" and forces Port5 to operate in MII mode (**P5_BUSMD0**).
2. Pin 89 (SPDTNP5) should be pull low or floating to set Port5 be operating in 100Mbit/s.
3. Pin 91 (DPHALFP5) should be pull low or floating to set Port5 be operating in full duplex mode.
4. Pin 90 (LNKFP5) should be pull low or floating to set Port5 Link up.

3.3 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

100Base-X physical coding sub-layer (PCS)

100Base-X physical medium attachment (PMA)

100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

10Base-T physical layer signaling (PLS)

10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

Clock synthesizer module

MII Registers

IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface.

Auto MDIX function is supported. This function can be Enable/Disabled by the hardware pin.

Digital approach for the integrated PHY of Samurai-6I/6IX (ADM6996I/IX) has been adopted.

3.3.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The Samurai-6I/6IX (ADM6996I/IX) supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the Samurai-6I/6IX (ADM6996I/IX) can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software enables bit 12 in MII register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the Samurai-6I/6IX (ADM6996I/IX) transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbit/s, 100 Mbit/s, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the “auto negotiation link partner ability register” are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

100Base-TX full duplex (highest priority)

100Base-TX half duplex

10Base-T full duplex

10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbit/s or 100 Mbit/s operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the Samurai-6I/6IX (ADM6996I/IX). The BMSR also provides status on:

Whether auto negotiation is complete (bit 5)

Whether the Link Partner is advertising that a remote fault has occurred (bit 4)

Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4_H indicates the auto negotiation abilities to be advertised by the Samurai-6I/6IX (ADM6996I/IX). All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1_H) is set.

3.3.2 Speed/Duplex Configuration

The twelve sets of four pins listed in [Table 46](#) configure the speed/duplex capability of each channel of Samurai-6I/6IX (ADM6996I/IX). The logic states of these pins are latched into the advertisement register (register address 4_H) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to [Table 46](#).

In order to make these pins have the same Read/Write priority as software, they should be programmed to 11111111_B in case user likes to update the advertisement register through software.

Table 46 Speed/Duplex Configuration

| Auto Negotiation (Pin & EEPROM) | Speed (Pin & EEPROM) | Duplex (Pin & EEPROM) | Auto Negotiation | Advertise Capability | | | | Parallel Detect Capability | | | |
|---------------------------------|----------------------|-----------------------|------------------|----------------------|------|-----|-----|----------------------------|------|-----|-----|
| | | | | 100F | 100H | 10F | 10H | 100F | 100H | 10F | 10H |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | — | — | — | — | — | — | — |
| 0 | 1 | 0 | 0 | — | 1 | — | — | — | — | — | — |
| 0 | 0 | 1 | 0 | — | — | 1 | — | — | — | — | — |
| 0 | 0 | 0 | 0 | — | — | — | 1 | — | — | — | — |

3.4 Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the Samurai-6I/6IX (ADM6996I/IX):

- Hardware Setting
- EEPROM Interface
- SMI Interface

Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See [Figure 10](#) as a description.

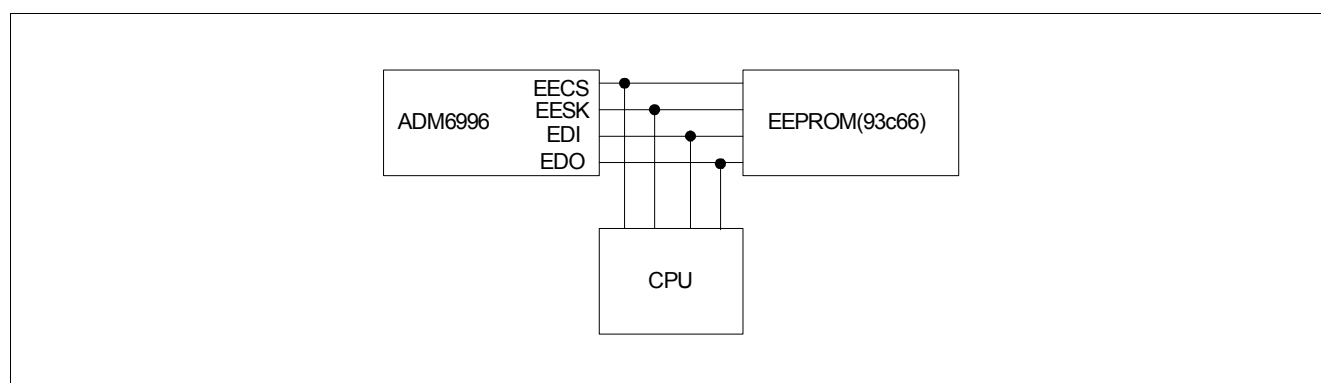


Figure 10 Interconnection between Samurai-6I/6IX (ADM6996I/IX), EEPROM and CPU

3.4.1 Hardware Setting

The Samurai-6I/6IX (ADM6996I/IX) provides some hardware pins where values reside during power on or reset, when they are strapped for the default setting.

Table 47 Hardware Setting

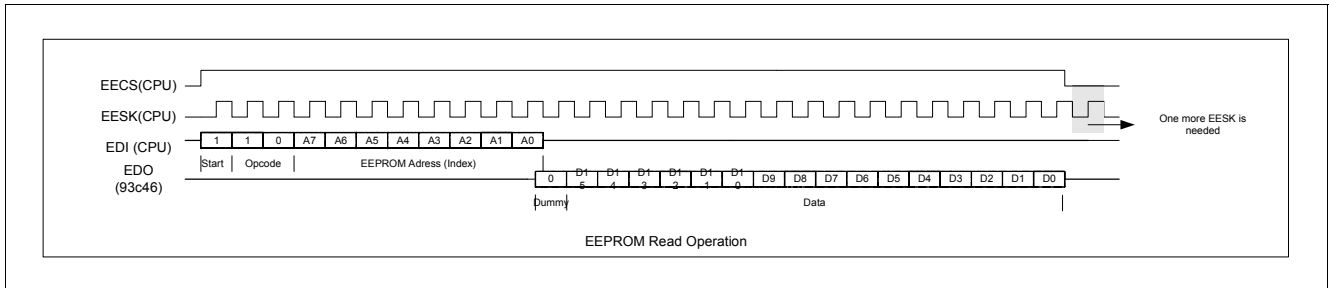
| Setting Name | Description |
|-----------------|--|
| GFCEN | Global Flow Control Enable. 0 _B Flow Control Capability is depended upon the register setting in corresponding EEPROM register 1 _B All ports flow control capability is enabled. |
| SDIO_MD | SDC/SDIO mode selection. 0 _B 16 bits mode 1 _B 32 bits mode |
| P5_BUSMD[1:0] | Port 5 bus mode selection bit 0. P5_BUSMD[1:0] Interface 00 _B MII01 01 _B GPSI 10 _B RMII 11 _B Reserved and Not Allowed. |
| BPEN | Recommend Back-Pressure in half-duplex. 0 _B Disable Back-Pressure. 1 _B Enable Back-Pressure |
| RECANEN | Recommend Auto Negotiation Enable. Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. 0 _B Disable all TP port auto negotiation capability 1 _B Enable all TP port auto negotiation capability |
| XOVEN | Cross Over Enable. Only available in TP interface. 0 _B Disable 1 _B Enable |
| LED_MODE | Enable Mac to choose LED Display Mode. 0 _B Single color LED 1 _B Dual color LED |

3.4.2 EEPROM Interface

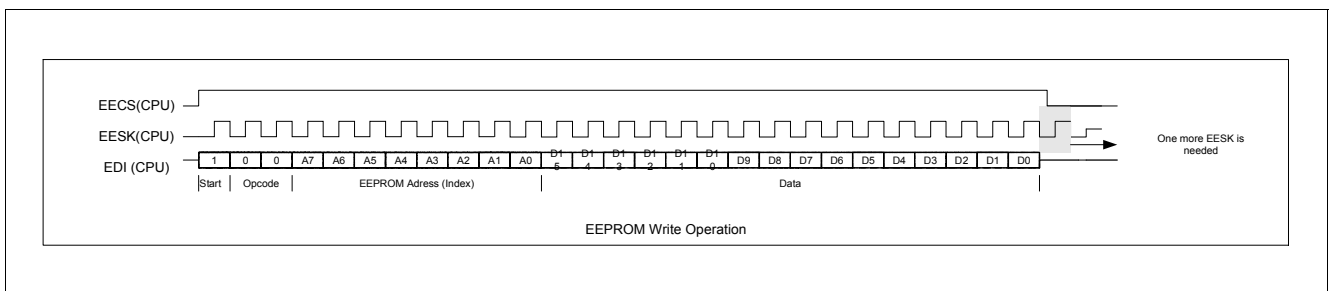
The EEPROM Interface is provided so users can easily configure the settings without the CPU's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After power up or reset (default value from the hardware pins fetched in this stage), the Samurai-6I/6IX (ADM6996I/IX) will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = 4154_H, it will read all the data in the 93c66. If not, the Samurai-6I/6IX (ADM6996I/IX) will stop loading the 93c66. The user also can pull down the **EDO** to force the Samurai-6I/6IX (ADM6996I/IX) not to load the 93c66. The 93c66 loading time is around 500ms. Then CPU should give the high-z value in the **EECS**, **EESK** and **EDI** pins in this period if we really want to use the CPU to read or write the registers in the Samurai-6I/6IX (ADM6996I/IX).

The EEPROM Interface needs only one Write command to complete a writing operation. If updating the 93c66 at the same time is necessary, three commands Write Enable, Write, and Write Disable are needed to complete this job (See 93c66 Spec. for a reference). Users should note that the EEPROM interface only allows the CPU to write the EEPROM register in the Samurai-6I/6IX (ADM6996I/IX) and doesn't support the READ command. If the CPU gives the Read Command, Samurai-6I/6IX (ADM6996I/IX) will not respond and 93c66 will respond with the value. Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write).

(1) Read 93c66 via the EEPROM Interface (Index = 2, Data = 1111_H).



(2) Write EEPROM registers in the Samurai-6I/6IX (ADM6996I/IX) (Index = 2, Data = 2222_H).



Power-On-Sequence of Samurai

The following diagram shows the power-on-sequence of Samurai.

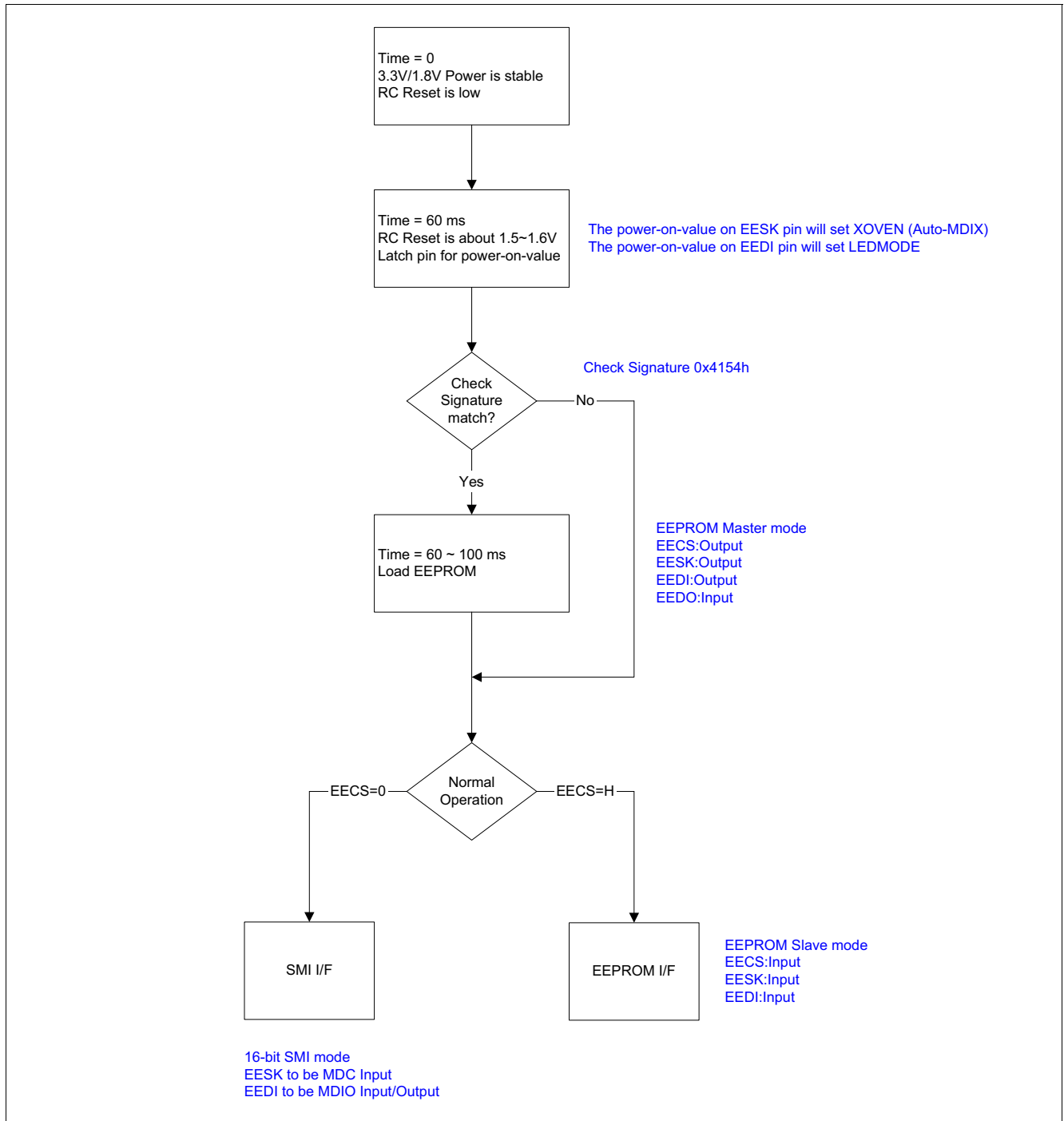


Figure 11 The Power-On-Sequence of Samurai

Set ADM6996LC/FC Pin59 SDIO_MD=1 to 16-bit SMI mode.

Set ADM6996I/IX/M Pin59 SDIO_MD=0(default) to 16-bit SMI mode.

Timing Diagram of RC, EECS and EESK (with correct signature EEPROM)

Waveform 1: RC Reset

Waveform 2: EECS

Waveform 4: EESK

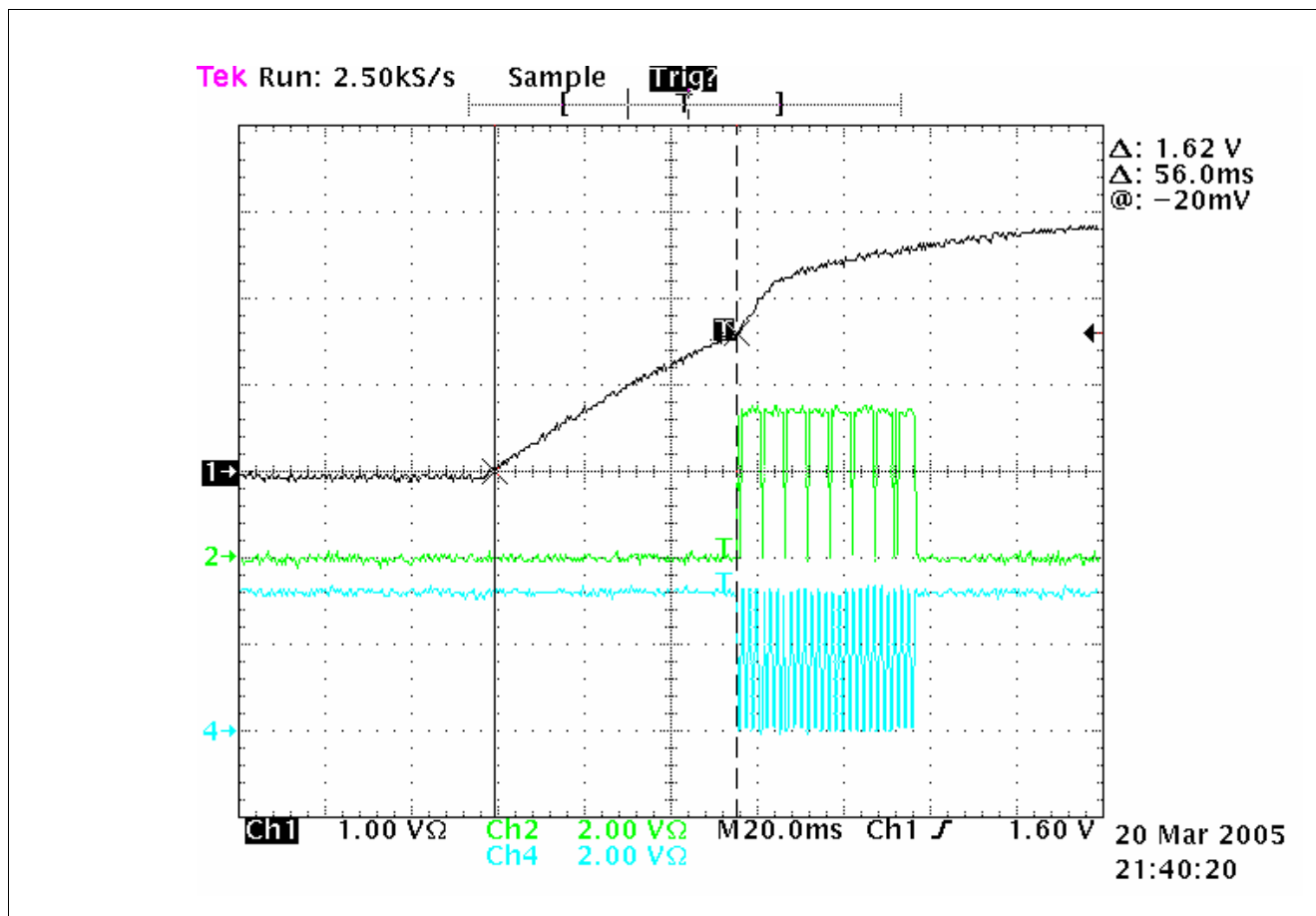


Figure 12 Timing Diagram of RC, EECS and EESK (with correct signature EEPROM)

Timing Diagram of RC, EECS and EESK (without EEPROM)

Waveform 1: RC Reset

Waveform 2: EECS

Waveform 4: EESK

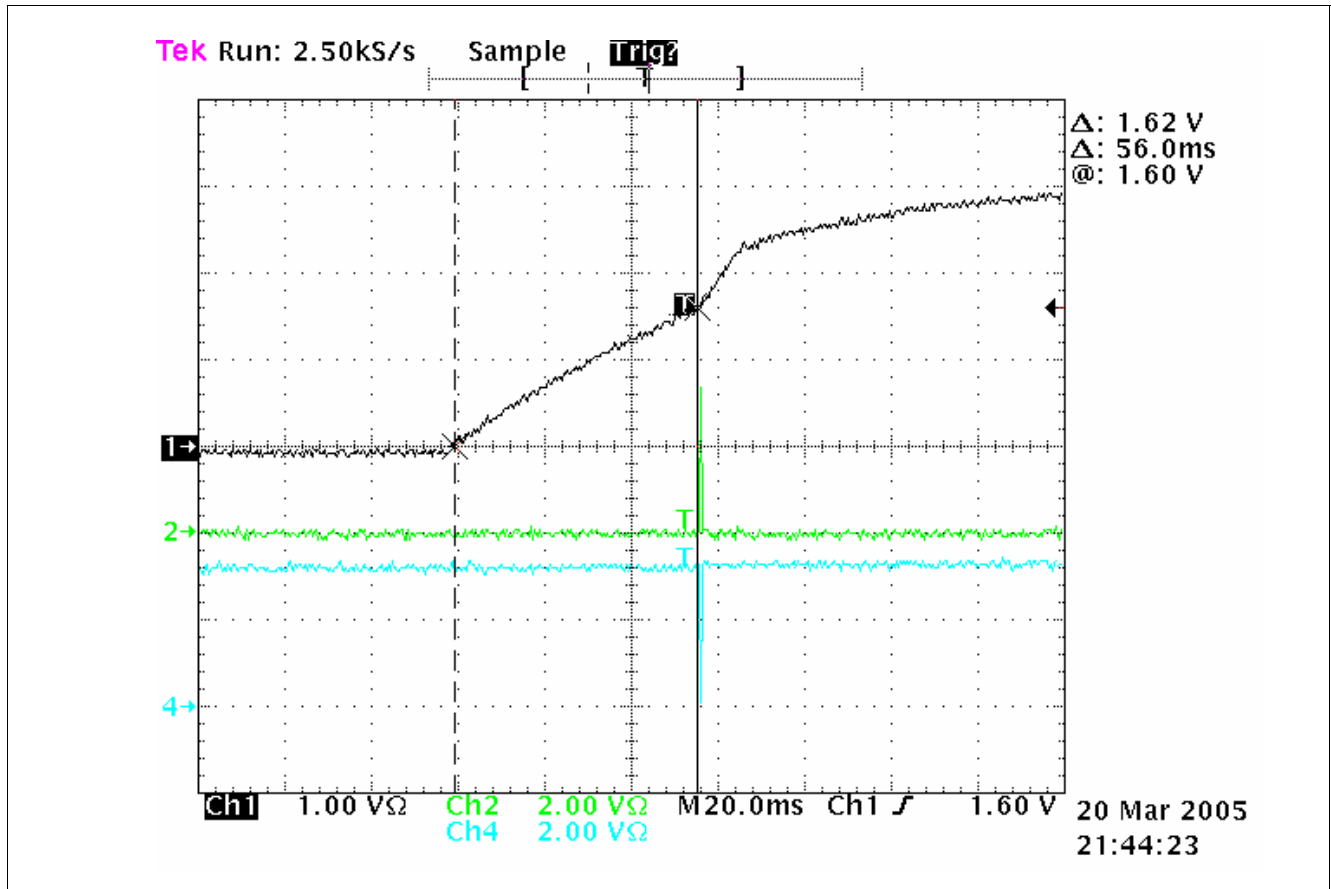


Figure 13 Timing Diagram of RC, EECS and EESK (without EEPROM)

3.4.3 SMI Interface

The SMI consists of two pins, management data clock (**EESK**) and management data input/output (**EDI**). The Samurai-6I/6IX (ADM6996I/IX) is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin may be needed (pulled to low) if the EEPROM interface is also used.

The EDI pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. Samurai-6I/6IX (ADM6996I/IX) requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a <01_B> pattern. The next field signals the operation code (OP): <10_B> indicates read from management register operation, and <01_B> indicates write to management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the management registers of the Samurai-6I/6IX (ADM6996I/IX).

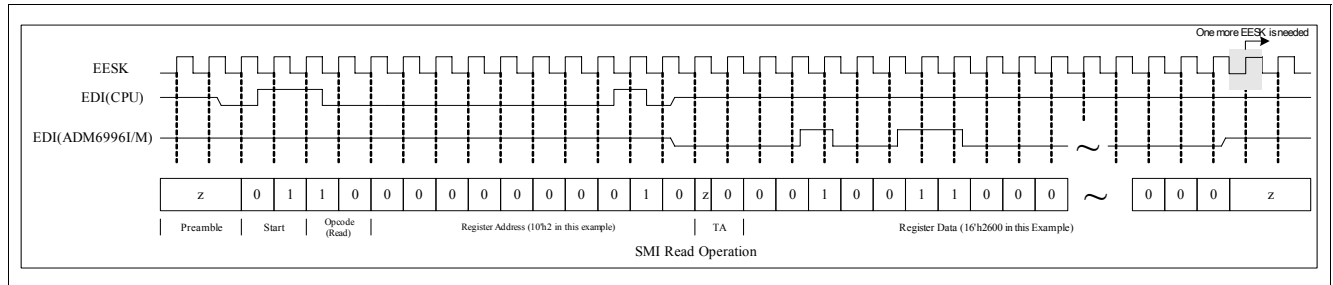
(A) Preamble Suppression

The SMI of Samurai-6I/6IX (ADM6996I/IX) supports a preamble suppression mode. The Samurai-6I/6IX (ADM6996I/IX) requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI. While the Samurai-6I/6IX (ADM6996I/IX) will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

Function Description

When Samurai-6I/6IX (ADM6996I/IX) detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then Samurai-6I/6IX (ADM6996I/IX) will tri-state the EDI pin.

(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 16'h2600)



(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 16'h1300)

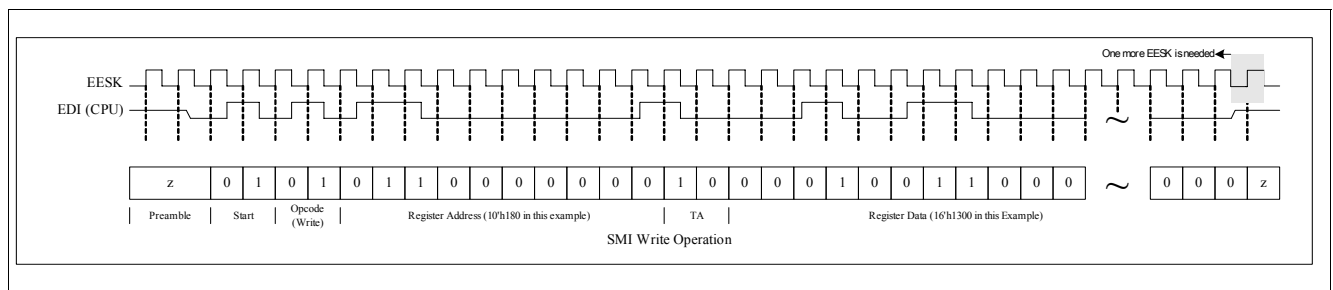


Table 48 (D) The Pin Type of EECS, EESK, EDI and EDO during the Operation

| Pin Name | Reset Operation | Load EEPROM | Write Operation | Read Operation |
|----------|-----------------|-------------|-----------------|----------------|
| EECS | Input | Output | Input | Input |
| EESK | Input | Output | Input | Input |
| EDI | Input | Output | Input | Input/Output |
| EDO | Input | Input | Input | Input |

How to Use Samurai 16-bit Mode SMI to Access EEPROM/Counter/PHY Register by CPU MDC/MDIO Interface

Samurai supports a 16-bit mode SMI interface to access EEPROM/Counter/PHY Register by CPU MDC/MDIO interface. The SMI interface consists of two pins, management data clock (EESK) and management data input/output (EDI).

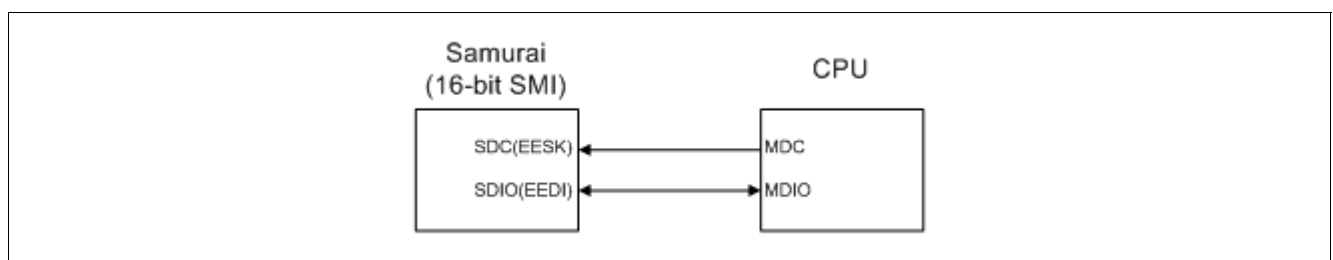


Figure 14 SMI Interface

- The difference between SMI Command and MDC/MDIO Command
 - Samurai SMI Command uses 10-bit register address to access allocate EEPROM/Counter/PHY Register.

Memory Map

Table 49 Memory Map

| Register | Definition |
|---------------------------------------|-------------------------------|
| 0000 _H ~ 003F _H | EEPROM BAISC Register Map |
| 0040 _H ~ 009B _H | EEPROM Extended Register Map |
| 00A0 _H ~ 0143 _H | Counter and Switch Status Map |
| 0200 _H ~ 02FF _H | PHY Register Map |

So you need to divide 10-bit register address to 5-bit PHY address and 5-bit REG address of MDC/MDIO command to access EEPROM/Counter Register Map. For Samurai PHY Register Map, you can set the 5-bit PHY address = '10000' and use the standard REG address to access P0~P4 PHY MII Register.

3.5 The Hardware Difference between ADM6996I/IX and ADM6996L

ADM6996LC is power-down version to replace ADM6996L and ADM6996I/IX is advanced function version to new application.

Pin Description(QFP128)

Table 50 Pin Description(QFP128)

| Pin No. | ADM6996I/IX | ADM6996L | Notes |
|---------|---------------------|---------------------|--|
| 47 | GNDIK(GND Digital) | NC | GNDIK in ADM6996L datasheet Ask the customer to double-check |
| 48 | VCCIK(1.8V Digital) | NC | VCCIK in ADM6996L datasheet Ask the customer to double-check |
| 59 | P5TXD3(SDIO_MD) | P5TXD3(VOL23) | For ADM6996LC, SDIO_MD=0 default 32bit mode For ADM6996I/IX, SDIO_MD=0 default 16bit mode Add pull-up/down resistor for ADM6996L/LC/I compatible design to avoid wrong power-on-latch. |
| 60 | P5TXD2(RMIISEL) | P5TXD2(ROMCODE25) | Add pull down resistor for ADM6996L/LC/I P5 MII mode to avoid wrong power-on-latch. |
| 61 | P5TXD1(7WIRE) | P5TXD1(P5GPSI) | Add pull down resistor for ADM6996L/LC/I P5 MII mode to avoid wrong power-on-latch. |
| 65 | INT_N | VCCIK(1.8V Digital) | Interrupt for Learning Table Access/Port Security/Counter Overflow/Port Status Add a option design to CPU INT_N pin |

4 Registers Description

The EEPROM provides Samurai-6I/6IX (ADM6996I/IX) with many option settings

Main Settings

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk.
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number

Table 51 Registers Address Space

| Module | Base Address | End Address | Note |
|-------------------------------|-------------------|-------------------|------|
| EEPROM Basic Register Map | 0000 _H | 003F _H | |
| EEPROM Extended Register Map | 0040 _H | 009C _H | |
| Counter and Switch Status Map | 00A0 _H | 0143 _H | |
| PHY Register Map | 0200 _H | 02FF _H | |

Table 52 Registers Overview

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|------------------------------|-----------------|-------------|
| SIG | Signature Register | 00 _H | 84 |
| P0BC | P0 Basic Control Register | 01 _H | 84 |
| P0EC | P0 Extended Control Register | 02 _H | 86 |
| P1EC | P1 Extended Control Register | 02 _H | 87 |
| P1 | Basic Control Register 1 | 03 _H | 86 |
| P2EC | P2 Extended Control Register | 04 _H | 87 |
| P3EC | P3 Extended Control Register | 04 _H | 87 |
| P2 | Basic Control Register 2 | 05 _H | 86 |
| P4EC | P4 Extended Control Register | 06 _H | 87 |
| P5EC | P5 Extended Control Register | 06 _H | 87 |
| P3 | Basic Control Register 3 | 07 _H | 86 |
| P4 | Basic Control Register 4 | 08 _H | 86 |
| P5 | Basic Control Register 5 | 09 _H | 86 |
| SC0 | System Control Register 0 | 0A _H | 87 |
| SC1 | System Control Register 1 | 0B _H | 88 |
| MS | Multicast Snooping Register | 0C _H | 90 |
| AR | ARP/RARP Register | 0D _H | 92 |
| VPM | VLAN Priority Map Register | 0E _H | 93 |
| TPM | TOS Priority Map Register | 0F _H | 94 |
| SC2 | System Control Register 2 | 10 _H | 95 |
| SC3 | System Control Register 3 | 11 _H | 96 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-----------------|-------------|
| SC4 | System Control Register 4 | 12 _H | 98 |
| P0SO | Port 0 Security Option | 13 _H | 99 |
| P1SO | Port 1 Security Option | 14 _H | 101 |
| P2SO | Port 2 Security Option | 15 _H | 101 |
| P3SO | Port 3 Security Option | 16 _H | 101 |
| P4SO | Port 4 Security Option | 17 _H | 101 |
| P5SO | Port 5 Security Option | 18 _H | 101 |
| UFGPM | Unicast Port Map and Forward Group Port Map | 19 _H | 101 |
| BFGPM | Broadcast Port Map and Forward Group Port Map | 1A _H | 102 |
| MFGPM | Multicast Port Map and Forward Group Port Map | 1B _H | 102 |
| RFGPM | Reserve Port Map and Forward Group Port Map | 1C _H | 103 |
| PIOFGPM | Packet Identification Option, Forward Group Port Map | 1D _H | 104 |
| VPEFGPM | VLAN Priority Enable and Forward Group Port Map | 1E _H | 105 |
| SPEFGPM | Service Priority Enable and Forward Group Port Map | 1F _H | 106 |
| IFNTFGPM | Input Force No Tag and Forward Group Port Map | 20 _H | 107 |
| IFFGPM | Ingress Filter and Forward Group Port Map | 21 _H | 108 |
| VSDFGPM | VLAN Security Disable and Forward Group Port Map | 22 _H | 109 |
| BT0 | Buffer Threshold Register 0 | 23 _H | 110 |
| BT1 | Buffer Threshold Register 1 | 24 _H | 110 |
| IMEIJT | IGMP/MLDTRAP Enable and Input Jam Threshold Register | 25 _H | 111 |
| Q2WVECPO | Queue 2 Weight, VID Exist Check, and PPPOE Port Only | 26 _H | 111 |
| Q3WBPVAO | Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged | 27 _H | 113 |
| IDTEP | Input Double Tag Enable, and P0VID[11:4] | 28 _H | 113 |
| ODTEP | Output Double Tag Enable, and P1VID[11:4] | 29 _H | 114 |
| OTBP | Output Tag Bypass, and P2VID[11:4] | 2A _H | 114 |
| P11_4 | P3VID[11:4], and P4VID[11:4] | 2B _H | 115 |
| RACP | Reserved Address Control, and P5VID[11:4] | 2C _H | 115 |
| PHYC | PHY Control Register | 2D _H | 116 |
| ATET | ADM TAG Ether Type | 2E _H | 116 |
| PR | PHY Restart Register | 2F _H | 117 |
| MISC | Miscellaneous Register | 30 _H | 117 |
| BBC0 | Basic Bandwidth Control Register 0 | 31 _H | 119 |
| BBC1 | Basic Bandwidth Control Register 1 | 32 _H | 119 |
| BCE | Bandwidth Control Enable Register | 33 _H | 120 |
| EBC0 | Extended Bandwidth Control Register 0 | 34 _H | 122 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|-------------------------|---|-----------------|---------------------|
| EBC1 | Extended Bandwidth Control Register 1 | 35 _H | 123 |
| EBC2 | Extended Bandwidth Control Register 2 | 36 _H | 123 |
| EBC3 | Extended Bandwidth Control Register 3 | 37 _H | 124 |
| EBC4 | Extended Bandwidth Control Register 4 | 38 _H | 124 |
| EBC5 | Extended Bandwidth Control Register 5 | 39 _H | 125 |
| DVMEBC6 | Default VLAN Member and Extended Bandwidth Control Register 6 | 3A _H | 125 |
| NS0 | New Storm Register 0 | 3B _H | 126 |
| NS1 | New Storm Register 1 | 3C _H | 126 |
| NRAC0 | New Reserve Address Control Register 0 | 3D _H | 127 |
| NRAC1 | New Reserve Address Control Register 1 | 3E _H | 129 |
| HIC | Hardware IGMP Control Register | 3F _H | 130 |
| VF0L | VLAN Filter 0 Low | 40 _H | 132 |
| VF0H | VLAN Filter 0 High | 41 _H | 133 |
| VF1L | VLAN Filter 1 Low | 42 _H | 132 |
| VF1H | VLAN Filter 1 High | 43 _H | 133 |
| VF2L | VLAN Filter 2 Low | 44 _H | 132 |
| VF2H | VLAN Filter 2 High | 45 _H | 133 |
| VF3L | VLAN Filter 3 Low | 46 _H | 132 |
| VF3H | VLAN Filter 3 High | 47 _H | 133 |
| VF4L | VLAN Filter 4 Low | 48 _H | 132 |
| VF4H | VLAN Filter 4 High | 49 _H | 133 |
| VF5L | VLAN Filter 5 Low | 4A _H | 132 |
| VF5H | VLAN Filter 5 High | 4B _H | 133 |
| VF6L | VLAN Filter 6 Low | 4C _H | 132 |
| VF6H | VLAN Filter 6 High | 4D _H | 133 |
| VF7L | VLAN Filter 7 Low | 4E _H | 132 |
| VF7H | VLAN Filter 7 High | 4F _H | 133 |
| VF8L | VLAN Filter 8 Low | 50 _H | 132 |
| VF8H | VLAN Filter 8 High | 51 _H | 133 |
| VF9L | VLAN Filter 9 Low | 52 _H | 132 |
| VF9H | VLAN Filter 9 High | 53 _H | 133 |
| VF10L | VLAN Filter 10 Low | 54 _H | 132 |
| VF10H | VLAN Filter 10 High | 55 _H | 133 |
| VF11L | VLAN Filter 11 Low | 56 _H | 132 |
| VF11H | VLAN Filter 11 High | 57 _H | 134 |
| VF12L | VLAN Filter 12 Low | 58 _H | 132 |
| VF12H | VLAN Filter 12 High | 59 _H | 134 |
| VF13L | VLAN Filter 13 Low | 5A _H | 133 |
| VF13H | VLAN Filter 13 High | 5B _H | 134 |
| VF14L | VLAN Filter 14 Low | 5C _H | 133 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|--------------------------|---|-----------------|---------------------|
| VF14H | VLAN Filter 14 High | 5D _H | 134 |
| VF15L | VLAN Filter 15 Low | 5E _H | 133 |
| VF15H | VLAN Filter 15 High | 5F _H | 134 |
| TF0 | Type Filter 0 | 60 _H | 134 |
| TF1 | Type Filter 1 | 61 _H | 134 |
| TF2 | Type Filter 2 | 62 _H | 134 |
| TF3 | Type Filter 3 | 63 _H | 134 |
| TF4 | Type Filter 4 | 64 _H | 134 |
| TF5 | Type Filter 5 | 65 _H | 134 |
| TF6 | Type Filter 6 | 66 _H | 134 |
| TF7 | Type Filter 7 | 67 _H | 134 |
| PF_1_0 | Protocol Filter 1 and 0 | 68 _H | 134 |
| PF_3_2 | Protocol Filter 3 and 2 | 68 _H | 135 |
| PF_5_4 | Protocol Filter 5 and 4 | 69 _H | 135 |
| PF_7_6 | Protocol Filter 7 and 6 | 6A _H | 135 |
| SPM0 | Service Priority Mapping 0 | 6C _H | 135 |
| SPM1 | Service Priority Mapping 1 | 6D _H | 136 |
| SPM2 | Service Priority Mapping 2 | 6E _H | 137 |
| SPM3 | Service Priority Mapping 3 | 6F _H | 138 |
| SPM4 | Service Priority Mapping 4 | 70 _H | 139 |
| SPM5 | Service Priority Mapping 5 | 71 _H | 139 |
| SPM6 | Service Priority Mapping 6 | 72 _H | 140 |
| SPM7 | Service Priority Mapping 7 | 73 _H | 141 |
| RA_01_00 | Reserve Action for 0180C2000001~0180C2000000 | 74 _H | 142 |
| RA_03_02 | Reserve Action for 0180C2000003~0180C2000002 | 75 _H | 143 |
| RA_05_04 | Reserve Action for 0180C2000005~0180C2000004 | 76 _H | 143 |
| RA_07_06 | Reserve Action for 0180C2000007~0180C2000006 | 77 _H | 144 |
| RA_09_08 | Reserve Action for 0180C2000009~0180C2000008 | 78 _H | 144 |
| RA_0B_0A | Reserve Action for 0180C200000B~0180C200000A | 79 _H | 144 |
| RA_0D_0C | Reserve Action for 0180C200000D~0180C200000C | 7A _H | 144 |
| RA_0F_0E | Reserve Action for 0180C200000F~0180C200000E | 7B _H | 144 |
| RA_11_10 | Reserve Action for 0180C2000011~0180C2000010 | 7C _H | 144 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-----------------|-------------|
| RA_13_12 | Reserve Action for 0180C2000013~0180C2000012 | 7D _H | 144 |
| RA_15_14 | Reserve Action for 0180C2000015~0180C2000014 | 7E _H | 144 |
| RA_17_16 | Reserve Action for 0180C2000017~0180C2000016 | 7F _H | 144 |
| RA_19_18 | Reserve Action for 0180C2000019~0180C2000018 | 80 _H | 144 |
| RA_1B_1A | Reserve Action for 0180C200001B~0180C200001A | 81 _H | 144 |
| RA_1D_1C | Reserve Action for 0180C200001D~0180C200001C | 82 _H | 144 |
| RA_1F_1E | Reserve Action for 0180C200001F~0180C200001E | 83 _H | 144 |
| RA_21_20 | Reserve Action for 0180C2000021~0180C2000020 | 84 _H | 144 |
| RA_23_22 | Reserve Action for 0180C2000023~0180C2000022 | 85 _H | 144 |
| RA_25_24 | Reserve Action for 0180C2000025~0180C2000024 | 86 _H | 144 |
| RA_27_26 | Reserve Action for 0180C2000027~0180C2000026 | 87 _H | 144 |
| RA_29_28 | Reserve Action for 0180C2000029~0180C2000028 | 88 _H | 144 |
| RA_2B_2A | Reserve Action for 0180C200002B~0180C200002A | 89 _H | 144 |
| RA_2D_2C | Reserve Action for 0180C200002D~0180C200002C | 8A _H | 144 |
| RA_2F_2E | Reserve Action for 0180C200002F~0180C200002E | 8B _H | 144 |
| TUF0 | TCP/UDP Filter 0 | 8C _H | 145 |
| TUF1 | TCP/UDP Filter 1 | 8D _H | 145 |
| TUF2 | TCP/UDP Filter 2 | 8E _H | 145 |
| TUF3 | TCP/UDP Filter 3 | 8F _H | 145 |
| TUF4 | TCP/UDP Filter 4 | 90 _H | 145 |
| TUF5 | TCP/UDP Filter 5 | 91 _H | 145 |
| TUF6 | TCP/UDP Filter 6 | 92 _H | 145 |
| TUF7 | TCP/UDP Filter 7 | 93 _H | 145 |
| TFA | Type Filter Action | 94 _H | 145 |
| PFA | Protocol Filter Action | 95 _H | 146 |
| TUA0 | TCP/UDP Action 0 | 96 _H | 147 |
| TUA1 | TCP/UDP Action 1 | 97 _H | 148 |
| TUA2 | TCP/UDP Action 2 | 98 _H | 149 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|-----------------|-------------|
| EICSTIC | Extended IGMP Control/Special Tag Insert Control | 99 _H | 150 |
| IE | Interrupt Enable Register | 9A _H | 151 |
| IS | Interrupt Status Register | 9B _H | 151 |
| SC | Security Control Register | 9C _H | 152 |
| CI0 | Chip Identifier 0 | A0 _H | 153 |
| CI1 | Chip Identifier 1 | A1 _H | 153 |
| PS0 | Port Status 0 | A2 _H | 153 |
| PS1 | Port Status 1 | A3 _H | 154 |
| PS2 | Port Status 2 | A4 _H | 155 |
| PS3 | Port Status 3 | A5 _H | 156 |
| CB0 | Cable Broken 0 | A6 _H | 156 |
| CB1 | Cable Broken 1 | A7 _H | 158 |
| CL0 | Port 0 Receive Packet Counter Low | A8 _H | 158 |
| CH0 | Port 0 Receive Packet Counter High | A9 _H | 159 |
| CL1 | Port 1 Receive Packet Counter Low | AC _H | 158 |
| CH1 | Port 1 Receive Packet Counter High | AD _H | 160 |
| CL2 | Port 2 Receive Packet Counter Low | B0 _H | 158 |
| CH2 | Port 2 Receive Packet Counter High | B1 _H | 160 |
| CL3 | Port 3 Receive Packet Counter Low | B4 _H | 158 |
| CH3 | Port 3 Receive Packet Counter High | B5 _H | 160 |
| CL4 | Port 4 Receive Packet Counter Low | B6 _H | 158 |
| CH4 | Port 4 Receive Packet Counter High | B7 _H | 160 |
| CL5 | Port 5 Receive Packet Counter Low | B8 _H | 158 |
| CH5 | Port 5 Receive Packet Counter High | B9 _H | 160 |
| CL6 | Port 0 Receive Packet Byte Count Low | BA _H | 158 |
| CH6 | Port 0 Receive Packet Byte Count High | BB _H | 160 |
| CL7 | Port 1 Receive Packet Byte Count Low | BE _H | 158 |
| CH7 | Port 1 Receive Packet Byte Count High | BF _H | 160 |
| CL8 | Port 2 Receive Packet Byte Count Low | C2 _H | 159 |
| CH8 | Port 2 Receive Packet Byte Count High | C3 _H | 160 |
| CL9 | Port 3 Receive Packet Byte Count Low | C6 _H | 159 |
| CH9 | Port 3 Receive Packet Byte Count High | C7 _H | 160 |
| CL10 | Port 4 Receive Packet Byte Count Low | C8 _H | 159 |
| CH10 | Port 4 Receive Packet Byte Count High | C9 _H | 160 |
| CL11 | Port 5 Receive Packet Byte Count Low | CA _H | 159 |
| CH11 | Port 5 Receive Packet Byte Count High | CB _H | 160 |
| CL12 | Port 0 Transmit Packet Count Low | CC _H | 159 |
| CH12 | Port 0 Transmit Packet Count High | CD _H | 160 |
| CL13 | Port 1 Transmit Packet Count Low | D0 _H | 159 |
| CH13 | Port 1 Transmit Packet Count High | D1 _H | 160 |
| CL14 | Port 2 Transmit Packet Count Low | D4 _H | 159 |

Registers Description

Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|------------------|-------------|
| CH14 | Port 2 Transmit Packet Count High | D5 _H | 160 |
| CL15 | Port 3 Transmit Packet Count Low | D8 _H | 159 |
| CH15 | Port 3 Transmit Packet Count High | D9 _H | 160 |
| CL16 | Port 4 Transmit Packet Count Low | DA _H | 159 |
| CH16 | Port 4 Transmit Packet Count High | DB _H | 160 |
| CL17 | Port 5 Transmit Packet Count Low | DC _H | 159 |
| CH17 | Port 5 Transmit Packet Count High | DD _H | 160 |
| CL18 | Port 0 Transmit Packet Byte Count Low | DE _H | 159 |
| CH18 | Port 0 Transmit Packet Byte Count High | DF _H | 160 |
| CL19 | Port 1 Transmit Packet Byte Count Low | E2 _H | 159 |
| CH19 | Port 1 Transmit Packet Byte Count High | E3 _H | 160 |
| CL20 | Port 2 Transmit Packet Byte Count Low | E6 _H | 159 |
| CH20 | Port 2 Transmit Packet Byte Count High | E7 _H | 160 |
| CL21 | Port 3 Transmit Packet Byte Count Low | EA _H | 159 |
| CH21 | Port 3 Transmit Packet Byte Count High | EB _H | 160 |
| CL22 | Port 4 Transmit Packet Byte Count Low | EC _H | 159 |
| CH22 | Port 4 Transmit Packet Byte Count High | ED _H | 160 |
| CL23 | Port 5 Transmit Packet Byte Count Low | EE _H | 159 |
| CH23 | Port 5 Transmit Packet Byte Count High | EF _H | 160 |
| CL24 | Port 0 Collision Count Low | F0 _H | 159 |
| CH24 | Port 0 Collision Count High | F1 _H | 160 |
| CL25 | Port 1 Collision Count Low | F4 _H | 159 |
| CH25 | Port 1 Collision Count High | F5 _H | 160 |
| CL26 | Port 2 Collision Count Low | F8 _H | 159 |
| CH26 | Port 2 Collision Count High | F9 _H | 160 |
| CL27 | Port 3 Collision Count Low | FC _H | 159 |
| CH27 | Port 3 Collision Count High | FD _H | 160 |
| CL28 | Port 4 Collision Count Low | FE _H | 159 |
| CH28 | Port 4 Collision Count High | FF _H | 160 |
| CL29 | Port 5 Collision Count Low | 100 _H | 159 |
| CH29 | Port 5 Collision Count High | 101 _H | 160 |
| CL30 | Port 0 Error Count Low | 102 _H | 159 |
| CH30 | Port 0 Error Count High | 103 _H | 160 |
| CL31 | Port 1 Error Count Low | 106 _H | 159 |
| CH31 | Port 1 Error Count High | 107 _H | 160 |
| CL32 | Port 2 Error Count Low | 10A _H | 159 |
| CH32 | Port 2 Error Count High | 10B _H | 160 |
| CL33 | Port 3 Error Count Low | 10E _H | 159 |
| CH33 | Port 3 Error Count High | 10F _H | 160 |
| CL34 | Port 4 Error Count Low | 110 _H | 159 |
| CH34 | Port 4 Error Count High | 111 _H | 161 |

Registers Description
Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|------------------|-------------|
| CL35 | Port 5 Error Count Low | 112 _H | 159 |
| CH35 | Port 5 Error Count High | 113 _H | 161 |
| OFF0 | Over-Flow Flag 0 | 114 _H | 161 |
| OFF1 | Over-Flow Flag 1 | 115 _H | 162 |
| OFF2 | Over-Flow Flag 2 | 116 _H | 162 |
| OFF3 | Over-Flow Flag 3 | 117 _H | 163 |
| OFF4 | Over-Flow Flag 4 | 118 _H | 164 |
| OFF5 | Over-Flow Flag 5 | 119 _H | 165 |
| HSL | Hardware Setting Low Register | 130 _H | 165 |
| HSH | Hardware Setting High Register | 131 _H | 166 |
| AA1 | Assign Address [15:0] Register | 132 _H | 167 |
| AA2 | Assign Address [31:16] Register | 133 _H | 167 |
| AA3 | Assign Address [47:32] Register | 134 _H | 168 |
| AO | Assign Option Register | 135 _H | 168 |
| MIRR0 | Mirror Register 0 | 136 _H | 169 |
| MIRR1 | Mirror Register 1 | 137 _H | 170 |
| SVP | Security Violation Port | 138 _H | 171 |
| SS0 | Security Status 0 | 139 _H | 171 |
| SS1 | Security Status 1 | 13A _H | 172 |
| FLAS | First Lock Address Search | 13B _H | 172 |
| FLA1 | First Lock Address [15:0] | 13C _H | 174 |
| FLA2 | First Lock Address [31:16] | 13D _H | 174 |
| FLA3 | First Lock Address [47:32] | 13E _H | 174 |
| FLF | First Lock FID | 13F _H | 175 |
| CCL | Counter Control Low Register | 140 _H | 175 |
| CCH | Counter Control High Register | 141 _H | 177 |
| CSL | Counter Status Low Register | 142 _H | 177 |
| CSH | Counter Status High Register | 143 _H | 177 |
| PHY_C0 | PHY Control Register of Port 0 | 200 _H | 178 |
| PHY_S0 | PHY Status Register of Port 0 | 201 _H | 180 |
| PHY_I0_A | PHY Identifier Register of Port 0 (A) | 202 _H | 182 |
| PHY_I0_B | PHY Identifier Register of Port 0 (B) | 203 _H | 182 |
| ANAP0 | Auto Negotiation Advertisement Register of Port 0 | 204 _H | 183 |
| ANLPA0 | Auto Negotiation Link Partner Ability Register of Port 0 | 205 _H | 184 |
| ANE0 | Auto Negotiation Expansion Register of Port 0 | 206 _H | 186 |
| NPT0 | Next Page Transmit Register of Port 0 | 207 _H | 186 |
| LPNP0 | Link Partner Next Page Register of Port 0 | 208 _H | 187 |
| PHY_C1 | PHY Control Register of Port 1 | 220 _H | 180 |
| PHY_S1 | PHY Status Register of Port 1 | 221 _H | 181 |
| PHY_I1_A | PHY Identifier Register of Port 1 (A) | 222 _H | 182 |

Registers Description
Table 52 Registers Overview (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|----------------------------|--|-----------------------|---------------------|
| PHY_I1_B | PHY Identifier Register of Port 1 (B) | 223 _H | 183 |
| ANAP1 | Auto Negotiation Advertisement Register of Port 1 | 224 _H | 184 |
| ANLPA1 | Auto Negotiation Link Partner Ability Register of Port 1 | 225 _H | 185 |
| ANE1 | Auto Negotiation Expansion Register of Port 1 | 226 _H | 186 |
| NPT1 | Next Page Transmit Register of Port 1 | 227 _H | 187 |
| LPNP1 | Link Partner Next Page Register of Port 1 | 228 _H | 188 |
| PHY_C2 | PHY Control Register of Port 2 | 240 _H | 180 |
| PHY_S2 | PHY Status Register of Port 2 | 241 _H | 181 |
| PHY_I2_A | PHY Identifier Register of Port 2 (A) | 242 _H | 182 |
| PHY_I2_B | PHY Identifier Register of Port 2 (B) | 243 _H | 183 |
| ANAP2 | Auto Negotiation Advertisement Register of Port 2 | 244 _H | 184 |
| ANLPA2 | Auto Negotiation Link Partner Ability Register of Port 2 | 245 _H | 185 |
| ANE2 | Auto Negotiation Expansion Register of Port 2 | 246 _H | 186 |
| NPT2 | Next Page Transmit Register of Port 2 | 247 _H | 187 |
| LPNP2 | Link Partner Next Page Register of Port 2 | 248 _H | 188 |
| PHY_C3 | PHY Control Register of Port 3 | 260 _H | 180 |
| PHY_S3 | PHY Status Register of Port 3 | 261 _H | 181 |
| PHY_I3_A | PHY Identifier Register of Port 3 (A) | 262 _H | 182 |
| PHY_I3_B | PHY Identifier Register of Port 3 (B) | 263 _H | 183 |
| ANAP3 | Auto Negotiation Advertisement Register of Port 3 | 264 _H | 184 |
| ANLPA3 | Auto Negotiation Link Partner Ability Register of Port 3 | 265 _H | 185 |
| ANE3 | Auto Negotiation Expansion Register of Port 3 | 266 _H | 186 |
| NPT3 | Next Page Transmit Register of Port 3 | 267 _H | 187 |
| LPNP3 | Link Partner Next Page Register of Port 3 | 268 _H | 188 |
| PHY_C4 | PHY Control Register of Port 4 | 280 _H | 180 |
| PHY_S4 | PHY Status Register of Port 4 | 281 _H | 181 |
| PHY_I4_A | PHY Identifier Register of Port 4 (A) | 282 _H | 182 |
| PHY_I4_B | PHY Identifier Register of Port 4 (B) | 283 _H | 183 |
| ANAP4 | Auto Negotiation Advertisement Register of Port 4 | 284 _H | 184 |
| ANLPA4 | Auto Negotiation Link Partner Ability Register of Port 4 | 285 _H | 185 |
| ANE4 | Auto Negotiation Expansion Register of Port 4 | 286 _H | 186 |
| NPT4 | Next Page Transmit Register of Port 4 | 287 _H | 187 |
| LPNP4 | Link Partner Next Page Register of Port 4 | 288 _H | 188 |

The register is addressed wordwise.

Registers Description
Table 53 Register Access Types

| Mode | Symbol | Description HW | Description SW |
|-------------------------------|--------|---|---|
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| Read only | ro | Register is set by HW (register between input and output -> one cycle delay) | SW can only read this register |
| Read virtual | rv | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the hw, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

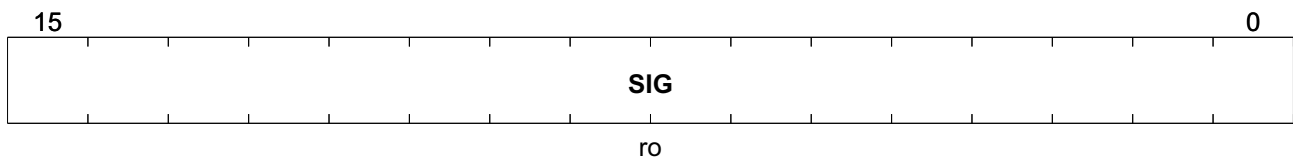
Table 54 Registers Clock Domains

| Clock Short Name | Description |
|------------------|-------------|
| – | – |

4.1 EEPROM Basic Registers

Signature Register

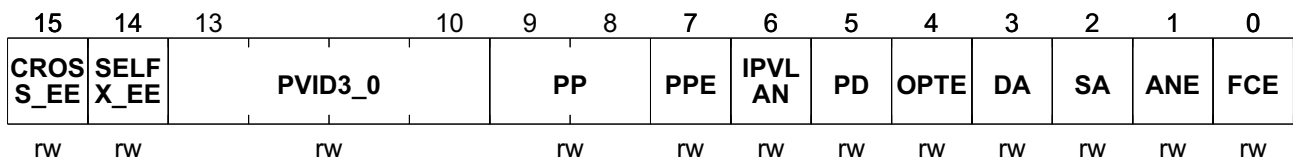
| | | |
|--------------------|-----------------|--------------------|
| SIG | Offset | Reset Value |
| Signature Register | 00 _H | 4154 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| SIG | 15:0 | ro | Signature The value must be 4154 _H . Samurai-6I/6IX (ADM6996I/IX) uses this value to check if the EEPROM is attached. If the value in the EEPROM does not equal to 4154 _H , Samurai-6I/6IX (ADM6996I/IX) will stop loading the EEPROM even if the EEPROM is attached. Samurai-6I/6IX (ADM6996I/IX) will use the default value to initialize. |

P0 Basic Control Register

| | | |
|---------------------------|-----------------|--------------------|
| P0BC | Offset | Reset Value |
| P0 Basic Control Register | 01 _H | 040F _H |



Registers Description

| Field | Bits | Type | Description |
|-----------|-------|------|--|
| CROSS_EE | 15 | rw | Crossover Auto Detect Enable This bit is used together with the value (cross_hw) on the pin EESK/SDC during the power on reset and the value (wait_init) on the pin WAIT_INIT during the normal mode to decide if PHY enables this function. This bit is useless in Port 5. Combine with wait_init and cross_hw, the crossover auto detect capability is summarized as below : {wait_init, cross_hw, cross_ee} Description 1x1 _B This port will enable Crossover Auto Detect Enable function 1x0 _B This port will disable Crossover Auto Detect Enable function 01x _B This port will enable Crossover Auto Detect Enable function 000 _B This port will disable Crossover Auto Detect Enable function 001 _B This port will enable Crossover Auto Detect Enable function |
| SELF_X_EE | 14 | rw | Select FX This bit is used together with the value (p4fx_hw) on the pin P4FX during the power on reset to decide if the PHY operates on the fiber mode. This bit is useless in Port 5. SELF_X_EE can set Port 0, 1, 2, 3 to FX or TX . Port 4 mode is decided by : {p4fx_hw, selfx_ee} Description 1x _B Port 4: Port 4 will operate in the fiber mode 00 _B Port 4: Port 4 will operate in the twisted mode 01 _B Port 4: Port 4 will operate in the fiber mode |
| PVID3_0 | 13:10 | rw | Private VID See 0028 _H ~ 002C _H to find the other PVID [11:4] |
| PP | 9:8 | rw | Port Priority 00 _B Assign packets to Queue 0 01 _B Assign packets to Queue 1 10 _B Assign packets to Queue 2 11 _B Assign packets to Queue 3 |
| PPE | 7 | rw | Port Priority Enable 0 _B The port priority is disabled 1 _B The port priority is enabled |
| IPVLAN | 6 | rw | IP over VLAN PRI This bit gives Switch instruction to check IP or VLAN priority when both priorities happened on coming packet. 0 _B Use the priority bits in the tag header to assign the priority queue 1 _B Use the IP PRI to assign the priority queue |
| PD | 5 | rw | Port Disable 0 _B Port 0, 1, 2, 3, 4: PHY work s normally. Port 5: Port 5 works normally 1 _B Port 0, 1, 2, 3, 4. PHY is disabled. Port 5: Port 5 is forced to link down |
| OPTE | 4 | rw | Output Packet Tagging Enable 0 _B Untagged packets are transmitted 1 _B Tagged packets are transmitted |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| DA | 3 | rw | Duplex Ability It is useless in Port 5. 0 _B Recommend PHY to work in the half duplex mode 1 _B Recommend PHY to work in the full duplex mode |
| SA | 2 | rw | Speed Ability 0 _B Recommend PHY to work in the 10M mode 1 _B Recommend PHY to work in the 100M mode |
| ANE | 1 | rw | Auto Negotiation Enable 0 _B Recommend PHY to work without Auto Negotiation 1 _B Recommend PHY to work with Auto Negotiation, when the value on the pin DUPCOL0 during the power on reset is 1 |
| FCE | 0 | rw | Flow Control Enable 0 _B Recommend MAC to work without Pause or Back Pressure 1 _B In full duplex, recommend MAC to work with Pause when the value on the TXD0 during the power on reset is 1. In half duplex, recommend MAC to work with Back Pressure when the value on the DUPCOL2 during the power on reset is 1 |

Similar Registers

Table 55 Basic Control Registers 1 to 5

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------------|-----------------|-------------|
| P1 | Basic Control Register 1 | 03 _H | |
| P2 | Basic Control Register 2 | 05 _H | |
| P3 | Basic Control Register 3 | 07 _H | |
| P4 | Basic Control Register 4 | 08 _H | |
| P5 | Basic Control Register 5 | 09 _H | |

P0 Extended Control Register

| | | |
|-------------------------------------|-----------------------|-------------------------|
| P0EC | Offset | Reset Value |
| P0 Extended Control Register | 02_H | 0000_H |

| | | | | | | | | | |
|-----|-----------|-----------|--------|-----|-----------|-----------|--------|---|---|
| 15 | 14 | 13 | 12 | 8 | 7 | 6 | 5 | 4 | 0 |
| Res | AD13 5 | LD13 5 | MNA135 | Res | AD02 4 | LD02 4 | MNA024 | | |
| r | rw | rw | rw | r | rw | rw | rw | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | Reserved |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|---|
| AD135 | 14 | rw | Aging Disable P1, P3, and P5. 0 _B Aging function is enabled 1 _B Aging function is disabled |
| LD135 | 13 | rw | Learning Disable P1, P3, and P5. 0 _B Learning function is enabled 1 _B Learning function is disabled |
| MNA135 | 12:8 | rw | Maximum Number of Addresses Learned from the port (P1, P3, and P5). <i>Note: Others = Constrain the number of addresses learned to this value.</i> 00000 _B Doesn't constrain the number of addresses learned |
| Res | 7 | r | Reserved |
| AD024 | 6 | rw | Aging Disable P0, P2, and P4. 0 _B Aging function is enabled. 1 _B Aging function is disabled. |
| LD024 | 5 | rw | Learning Disable P0, P2, and P4. 0 _B Learning function is enabled. 1 _B Learning function is disabled. |
| MNA024 | 4:0 | rw | Maximum Number of Addresses Learned from the port (P0, P2, and P4). <i>Note: Others = Constrain the number of addresses learned to this value.</i> 00000 _B Doesn't constrain the number of addresses learned |

Similar Registers

Table 56 Px_EC Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|------------------------------|-----------------|-------------|
| P1EC | P1 Extended Control Register | 02 _H | |
| P2EC | P2 Extended Control Register | 04 _H | |
| P3EC | P3 Extended Control Register | 04 _H | |
| P4EC | P4 Extended Control Register | 06 _H | |
| P5EC | P5 Extended Control Register | 06 _H | |

System Control Register 0

| | | |
|----------------------------------|-----------------------|-------------------------|
| SC0 | Offset | Reset Value |
| System Control Register 0 | 0A_H | 5902_H |

Registers Description

| | | | | | | | | | | | | | | | | |
|---------|--|--|--|-----|-----|-----------|-----------|-------------|------|---|---|---|------|----|----|---|
| 15 | | | | 12 | | 11 | 10 | 9 | 8 | 7 | 6 | 3 | | 2 | 1 | 0 |
| ERCMPTH | | | | PCR | PCE | RVID 0 | RVID 1 | RVID FFF | DFID | | | | NTTE | TU | PM | |
| rw | | | | rw | rw | rw | rw | rw | rw | | | | rw | rw | rw | |

| Field | Bits | Type | Description |
|---------|-------|------|--|
| ERCMPTH | 15:12 | rw | Earlier Cycles for Transmission It means the earlier cycles for transmission used in Samurai-6I/6IX (ADM6996I/IX). It is for the engineer debug purpose. |
| PCR | 11 | rw | Priority Change Rule 0 _B Use VLAN_PRI field in the matched VLAN filter 1 _B Reverse PRI in the same way as untagged packet |
| PCE | 10 | rw | Priority Change Enable 0 _B Do not change the priority in the tag header 1 _B Change the priority field in the tag header |
| RVID0 | 9 | rw | Replace VID0 0 _B Do not replace 1 _B Replace |
| RVID1 | 8 | rw | Replace VID1 0 _B Do not replace 1 _B Replace |
| RVIDFFF | 7 | rw | Replace VIDFFF 0 _B Do not replace 1 _B Replace |
| DFID | 6:3 | rw | Default FID See Chapter 3.1.14.7 FID and VLAN Boundary for more detail information. |
| NTTE | 2 | rw | New Transmit Tag Enable 0 _B Use old 1 _B Use new |
| TU | 1 | rw | TOS Using 0 _B Use the most significant 6 bits of the TOS field in the IPV4 header to map the priority queue 1 _B Use the most significant 3 bits of the TOS field in the IPV4 header to map the priority queue |
| PM | 0 | rw | PPPOE Manage When the port is configured a PPPOE Only, the port will only transmit the PPPOE packets. But when the packet is a management one, users could configure PPPOE Manage to 1 _B to transmit this packet on the PPPOE Only port even if it is not a PPPOE packet. Samurai-6I/6IX (ADM6996I/IX) identifies packets with Ether-Type = 8863 _H or 8864 _H as the PPPOE packet. |

System Control Register 1

Registers Description

SC1 **Offset** **Reset Value**
System Control Register 1 **0B_H** **8001_H**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|-----|-----|-----|-----|-----|----|------|------|------|------|------|------|----|----|
| DFFD | IF | ASC | SIC | SIM | SIA | CMS | TE | TSIE | CPDC | SVOR | SVOA | SVOS | SVOD | NE | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| DFFD | 15 | rw | Disable Far-End-Fault Detection 0 _B Far-End-Fault detect ion is enabled 1 _B Far-End-Fault detect ion is disabled |
| IF | 14 | rw | Input Filter 0 _B Discard packets directly when storming or the lack of input buffers 1 _B Forward packets to the un-congested port when storming or the lack of input buffers |
| ASC | 13:12 | rw | Additional Snooping Control These bits are used when the packets on the incoming port with the Ethernet destination address = 01005Exxxxxx _H /3333xxxxxx _H are not IGMP_IP/ MLD_IPV/MLD_IPV6 packets and not found in the learning table or the hardware IGMP table. 00 _B As normal multicast packets 01 _B Drop 10 _B Send to CPU if the receiving port is non-CPU port or send to Multicast Portmap if the receiving is the CPU port 11 _B Reserve |
| SIC | 11 | rw | Source Intrusion Condition 0 _B Learning table source violation does not consider the port match 1 _B Learning table source violation takes the port match into consideration |
| SIM | 10 | rw | Source Intrusion Must 0 _B Learning table source violation will be effective in the following conditions.1. The packets are not the management packets.2. The packets are the management packets but Source Violation Over Reserve is 1 _B 1 _B Must follow the learning table source violation rules |
| SIA | 9 | rw | Source Intrusion Action 0 _B Discard 1 _B Send to the CPU port |
| CMS | 8 | rw | Carrier Mask Select 0 _B Mask CRS of 4 Cycles 1 _B Mask CRS of 5 Cycles |
| TE | 7 | rw | Port 3 and Port 4 Trunk Enable 0 _B No trunk is enabled 1 _B Port 3 and Port 4 are trunked |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| TSIE | 6 | rw | Transmit Short IPG Enable 0 _B 96 bits time is used 1 _B 88/96 bits time is used |
| CPDC | 5 | rw | CPU Port Doesn' t Check CPU Port doesn' t check CRC for packets with Special Tag. 0 _B Check 1 _B Doesn' t Check |
| SVOR | 4 | rw | Source Violation Over Reserve This bit is used when the management packet with DA = 0180C20000xx _H violates the source rule. 0 _B Source violation doesn't change the forwarding algorithm 1 _B Source violation will change the forwarding algorithm |
| SVOA | 3 | rw | Source Violation Over ARP/RARP This bit is used when the ARP/RARP packet classified as management violates the source rule. 0 _B Source violation doesn't change the forwarding algorithm 1 _B Source violation will change the forwarding algorithm |
| SVOS | 2 | rw | Source Violation Over Snooping This bit is used when the MLD_IPV6/MLD_IP/IGMP/IP packet classified as management violates the source rule. 0 _B Source violation doesn't change the forwarding algorithm 1 _B Source violation will change the forwarding algorithm |
| SVOD | 1 | rw | Source Violation Over Default This bit is used when the packet that is not the same as the above and is classified as management violates the source rule. 0 _B Source violation doesn't change the forwarding algorithm 1 _B Source violation will change the forwarding algorithm |
| NE | 0 | rw | New EEPROM 0 _B Use old EEPROM functions 1 _B New EEPROM function is enabled |

Multicast Snooping Register

MS Offset Reset Value
Multicast Snooping Register 0C_H 0000_H

| | | | | | | | | | | | | | | | |
|------|-----------|------|--------|-----------|-----------|-----------|-----------|------|-----|------|------|-----------|----|----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCPA | SCPP E | SCPP | SCPTTH | SCPT C | SCPT M | SCPT S | TMI6 P | TMIP | TIP | HIPI | HISE | HIDR E | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Registers Description

| Field | Bits | Type | Description |
|--------|-------|------|--|
| SCPA | 15:14 | rw | Snooping Control Packet Action 00 _B IGMP Portmap is 000000 _B 01 _B IGMP Portmap is the Multicast Portmap 10 _B If the incoming port is not the CPU port, then the IGMP Portmap is the CPU port. If the incoming port is the CPU port, then the IGMP Portmap is the Multicast Portmap except the CPU port 11 _B If the incoming port is not the CPU port, then the Multicast Portmap is the CPU port. If the incoming port is the CPU port, then the Multicast Portmap is the default output ports except the CPU port |
| SCPPE | 13 | rw | Snooping Control Packet Priority Enable 0 _B Disable 1 _B Enable |
| SCPP | 12:11 | rw | Snooping Control Packet Priority 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| SCPTTH | 10:9 | rw | Snooping Control Packet Transmission Tag Handle 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| SCPTC | 8 | rw | Snooping Control Packet Treated as Cross_VLAN Packet 0 _B Doesn't identify 1 _B Identify as the cross_VLAN packet |
| SCPTM | 7 | rw | Snooping Control Packet Treated as Management Packet 0 _B Doesn't identify 1 _B Identify as the management packet |
| SCPTS | 6 | rw | Snooping Control Packet Treated as Span Packet 0 _B Doesn't identify 1 _B Identify as the span packet |
| TMI6P | 5 | rw | Trap MLD_IPV6 Packet 0 _B Doesn't trap 1 _B Trap |
| TMIP | 4 | rw | Trap MLD_IP Packet 0 _B Doesn't trap 1 _B Trap |
| TIP | 3 | rw | Trap IGMP_IP Packet 0 _B Doesn't Trap 1 _B Trap |
| HIPI | 2 | rw | Hardware IGMP Packet Ignore CPU Port 0 _B IGMP packet forwards to CPU also when Hardware IGMP Snooping is enabled 1 _B IGMP packet doesn't forward to CPU when Hardware IGMP Snooping is enabled |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| HISE | 1 | rw | Hardware IGMP Snooping Enable 0 _B Disable Hardware IGMP Snooping 1 _B Enable Hardware IGMP Snooping |
| HIDRE | 0 | rw | Hardware IGMP Default Router Enable 0 _B Disable 1 _B Enable |

ARP/RARP Register

| AR ARP/RARP Register | Offset 0D _H | Reset Value 0000 _H |
|-------------------------|---------------------------|----------------------------------|
|-------------------------|---------------------------|----------------------------------|

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|------|-------|------|--------|-----|-------|-------|-----|-----|----|----|----|
| Res | IMP | UPT | RPT | RAPA | RAPPE | RAPP | RAPOTH | APT | RAPTM | TAPTS | TAP | TRP | | | |
| r | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| Res | 15 | r | Reserved |
| IMP | 14 | rw | IP Multicast Packet Treated as Cross_VLAN packet 0 _B Do not identify 1 _B Identify as the cross_VLAN packet |
| UPT | 13 | rw | Unicast packet Treated as Cross_VLAN packet 0 _B Do not identify 1 _B Identify as the cross_VLAN packet when there is a match in the learning table |
| RPT | 12 | rw | RARP Packet Treated as Cross_VLAN Packet 0 _B Doesn't identify 1 _B Identify as the cross_VLAN packet |
| RAPA | 11:10 | rw | RARP/ARP Packet Action 00 _B ARP/RARP Portmap is 000000 _B 01 _B ARP/RARP Portmap is the Broadcast Portmap 10 _B If the incoming port is not the CPU port, then the ARP/RARP Portmap is the CPU port. If the incoming port is the CPU port, then the ARP/RARP Portmap is the Broadcast Portmap except the CPU port 11 _B If the incoming port is not the CPU port, then the ARP/RARP Portmap is the CPU port. If the incoming port is the CPU port, then the ARP/RARP Portmap is the default output ports except the CPU port |
| RAPPE | 9 | rw | RARP/ARP Packet Priority Enable 0 _B Disable 1 _B Enable |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|--|
| RAPP | 8:7 | rw | RARP/ARP Packet Priority 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| RAPOTH | 6:5 | rw | RARP/ARP Packet Output Tag Handle 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| APT | 4 | rw | ARP Packet Treated as Cross _ VLAN Packet 0 _B Doesn't identify 1 _B Identify as the cross_VLAN packet |
| RAPTM | 3 | rw | RARP/ARP Packet Treated as Management Packet 0 _B Do not identify 1 _B Identify as the management packet |
| TAPTS | 2 | rw | RARP/ARP Packet Treated as Span Packet 0 _B Do not identify 1 _B Identify as the span packet |
| TAP | 1 | rw | Trap ARP Packet 0 _B Do not Trap 1 _B Trap |
| TRP | 0 | rw | Trap RARP Packet 0 _B Do not Trap 1 _B Trap |

VLAN Priority Map Register

VPM Offset **0E_H** Reset Value **FA50_H**
VLAN Priority Map Register

| | | | | | | | | | | | | | | | |
|-----|----|-----|----|-----|----|-----|---|-----|---|-----|---|-----|---|-----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PQ7 | | PQ6 | | PQ5 | | PQ4 | | PQ3 | | PQ2 | | PQ1 | | PQ0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

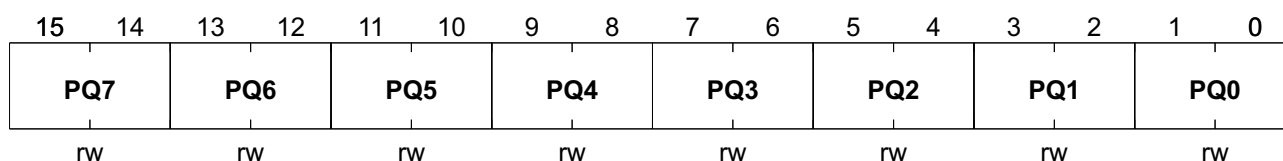
| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ7 | 15:14 | rw | Priority Queue 7 These 2 bits are used as the priority queue when the tagged packets with the user priority = 111 _B are received on the port. 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |

Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ6 | 13:12 | rw | Priority Queue 6 These 2 bits are used as the priority queue when the tagged packets with the user priority = 110 _B are received on the port. |
| PQ5 | 11:10 | rw | Priority Queue 5 These 2 bits are used as the priority queue when the tagged packets with the user priority = 101 _B are received on the port. |
| PQ4 | 9:8 | rw | Priority Queue 4 These 2 bits are used as the priority queue when the tagged packets with the user priority = 100 _B are received on the port. |
| PQ3 | 7:6 | rw | Priority Queue 3 These 2 bits are used as the priority queue when the tagged packets with the user priority = 011 _B are received on the port. |
| PQ2 | 5:4 | rw | Priority Queue 2 These 2 bits are used as the priority queue when the tagged packets with the user priority = 010 _B are received on the port. |
| PQ1 | 3:2 | rw | Priority Queue 1 These 2 bits are used as the priority queue when the tagged packets with the user priority = 001 _B are received on the port. |
| PQ0 | 1:0 | rw | Priority Queue 0 These 2 bits are used as the priority queue when the tagged packets with the user priority = 000 _B are received on the port. |

TOS Priority Map Register

| TPM | Offset | Reset Value |
|---------------------------|-----------------|-------------------|
| TOS Priority Map Register | 0F _H | FA50 _H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ7 | 15:14 | rw | Priority Queue 7 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 111 _B 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| PQ6 | 13:12 | rw | Priority Queue 6 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 110 _B |

Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ5 | 11:10 | rw | Priority Queue 5 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 101 _B |
| PQ4 | 9:8 | rw | Priority Queue 4 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 100 _B |
| PQ3 | 7:6 | rw | Priority Queue 3 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 011 _B |
| PQ2 | 5:4 | rw | Priority Queue 2 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 010 _B |
| PQ1 | 3:2 | rw | Priority Queue 1 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 001 _B |
| PQ0 | 1:0 | rw | Priority Queue 0 These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 000 _B |

System Control Register 2

| SC2 | Offset | Reset Value |
|---------------------------|-----------------|-------------------|
| System Control Register 2 | 10 _H | 0040 _H |

| | | | | | | | | | | | | | | | |
|-------|----|-------|----|-------|----|-------|---|----|----|----|-----|----|----|----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DM_Q3 | | DM_Q2 | | DM_Q1 | | DM_Q0 | | AD | CC | MP | CCD | BD | SE | ST | |
| rw | | rw | | rw | | rw | | rw | rw | rw | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| DM_Q3 | 15:14 | rw | Discard Mode Q3 Discard Mode (Drop scheme for Packets Classified as Q3) . See Chapter 3.1.11 Smart Discard for more detail information. |
| DM_Q2 | 13:12 | rw | Discard Mode Q2 Discard Mode (Drop scheme for Packets Classified as Q2) . See Chapter 3.1.11 Smart Discard for more detail information. |
| DM_Q1 | 11:10 | rw | Discard Mode Q1 Discard Mode (Drop scheme for Packets Classified as Q1) . See Chapter 3.1.11 Smart Discard for more detail information. |
| DM_Q0 | 9:8 | rw | Discard Mode Q0 Discard Mode (Drop scheme for Packets Classified as Q0) . See Chapter 3.1.11 Smart Discard for more detail information. |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| AD | 7 | rw | Aging Disable Useless in Samurai-6I/6IX (ADM6996I/IX) 0 _B Age enable 1 _B Age disable |
| CC | 6 | rw | Rx Clock Change to Tx Clock for GPSI Interface 0 _B Samurai-6I/6IX (ADM6996I/IX) does not use Tx clock to replace Rx clock when Rx clock stops. 1 _B Samurai-6I/6IX (ADM6996I/IX) uses Tx clock to replace Rx clock when Rx clock stops |
| MP | 5 | rw | Multicast Packet Counted into the Storm Counter 0 _B Only broadcast packets are counted into the storming counter 1 _B Multicast and broadcast packets are counted into the storming counter |
| CCD | 4 | rw | CRC Check Disable 0 _B Check CRC 1 _B Do not check CRC |
| BD | 3 | rw | Back Off Disable 0 _B Back-off is enabled 1 _B Back-off is disabled |
| SE | 2 | rw | Storming Enable It is used in ADM6996L/F style storm control. 0 _B Disable broadcast/multicast storm protection. 1 _B Enable broadcast/multicast storm protection. |
| ST | 1:0 | rw | Storming Threshold[1:0] It is used in ADM6996L/F style storm control. |

System Control Register 3

SC3 **Offset** **Reset Value**
System Control Register 3 **11_H** **E300_H**

| | | | | | | | | | | | | | |
|-----|------|------|----|-----|-----|-----|-----|----|-----|-----|----|----|----|
| 15 | 13 | 12 | 11 | 10 | 9 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CPN | STRE | STTE | P | MPL | NSE | TBV | MCE | QO | IPI | ATS | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| CPN | 15:13 | rw | CPU Port Number 000 _B The CPU is attached to Port 0 001 _B The CPU is attached to Port 1 010 _B The CPU is attached to Port 2 011 _B The CPU is attached to Port 3 100 _B The CPU is attached to Port 4 101 _B The CPU is attached to Port 5 111 _B No CPU exists |
| STRE | 12 | rw | Special TAG Receive Enable 0 _B Samurai-6I/6IX (ADM6996I/IX) doesn't identify the Special TAG for the incoming packets 1 _B Samurai-6I/6IX (ADM6996I/IX) identifies the Special TAG for the incoming packets |
| STTE | 11 | rw | Special TAG Transmit Enable 0 _B Samurai-6I/6IX (ADM6996I/IX) does not insert Special TAG for the packets transmitted to the CPU port 1 _B Samurai-6I/6IX (ADM6996I/IX) inserts Special TAG for the packets transmitted to the CPU port. |
| P | 10 | rw | Pause Also add s Speci a I Tag when Special TAG Transmit is enabled . 0 _B Do not add Special Tag on the PAUSE packets 1 _B Add Special Tag in the PAUSE packets |
| MPL | 9:7 | rw | Max Packet Length 000 _B 1518 bytes 001 _B 1536 bytes 010 _B 1664 bytes 110 _B 1522 bytes x11 _B 1784 bytes 10x _B 1784 bytes |
| NSE | 6 | rw | New Storming Enable 0 _B Use the ADM6996L/F style storming control 1 _B Use the Samurai-6I/6IX (ADM6996I/IX) style storming control |
| TBV | 5 | rw | Tag Base VLAN 0 _B Port VLAN 1 _B Tagged VLAN |
| MCE | 4 | rw | MAC Clone Enable 0 _B MAC Clone is disabled 1 _B MAC Clone is enabled |
| QO | 3 | rw | Queue Option It ' s the test for the designer in the queue control. |
| IPI | 2 | rw | Interrupt Polarity Inverter 0 _B The interrupt signal is active pull low 1 _B The interrupt signal is active pull high |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| ATS | 1:0 | rw | Aging Timer Select 00 _B 300 Seconds 01 _B 75 Seconds 10 _B 18 Seconds 11 _B 1 Second |

System Control Register 4

| | | |
|---------------------------|-----------------|-------------------|
| SC4 | Offset | Reset Value |
| System Control Register 4 | 12 _H | 3600 _H |

| | | | | | | | | | | | | | | | |
|----|----------|-----|-----|-----|-----|------|------|------|----|------|-------|------|------|------|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP | DUP COL* | Res | TLE | Res | Res | O5FL | O4FL | O3FL | PI | O2FL | DUAL* | O1FL | LED* | O0FL | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|--------------|-------|------|---|
| DP | 15 | rw | Drop Packet When Excessive Collision Happen 0 _B Do not drop 1 _B Drop |
| DUP_COL_SE P | 14 | rw | Duplex and Col Separate 0 _B Indicate the duplex and collision status at the same time 1 _B Indicate the duplex status only |
| Res | 13:12 | rw | Reserved |
| TLE | 11 | rw | Ten Limit Enable This function works only when Full Flow Control/Half Back Pressure is enabled. 0 _B The switch will not ignore 10 Mbit/s paths even when the ten limit reaches 1 _B The switch will forward packets with Multicast, Broadcast, or Unicast but not learned DA addresses from 100 Mbit/s only to 100 Mbit/s ports and ignore the 10M paths when the ten limit reaches. This function allows the switch to balance the high and the low speed |
| Res | 10 | rw | Reserved |
| Res | 9 | rw | Reserved |
| O5FL | 8 | rw | OLD P5 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |
| O4FL | 7 | rw | OLD P4 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |

Registers Description

| Field | Bits | Type | Description |
|---------------|------|------|---|
| O3FL | 6 | rw | OLD P3 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |
| PI | 5 | rw | Pause Ignore 0 _B Do not ignore Pause packets 1 _B Ignore Pause packets in half duplex or in full duplex when flow control is not enabled |
| O2FL | 4 | rw | OLD P2 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |
| DUAL-COLOR-EE | 3 | rw | Dual Color in MDC / MDIO with CPU See Chapter 3.1.12 LED Display for more detail information. 0 _B Single Color 1 _B Dual Color |
| O1FL | 2 | rw | OLD P1 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |
| LED-ENABLE | 1 | rw | LED Enable 0 _B Disable 1 _B Enable |
| O0FL | 0 | rw | OLD P0 First Lock 0 _B First Lock is disabled 1 _B First Lock is enabled |

Port 0 Security Option

Port Spanning Tree State and Forward Group Port Map.

| | | |
|-------------------------------|-----------------------|-------------------------|
| P0SO | Offset | Reset Value |
| Port 0 Security Option | 13_H | 01D5_H |

| | | | | | | | | | | | | | | |
|-----|----|-----|------|----|----|----|-----|----|-----|----|-----|----|---|---|
| 15 | 14 | 13 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | CP | PSO | STPS | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 | | |
| r | rw | rw | rw | rw | rw | rw | r | rw | r | rw | r | rw | | |

| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15 | r | Reserved |
| CP | 14 | rw | Close Port 0 _B Doesn't close the port 1 _B When port security exists, the port is closed automatically |

Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|---|
| PSO | 13:11 | rw | Port Security Option 001 _B Unknown to CPU 010 _B Discard Unknown 011 _B First Lock 100 _B First Link Lock 101 _B Assign Lock 110 _B Assign Link Lock |
| STPS | 10:9 | rw | Spanning Tree Port Status The Samurai-6I/6IX (ADM6996I/IX) supports 4 port status to support Spanning Tree Protocol . 00 _B Forwarding State. The port acts as the normal mode 01 _B Disabled State . The port entity will not transmit and receive any packets. Learning is disabled in this state 10 _B Learning State . The port entity will only transmit and receive span packets. All other packets are discarded. Learning is enabled for all good frames 11 _B Blocking/Listening. Only the span packets defined by Samurai-6I/6IX (ADM6996I/IX) will be received and transmitted. All other packets are discarded by the port entity. Learning is disabled in this state |
| P5 | 8 | rw | Port 5 is a Member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a Member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a Member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a Member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a Member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a Member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Similar Registers

Table 57 PxSO Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|------------------------|-----------------|-------------|
| P1SO | Port 1 Security Option | 14 _H | |
| P2SO | Port 2 Security Option | 15 _H | |
| P3SO | Port 3 Security Option | 16 _H | |
| P4SO | Port 4 Security Option | 17 _H | |
| P5SO | Port 5 Security Option | 18 _H | |

Unicast Port Map and Forward Group Port Map

| UFGPM | Offset | Reset Value |
|---|-----------------|-------------------|
| Unicast Port Map and Forward Group Port Map | 19 _H | FFD5 _H |

| | | | | | | | | | | | | | | |
|-----|----|--|--|--|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| UP | 14:9 | rw | Unicast Portmap See Chapter 3.1.20 Packet Forwarding for more detail information. |
| P5 | 8 | rw | Port 5 is a Member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a Member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a Member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a Member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a Member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| P0 | 0 | rw | Port 0 is a Member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Broadcast Port Map and Forward Group Port Map

| | | |
|--|-----------------------|-------------------------|
| BFGPM | Offset | Reset Value |
| Broadcast Port Map and Forward Group Port Map | 1A_H | FFD5_H |

| | | | | | | | | | | | | | | | |
|-----|----|--|--|-----------|--|---|-----------|-----------|-----------|-----|-----------|-----|-----------|-----|-----------|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | BP | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | rw | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| BP | 14:9 | rw | Broadcast Portmap See Chapter 3.1.20 Packet Forwarding for more detail information. |
| P5 | 8 | rw | Port 5 is a Member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a Member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a Member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a Member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a Member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a Member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Multicast Port Map and Forward Group Port Map

Registers Description

MFGPM **Offset**
Multicast Port Map and Forward Group Port **1B_H**
Map **Reset Value**
FFD5_H

| | | | | | | | | | | | | | | |
|-----|----|--|--|-----------|---|-----------|-----------|-----------|-----|-----------|-----|-----------|-----|-----------|
| 15 | 14 | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | MP | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | rw | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| MP | 14:9 | rw | Multicast Portmap See Chapter 3.1.20 Packet Forwarding for more detail information. |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Reserve Port Map and Forward Group Port Map

RFGPM **Offset**
Reserve Port Map and Forward Group Port **1C_H**
Map **Reset Value**
FFD5_H

Registers Description

| | | | | | | | | | | | | | | | |
|-----|----|--|--|--|--|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| RP | 14:9 | rw | Reserve Portmap See Chapter 3.1.20 Packet Forwarding for more detail information. |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Packet Identification Option, Forward Group Port Map

| PIOFGPM | Offset | Reset Value |
|--|-----------------|-------------------|
| Packet Identification Option, Forward Group Port Map | 1D _H | FFD5 _H |

| | | | | | | | | | | | | | | | |
|------|------|-------------------|-------------------|-----|------|-----|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSPH | DIVS | DIIP ₆ | DIIP ₅ | DIE | DIIP | DIS | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | r | rw | r | rw | r | rw |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| MSPH | 15 | rw | MLD Snooping Protocol Header 0 _B Protocol Header is 01 _H . 1 _B Protocol Header is 3A _H . |
| DIVS | 14 | rw | Do not Identify VLAN after SNAP 0 _B Identify 1 _B Do not identify |
| DII6P | 13 | rw | Do not Identify IPV6 in PPPOE 0 _B Identify 1 _B Do not identify |
| DIIPS | 12 | rw | Do not Identify IP in PPPOE after SNAP 0 _B Identify 1 _B Do not identify |
| DIE | 11 | rw | Do not Identify Ether-Type = 0x0800, IP VER = 6 as IPV6 packets 0 _B Identify 1 _B Do not identify |
| DIIP | 10 | rw | Do not Identify IP in PPPOE 0 _B Identify 1 _B Do not identify |
| DIS | 9 | rw | Do not Identify SNAP 0 _B Identify 1 _B Do not Identify |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

VLAN Priority Enable and Forward Group Port Map

Registers Description

VPEFGPM

VLAN Priority Enable and Forward Group
Port Map

Offset

1E_H

Reset Value

FFD5_H

| | | | | | | | | | | | | | | |
|-----|----|--|--|-----|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | VPE | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | rw | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| VPE | 14:9 | rw | VLAN Priority Enable 0 _B Do not care the PRI in the tag header 1 _B PRI in the tag header will be taken into priority determination consideration |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a membe |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Service Priority Enable and Forward Group Port Map

SPEFGPM

Service Priority Enable and Forward Group
Port Map

Offset

1F_H

Reset Value

FFD5_H

Registers Description

| | | | | | | | | | | | | | | | |
|-----|----|--|--|--|--|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| SPE | 14:9 | rw | Service Priority Enable 0 _B Don't care IPV4 TOS /IPV6 Traffic Class 1 _B Care IPV4 TOS/IPV6 Traffic for priority decision |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Input Force No Tag and Forward Group Port Map

| | | |
|--|-----------------------|-------------------------|
| IFNTFGPM | Offset | Reset Value |
| Input Force No Tag and Forward Group Port Map | 20_H | FFD5_H |

| | | | | | | | | | | | | | | | |
|-----|----|--|--|--|--|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| IFNTE | 14:9 | rw | Input Force No TAG Enable 0 _B Disabled 1 _B Enabled |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Ingress Filter and Forward Group Port Map

| IFFGPM | Offset | Reset Value |
|---|-----------------|-------------------|
| Ingress Filter and Forward Group Port Map | 21 _H | FFD5 _H |

| | | | | | | | | | | | | | | | |
|-----|----|--|--|--|--|---|----|----|----|-----|----|-----|----|-----|----|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| IFE | 14:9 | rw | Ingress Filter Enable 0 _B Do not filter 1 _B Filter |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

VLAN Security Disable and Forward Group Port Map

| | | |
|---|-----------------------|-------------------------|
| VSDFGPM | Offset | Reset Value |
| VLAN Security Disable and Forward Group Port Map | 22_H | FFD5_H |

| | | | | | | | | | | | | | | | |
|-----|----|--|--|--|--|---|-----------|-----------|-----------|-----|-----------|-----|-----------|-----|-----------|
| 15 | 14 | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | | | | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | | | | rw | rw | rw | r | rw | r | rw | r | rw |

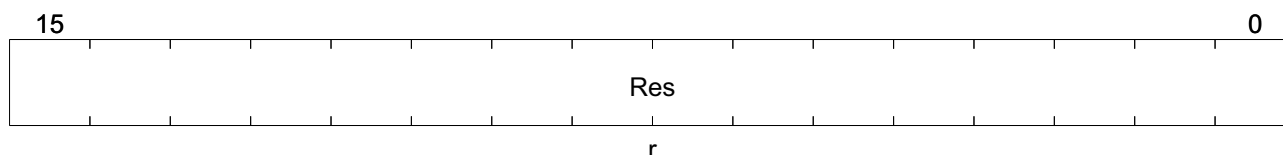
| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15 | r | Reserved |
| VSD | 14:9 | rw | VLAN Security Disable 0 _B Do not disable 1 _B Disable |
| P5 | 8 | rw | Port 5 is a member of the Forwarding Group 0 _B Port 5 is not a member 1 _B Port 5 is a member |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| P4 | 7 | rw | Port 4 is a member of the Forwarding Group 0 _B Port 4 is not a member 1 _B Port 4 is a member |
| P3 | 6 | rw | Port 3 is a member of the Forwarding Group 0 _B Port 3 is not a member 1 _B Port 3 is a member |
| Res | 5 | r | Reserved |
| P2 | 4 | rw | Port 2 is a member of the Forwarding Group 0 _B Port 2 is not a member 1 _B Port 2 is a member |
| Res | 3 | r | Reserved |
| P1 | 2 | rw | Port 1 is a member of the Forwarding Group 0 _B Port 1 is not a member 1 _B Port 1 is a member |
| Res | 1 | r | Reserved |
| P0 | 0 | rw | Port 0 is a member of the Forwarding Group 0 _B Port 0 is not a member 1 _B Port 0 is a member |

Buffer Threshold Register 0

| | | |
|------------------------------------|-----------------------|-------------------------|
| BT0 | Offset | Reset Value |
| Buffer Threshold Register 0 | 23_H | 0000_H |

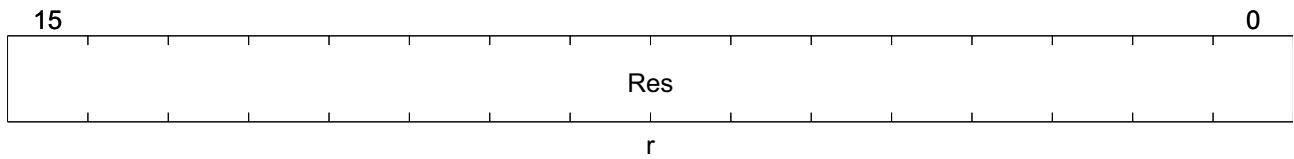


| Field | Bits | Type | Description |
|-------|------|------|-----------------|
| Res | 15:0 | r | Reserved |

Buffer Threshold Register 1

| | | |
|------------------------------------|-----------------------|-------------------------|
| BT1 | Offset | Reset Value |
| Buffer Threshold Register 1 | 24_H | 0000_H |

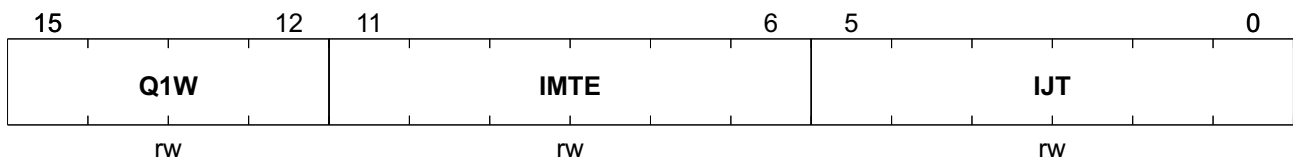
Registers Description



| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:0 | r | Reserved |

IGMP/MLDTRAP Enable and Input Jam Threshold Register

| | | |
|--|-----------------|-------------------|
| IMEIJT | Offset | Reset Value |
| IGMP/MLDTRAP Enable and Input Jam Threshold Register | 25 _H | 1000 _H |

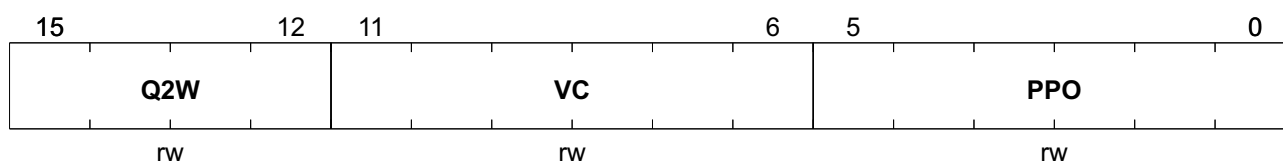


| Field | Bits | Type | Description |
|-------|-------|------|--|
| Q1W | 15:12 | rw | Queue 1 Weight See Chapter 3.1.15 Priority Queue for more detail information. |
| IMTE | 11:6 | rw | IGMP/MLD Trap Enable It is a per port function. 0 _B The port does not enable its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useless in this port 1 _B The port enables its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useful in this port |
| IJT | 5:0 | rw | Input Jam Threshold |

Queue 2 Weight, VID Exist Check, and PPPOE Port Only

| | | |
|--|-----------------|-------------------|
| Q2WVECPO | Offset | Reset Value |
| Queue 2 Weight, VID Exist Check, and PPPOE Port Only | 26 _H | 1000 _H |

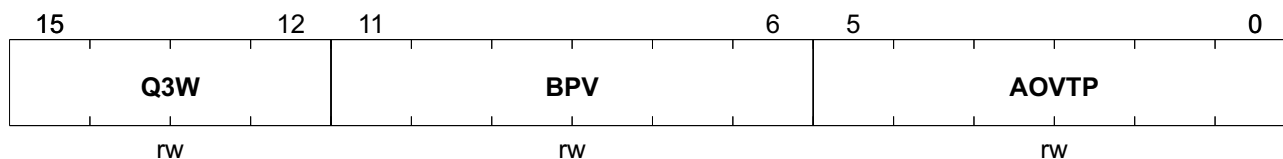
Registers Description



| Field | Bits | Type | Description |
|-------|-------|------|--|
| Q2W | 15:12 | rw | Queue 2 Weight See Chapter 3.1.15 Priority Queue for more detail information. |
| VC | 11:6 | rw | VID Check It is a per port function. 0 _B Do not check 1 _B check |
| PPO | 5:0 | rw | PPPOE Port Only It's a per port function 0 _B The port is not a PPPOE Only port 1 _B The port is a PPPOE Only port |

Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged

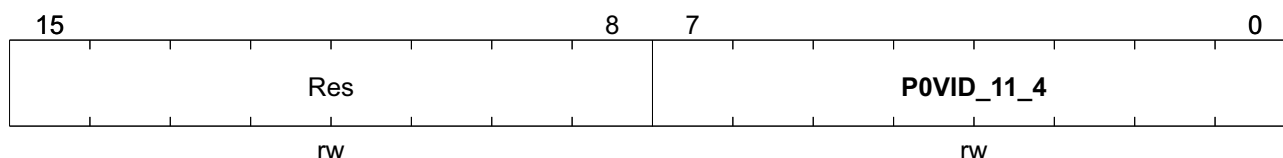
Q3WBPVAO Offset **Reset Value**
Queue 3 Weight, Back to Port VLAN, and **27_H** **1000_H**
Admit Only VLAN-Tagged



| Field | Bits | Type | Description |
|-------|-------|------|--|
| Q3W | 15:12 | rw | Queue 3 Weight See Chapter 3.1.15 Priority Queue for more detail information. |
| BPV | 11:6 | rw | Back To Port VLAN It is a per port function 0 _B Do not back to Port VLAN 1 _B Back to Port VLAN |
| AOVTP | 5:0 | rw | Admit Only VLAN_Tagged Packet It is a per port function 0 _B The port Do not check if the packets are VLAN-Tagged 1 _B The port drops the packets that carry no VID. (That is Untagged Packets or Priority-Tagged Packets) |

Input Double Tag Enable, and P0VID[11:4]

IDTEP Offset **Reset Value**
Input Double Tag Enable, and P0VID[11:4] **28_H** **0000_H**

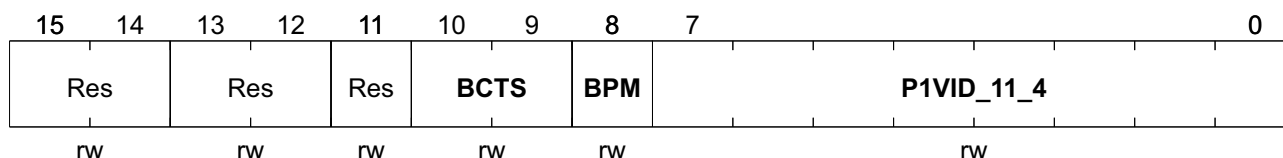


| Field | Bits | Type | Description |
|------------|------|------|--|
| Res | 15:8 | rw | Reserved |
| P0VID_11_4 | 7:0 | rw | P0VID[11:4] VID bit 11 ~ 4 fo Port 0 |

Registers Description

Output Double Tag Enable, and P1VID[11:4]

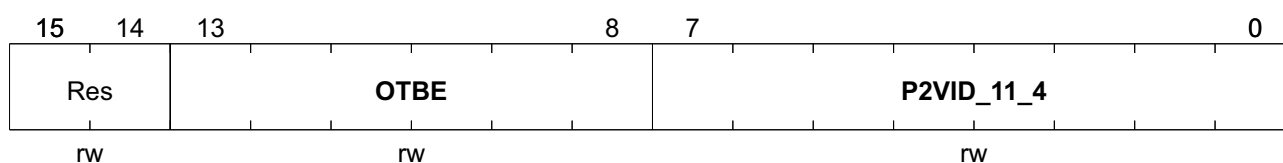
ODTEP **Offset**
Output Double Tag Enable, and P1VID[11:4] **Reset Value**
29_H **0000_H**



| Field | Bits | Type | Description |
|------------|-------|------|--|
| Res | 15:14 | rw | Reserved |
| Res | 13:12 | rw | Reserved |
| Res | 11 | rw | Reserved |
| BCTS | 10:9 | rw | Bandwidth Control Timer Select 00 _B 8 ms, 64Kbps step, apply to 64Kbps~2.2Mbps 01 _B 1 ms, 512Kbps step, apply to 512Kbps~18Mbps 10 _B 40 us, 200Kbps step, apply to 200Kbps~100Mbps 11 _B 500 us, 16Kbps step, apply to 16Kbps~32Mbps |
| BPM | 8 | rw | Back Pressure Mechanism 0 _B Exit collision state when CRS goes low 1 _B Exit collision state when RXDV goes low |
| P1VID_11_4 | 7:0 | rw | P1VID[11:4] VID bit 11 ~ 4 of Port 1. |

Output Tag Bypass, and P2VID[11:4]

OTBP **Offset**
Output Tag Bypass, and P2VID[11:4] **Reset Value**
2A_H **3F00_H**



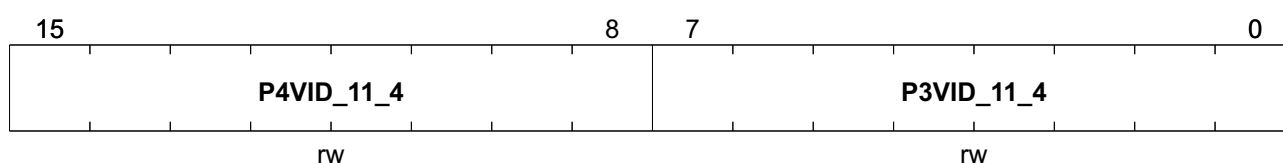
| Field | Bits | Type | Description |
|-------|-------|------|---|
| Res | 15:14 | rw | Reserved |
| OTBE | 13:8 | rw | Output Tag Bypass Enable It's a per port function. See Chapter 3.1.14.12 Egress Tag Rule for more detail information. |

Registers Description

| Field | Bits | Type | Description |
|------------|------|------|---|
| P2VID_11_4 | 7:0 | rw | P2VID[11:4] VID bit 11 ~ 4 of Port 2. |

P3VID[11:4], and P4VID[11:4]

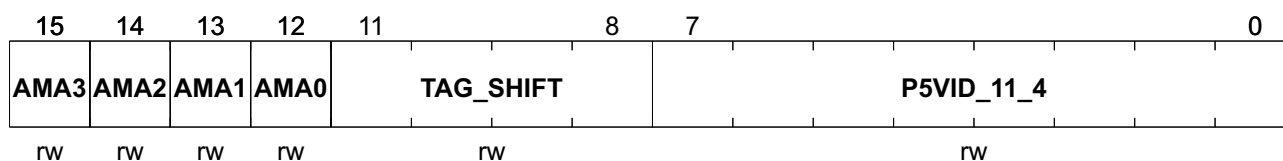
| | | |
|---|--|---|
| P11_4 P3VID[11:4], and P4VID[11:4] | Offset 2B_H | Reset Value 0000_H |
|---|--|---|



| Field | Bits | Type | Description |
|------------|------|------|---|
| P4VID_11_4 | 15:8 | rw | P4VID[11:4] VID bit 11 ~ 4 of Port 4. |
| P3VID_11_4 | 7:0 | rw | P3VID[11:4] VID bit 11 ~ 4 of Port 3. |

Reserved Address Control, and P5VID[11:4]

| | | |
|---|--|---|
| RACP Reserved Address Control, and P5VID[11:4] | Offset 2C_H | Reset Value D000_H |
|---|--|---|



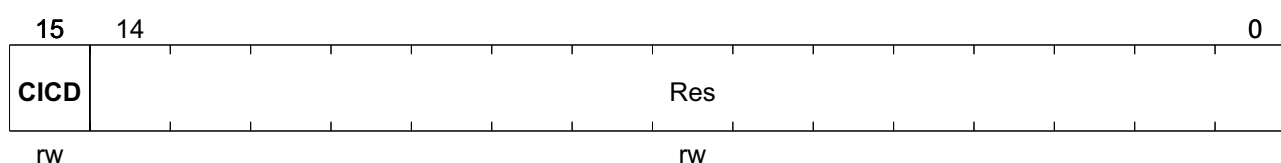
| Field | Bits | Type | Description |
|-----------|------|------|---|
| AMA3 | 15 | rw | Action of MAC Address 3 The Action of MAC Address = 0180C2000010 _H ~ 0180C20000FF _H |
| AMA2 | 14 | rw | Action of MAC Address 2 The Action of MAC Address = 0180C2000002 _H ~ 0180C200000F _H |
| AMA1 | 13 | rw | Action of MAC Address 1 The Action of MAC Address = 0180C2000001 _H |
| AMA0 | 12 | rw | Action of MAC Address 0 The Action of MAC Address = 0180C2000000 _H |
| TAG_SHIFT | 11:8 | rw | Tag Shift |

Registers Description

| Field | Bits | Type | Description |
|------------|------|------|--|
| P5VID_11_4 | 7:0 | rw | P5VID[11:4] VID bit 11 ~ 4 of Port 5 |

PHY Control Register

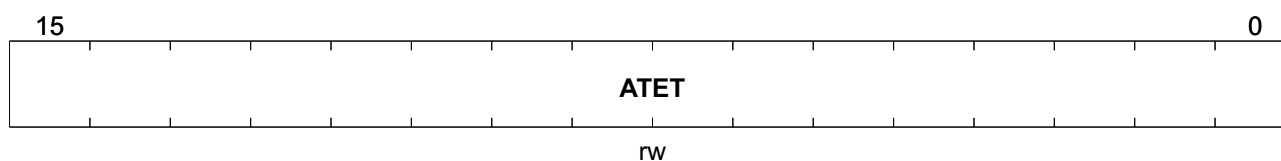
| | | |
|-------------------------------------|----------------------------------|---|
| PHYC PHY Control Register | Offset 2D _H | Reset Value 4442 _H |
|-------------------------------------|----------------------------------|---|



| Field | Bits | Type | Description |
|-------|------|------|--|
| CICD | 15 | rw | Chip ID Check Disable 0 _B Check CHIP ID in 32 bit SDC/SDO 1 _B Do not check CHIP ID in 32 bit SDC/SDIO |
| Res | 14:0 | rw | Reserved |

ADM TAG Ether Type

| | | |
|-----------------------------------|----------------------------------|---|
| ATET ADM TAG Ether Type | Offset 2E _H | Reset Value 0000 _H |
|-----------------------------------|----------------------------------|---|

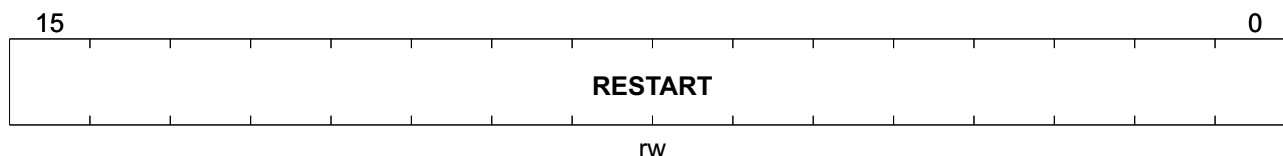


| Field | Bits | Type | Description |
|-------|------|------|--|
| ATET | 15:0 | rw | ADM TAG Ether Type This value is used by the user to define their Ether-Type. When Special Tag Receive is enabled, Samurai-6I/6IX (ADM6996I/IX) checks the packets on the CPU port to see if the two bytes following the SA are the same as ADM TAG Ether Type . If they are different, Samurai-6I/6IX (ADM6996I/IX) bypasses the Special Tag. If the same, Samurai-6I/6IX (ADM6996I/IX) will use the value in the Special Tag to do switching decisions . |

Registers Description

PHY Restart Register

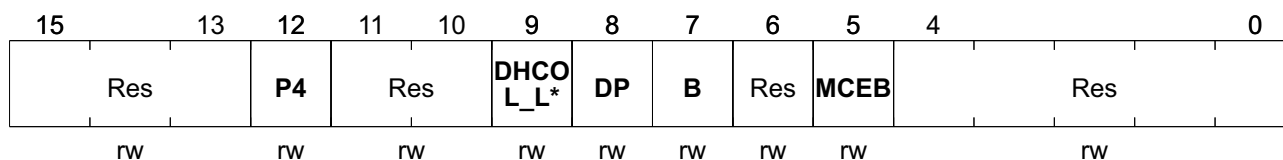
PR Offset **Reset Value**
PHY Restart Register **2F_H** **0000_H**



| Field | Bits | Type | Description |
|---------|------|------|--|
| RESTART | 15:0 | rw | Restart Samurai-6I/6IX (ADM6996I/IX) writes this register to restart all the PHYs in the switch. The value written is not important. |

Miscellaneous Register

MISC Offset **Reset Value**
Miscellaneous Register **30_H** **0987_H**



| Field | Bits | Type | Description |
|--------------|-------|------|---|
| Res | 15:13 | rw | Reserved |
| P4 | 12 | rw | Port 4 LED Mode 0 _B LinkAct/DupCol/Speed. 1 _B Link/Act/Speed. |
| Res | 11:10 | rw | Reserved |
| DHCOL_LED_EN | 9 | rw | Dual Speed Hub COL_LED Enable 0 _B Normal LED display. 1 _B Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED. |
| DP | 8 | rw | Drop Packets Drop packets when the link partner does not follow the PAUSE protocol. 0 _B Disable. 1 _B Enable to drop packets. |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| B | 7 | rw | BYPASS Bypass Tag/Untag function. 0 _B Disable. 1 _B Enable to bypass Tag/Untag function |
| Res | 6 | rw | Reserved |
| MCEB | 5 | rw | MAC Clone Enable Bits Select 0 _B Select 1 bit MAC Clone function. 1 _B Select 2 bits MAC Clone function. |
| Res | 4:0 | rw | Reserved |

Basic Bandwidth Control Register 0

BBC0 Offset **31_H** Reset Value **0000_H**
Basic Bandwidth Control Register 0

| | | | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|----|----|---|---|
| 15 | 14 | 12 | 11 | 10 | 8 | 7 | 6 | 4 | 3 | 2 | 0 |
| R3BW_TH1 | R3BW_TH0 | R2BW_TH1 | R2BW_TH0 | R1BW_TH1 | R1BW_TH0 | R0BW_TH1 | R0BW_TH0 | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | |

| Field | Bits | Type | Description |
|----------|-------|------|---|
| R3BW_TH1 | 15 | rw | Port 3 Receive Bandwidth Maximum[3]. See register 0033 _H , P3RBCE for more detail. |
| R3BW_TH0 | 14:12 | rw | Port 3 Receive Bandwidth Configuration See register 0033 _H , P3RBCE for more detail. |
| R2BW_TH1 | 11 | rw | Port 2 Receive Bandwidth Maximum[3]. See register 0033 _H , P2RBCE for more detail. |
| R2BW_TH0 | 10:8 | rw | Port 2 Receive Bandwidth Configuration See register 0033 _H , P2RBCE for more detail. |
| R1BW_TH1 | 7 | rw | Port 1 Receive Bandwidth Maximum[3]. See register 0033 _H , P1RBCE for more detail. |
| R1BW_TH0 | 6:4 | rw | Port 1 Receive Bandwidth Configuration See register 0033 _H , P1RBCE for more detail. |
| R0BW_TH1 | 3 | rw | Port 0 Receive Bandwidth Maximum[3]. See register 0033 _H , P0RBCE for more detail. |
| R0BW_TH0 | 2:0 | rw | Port 0 Receive Bandwidth Configuration See register 0033 _H , P0RBCE for more detail. |

Basic Bandwidth Control Register 1

BBC1 Offset **32_H** Reset Value **0000_H**
Basic Bandwidth Control Register 1

| | | | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|----|----|---|---|
| 15 | 14 | 12 | 11 | 10 | 8 | 7 | 6 | 4 | 3 | 2 | 0 |
| T1BW_TH1 | T1BW_TH0 | T0BW_TH1 | T0BW_TH0 | R5BW_TH1 | R5BW_TH0 | R4BW_TH1 | R4BW_TH0 | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | |

Registers Description

| Field | Bits | Type | Description |
|----------|-------|------|---|
| T1BW_TH1 | 15 | rw | Port 1 Transmit Bandwidth Maximum[3]. See register 0033 _H , P1TBCE for more detail. |
| T1BW_TH0 | 14:12 | rw | Port 1 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P1TBCE for more detail. |
| T0BW_TH1 | 11 | rw | Port 0 Transmit Bandwidth Maximum[3]. See register 0033 _H , P0TBCE for more detail. |
| T0BW_TH0 | 10:8 | rw | Port 0 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P0TBCE for more detail. |
| R5BW_TH1 | 7 | rw | Port 5 Receive Bandwidth Maximum[3]. See register 0033 _H , P5RBCE for more detail. |
| R5BW_TH0 | 6:4 | rw | Port 5 Receive Bandwidth Configuration See register 0033 _H , P5RBCE for more detail. |
| R4BW_TH1 | 3 | rw | Port 4 Receive Bandwidth Maximum[3]. See register 0033 _H , P4RBCE for more detail. |
| R4BW_TH0 | 2:0 | rw | Port 4 Receive Bandwidth Configuration See register 0033 _H , P4RBCE for more detail. |

Bandwidth Control Enable Register

| | | |
|--|-----------------------|-------------------------|
| BCE | Offset | Reset Value |
| Bandwidth Control Enable Register | 33_H | 0000_H |

| | | | | | | | | | | | | | | | |
|------|-----|-----|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IPCP | CLC | Res | ANBCE | P5TBCE | P4TBCE | P3TBCE | P5RBCE | P4RBCE | P3RBCE | P2TBCE | P2RBCE | P1TBCE | P1RBCE | P0TBCE | P0RBCE |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|---|
| IPCP | 15 | rw | Invert P4 Clock in PCS 0 _D Disable 1 _D Enable |
| CLC | 14 | rw | Check the Length of CRS 0 _D Enable 1 _D Disable |
| Res | 13 | rw | Reserved |
| ANBCE | 12 | rw | Samurai-6I/6IX (ADM6996I/IX) New Bandwidth Control Enable 0 _B Disable 1 _B Enable |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|---|
| P5TBCE | 11 | rw | Port 5 Transmit Bandwidth Control Enable The transmit bandwidth is { T5BW_TH3 , T5BW_TH2 , T5BW_TH1 , T5BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P4TBCE | 10 | rw | Port 4 Transmit Bandwidth Control Enable The transmit bandwidth is { T4BW_TH3 , T4BW_TH2 , T4BW_TH1 , T4BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P3TBCE | 9 | rw | Port 3 Transmit Bandwidth Control Enable The transmit bandwidth is { T3BW_TH3 , T3BW_TH2 , T3BW_TH1 , T3BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P5RBCE | 8 | rw | Port 5 Receive Bandwidth Control Enable The receive bandwidth is { R5BW_TH3 , R5BW_TH2 , R5BW_TH1 , R5BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P4RBCE | 7 | rw | Port 4 Receive Bandwidth Control Enable The receive bandwidth is { R4BW_TH3 , R4BW_TH2 , R4BW_TH1 , R4BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P3RBCE | 6 | rw | Port 3 Receive Bandwidth Control Enable The receive bandwidth is { R3BW_TH3 , R3BW_TH2 , R3BW_TH1 , R3BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P2TBCE | 5 | rw | Port 2 Transmit Bandwidth Control Enable The transmit bandwidth is { T2BW_TH3 , T2BW_TH2 , T2BW_TH1 , T2BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P2RBCE | 4 | rw | Port 2 Receive Bandwidth Control Enable The receive bandwidth is { R2BW_TH3 , R2BW_TH2 , R2BW_TH1 , R2BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P1TBCE | 3 | rw | Port 1 Transmit Bandwidth Control Enable The transmit bandwidth is { T1BW_TH3 , T1BW_TH2 , T1BW_TH1 , T1BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|---|
| P1RBCE | 2 | rw | Port 1 Receive Bandwidth Control Enable The receive bandwidth is { R1BW_TH3 , R1BW_TH2 , R1BW_TH1 , R1BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P0TBCE | 1 | rw | Port 0 Transmit Bandwidth Control Enable The transmit bandwidth is { T0BW_TH3 , T0BW_TH2 , T0BW_TH1 , T0BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |
| P0RBCE | 0 | rw | Port 0 Receive Bandwidth Control Enable The receive bandwidth is { R0BW_TH3 , R0BW_TH2 , R0BW_TH1 , R0BW_TH0 , 000000 _B } kbit/s. K = 1000. 0 _B Disable 1 _B Enable |

Extended Bandwidth Control Register 0

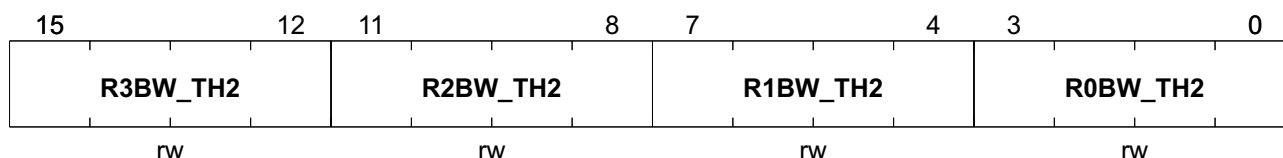
| | | |
|--|-----------------------|-------------------------|
| EBC0 | Offset | Reset Value |
| Extended Bandwidth Control Register 0 | 34_H | 0000_H |

| | | | | | | | | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----|----|---|---|
| 15 | 14 | 12 | 11 | 10 | 8 | 7 | 6 | 4 | 3 | 2 | 0 |
| T5BW_TH1 | T5BW_TH0 | T4BW_TH1 | T4BW_TH0 | T3BW_TH1 | T3BW_TH0 | T2BW_TH1 | T2BW_TH0 | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | |

| Field | Bits | Type | Description |
|----------|-------|------|---|
| T5BW_TH1 | 15 | rw | Port 5 Transmit Bandwidth Maximum[3]. See register 0033 _H , P5TBCE for more detail. |
| T5BW_TH0 | 14:12 | rw | Port 5 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P5TBCE for more detail. |
| T4BW_TH1 | 11 | rw | Port 4 Transmit Bandwidth Maximum[3]. See register 0033 _H , P4TBCE for more detail. |
| T4BW_TH0 | 10:8 | rw | Port 4 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P4TBCE for more detail. |
| T3BW_TH1 | 7 | rw | Port 3 Transmit Bandwidth Maximum[3]. See register 0033 _H , P3TBCE for more detail. |
| T3BW_TH0 | 6:4 | rw | Port 3 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P3TBCE for more detail. |
| T2BW_TH1 | 3 | rw | Port 2 Transmit Bandwidth Maximum[3]. See register 0033 _H , P2TBCE for more detail. |
| T2BW_TH0 | 2:0 | rw | Port 2 Transmit Bandwidth Maximum[2:0]. See register 0033 _H , P2TBCE for more detail. |

Extended Bandwidth Control Register 1

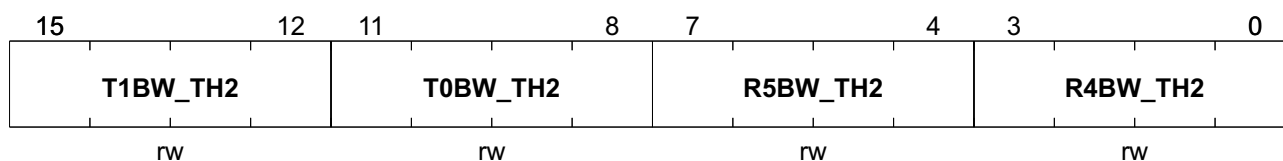
EBC1 **Extended Bandwidth Control Register 1** **Offset** **35_H** **Reset Value** **0000_H**



| Field | Bits | Type | Description |
|----------|-------|------|---|
| R3BW_TH2 | 15:12 | rw | Port 3 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P3RBCE for more detail. |
| R2BW_TH2 | 11:8 | rw | Port 2 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P2RBCE for more detail. |
| R1BW_TH2 | 7:4 | rw | Port 1 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P1RBCE for more detail. |
| R0BW_TH2 | 3:0 | rw | Port 0 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P0RBCE for more detail. |

Extended Bandwidth Control Register 2

EBC2 **Extended Bandwidth Control Register 2** **Offset** **36_H** **Reset Value** **0000_H**



| Field | Bits | Type | Description |
|----------|-------|------|--|
| T1BW_TH2 | 15:12 | rw | Port 1 Transmit Bandwidth Maximum[7:4] See register 0033 _H , P1TBCE for more detail. |
| T0BW_TH2 | 11:8 | rw | Port 0 Transmit Bandwidth Maximum[7:4]. See register 0033 _H , P0TBCE for more detail. |
| R5BW_TH2 | 7:4 | rw | Port 5 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P5RBCE for more detail. |
| R4BW_TH2 | 3:0 | rw | Port 4 Receive Bandwidth Maximum[7:4]. See register 0033 _H , P4RBCE for more detail. |

Extended Bandwidth Control Register 3

EBC3 **Extended Bandwidth Control Register 3** **Offset** **37_H** **Reset Value** **0000_H**

| | | | | | | | | |
|----------|----|----|---|----------|---|----------|---|----------|
| 15 | 12 | 11 | 8 | 7 | 4 | 3 | 0 | |
| T5BW_TH2 | | | | T4BW_TH2 | | T3BW_TH2 | | T2BW_TH2 |
| rw | | | | rw | | rw | | rw |

| Field | Bits | Type | Description |
|----------|-------|------|--|
| T5BW_TH2 | 15:12 | rw | Port 5 Transmit Bandwidth Maximum[7:4]. See register 0033 _H , P5TBCE for more detail. |
| T4BW_TH2 | 11:8 | rw | Port 4 Transmit Bandwidth Maximum[7:4]. See register 0033 _H , P4TBCE for more detail. |
| T3BW_TH2 | 7:4 | rw | Port 3 Transmit Bandwidth Maximum[7:4]. See register 0033 _H , P3TBCE for more detail. |
| T2BW_TH2 | 3:0 | rw | Port 2 Transmit Bandwidth Maximum[7:4]. See register 0033 _H , P2TBCE for more detail. |

Extended Bandwidth Control Register 4

EBC4 **Extended Bandwidth Control Register 4** **Offset** **38_H** **Reset Value** **0000_H**

| | | | | | | | | | | |
|------------|----------|----|----------|---|----------|---|----------|---|----------|---|
| 15 | 14 | 12 | 11 | 9 | 8 | 6 | 5 | 3 | 2 | 0 |
| FMDI X0 | R4BW_TH3 | | R3BW_TH3 | | R2BW_TH3 | | R1BW_TH3 | | R0BW_TH3 | |
| rw | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|----------|-------|------|--|
| FMDIX0 | 15 | rw | Port 0 MDIX Control It is useful when Port 0 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 _B Using MDI 1 _B Using MDIX |
| R4BW_TH3 | 14:12 | rw | Port 4 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P4RBCE for more detail. |
| R3BW_TH3 | 11:9 | rw | Port 3 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P3RBCE for more detail. |

Registers Description

| Field | Bits | Type | Description |
|----------|------|------|--|
| R2BW_TH3 | 8:6 | rw | Port 2 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P2RBCE for more detail. |
| R1BW_TH3 | 5:3 | rw | Port 1 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P1RBCE for more detail. |
| R0BW_TH3 | 2:0 | rw | Port 0 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P0RBCE for more detail. |

Extended Bandwidth Control Register 5

| | | |
|--|-----------------------|-------------------------|
| EBC5 | Offset | Reset Value |
| Extended Bandwidth Control Register 5 | 39_H | 0000_H |

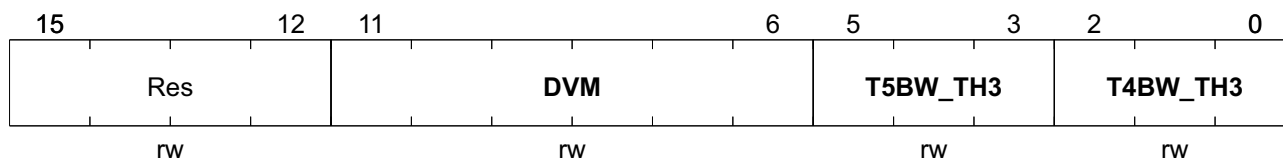
| | | | | | | | | | | |
|---------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|---|---|---|---|
| 15 | 14 | 12 | 11 | 9 | 8 | 6 | 5 | 3 | 2 | 0 |
| FMDIX1 | T3BW_TH3 | T2BW_TH3 | T1BW_TH3 | T0BW_TH3 | R5BW_TH3 | | | | | |
| r | rw | rw | rw | rw | rw | | | | | |

| Field | Bits | Type | Description |
|----------|-------|------|--|
| FMDIX1 | 15 | r | Port 1 MDIX Control It is useful when Port 1 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 _B Using MDI 1 _B Using MDIX |
| T3BW_TH3 | 14:12 | rw | Port 3 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P3TBCE for more detail. |
| T2BW_TH3 | 11:9 | rw | Port 2 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P2TBCE for more detail. |
| T1BW_TH3 | 8:6 | rw | Port 1 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P1TBCE for more detail. |
| T0BW_TH3 | 5:3 | rw | Port 0 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P0TBCE for more detail. |
| R5BW_TH3 | 2:0 | rw | Port 5 Receive Bandwidth Maximum[10:8]. See register 0033 _H , P5RBCE for more detail. |

Default VLAN Member and Extended Bandwidth Control Register 6

| | | |
|--|-----------------------|-------------------------|
| DVMEBC6 | Offset | Reset Value |
| Default VLAN Member and Extended Bandwidth Control Register 6 | 3A_H | 0FC0_H |

Registers Description



| Field | Bits | Type | Description |
|----------|-------|------|---|
| Res | 15:12 | rw | Reserved |
| DVM | 11:6 | rw | Default VLAN Member |
| T5BW_TH3 | 5:3 | rw | Port 5 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P5TBCE for more detail. |
| T4BW_TH3 | 2:0 | rw | Port 4 Transmit Bandwidth Maximum[10:8]. See register 0033 _H , P4TBCE for more detail. |

New Storm Register 0

| | | |
|-----------------------------|-----------------------|-------------------------|
| NS0 | Offset | Reset Value |
| New Storm Register 0 | 3B_H | 0000_H |

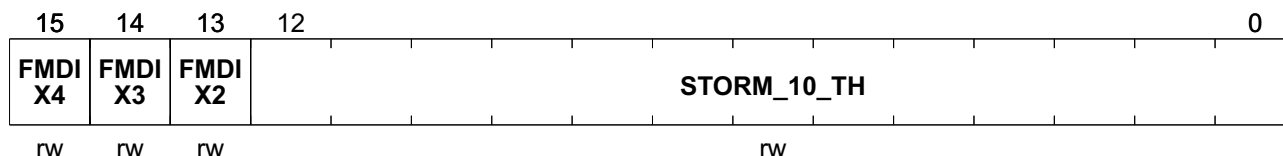


| Field | Bits | Type | Description |
|-------------------|------|------|--|
| Res | 15 | r | Reserved |
| STORM_DRO P_EN | 14 | rw | Storm Drop Enable 0 _B Do not drop in the storming period 1 _B Drop in the storming period |
| STORM_EN | 13 | rw | Storm Enable 0 _B Disable Samurai-6I/6IX (ADM6996I/IX) style broadcast storm protection 1 _B Enable Samurai-6I/6IX (ADM6996I/IX) style broadcast storm protection |
| STORM_100_ TH | 12:0 | rw | 100M Threshold See Chapter 3.1.9 Broadcast/Multicast Storm for more detail information. It is used when all ports link up in the 100M. The upper bound is reached when the number of the packets received during the 50 ms is over 100M Threshold. |

New Storm Register 1

Registers Description

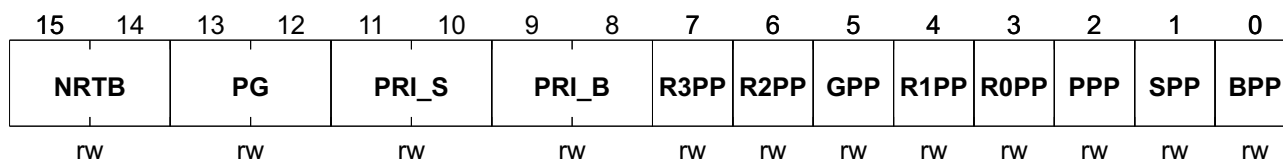
NS1 **Offset** **Reset Value**
New Storm Register 1 **3C_H** **0000_H**



| Field | Bits | Type | Description |
|-------------|------|------|--|
| FMDIX4 | 15 | rw | Port 4 MDIX Control It is useful when Port 4Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 _B Using MDI 1 _B Using MDIX |
| FMDIX3 | 14 | rw | Port 3 MDIX Control It is useful when Port 3Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 _B Using MDI 1 _B Using MDIX |
| FMDIX2 | 13 | rw | Port 2 MDIX Control It is useful when Port 2 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 _B Using MDI 1 _B Using MDIX |
| STORM_10_TH | 12:0 | rw | 10M Threshold See Chapter 3.1.9 Broadcast/Multicast Storm for more detail information. It is used when one of ports link up in the 10M. The upper bound is reached when the number of the packets received during the 50 ms is over 10M Threshold. |

New Reserve Address Control Register 0

NRAC0 **Offset** **Reset Value**
New Reserve Address Control Register 0 **3D_H** **00FD_H**



Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|---|
| NRTB | 15:14 | rw | New Reserve TXTAG for BPDU 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| PG | 13:12 | rw | PRI for GXP 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| PRI_S | 11:10 | rw | PRI for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| PRI_B | 9:8 | rw | PRI for BPDU 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |
| R3PP | 7 | rw | RESER_R3 Pass Portmap 0 _B RESER_R3 Pass Portmap is 000000 _B 1 _B RESER_R3 Pass Portmap is 111111 _B |
| R2PP | 6 | rw | RESER_R2 Pass Portmap 0 _B RESER_R2 Pass Portmap is 000000 _B 1 _B RESER_R2 Pass Portmap is 111111 _B |
| GPP | 5 | rw | GXP Pass Portmap 0 _B GXP Pass Portmap is 000000 _B 1 _B GXP Pass Portmap is 111111 _B |
| R1PP | 4 | rw | RESER_R1 Pass Portmap 0 _B RESER_R1 Pass Portmap is 000000 _B 1 _B RESER_R1 Pass Portmap is 111111 _B |
| R0PP | 3 | rw | RESER_R0 Pass Portmap 0 _B RESER_R0 Pass Portmap is 000000 _B 1 _B RESER_R0 Pass Portmap is 111111 _B |
| PPP | 2 | rw | PAE Pass Portmap 0 _B PAE Pass Portmap is 000000 _B 1 _B PAE Pass Portmap is 111111 _B |
| SPP | 1 | rw | Slow Pass Portmap 0 _B SLOW Pass Portmap is 000000 _B 1 _B SLOW Pass Portmap is 111111 _B |
| BPP | 0 | rw | BPDU Pass Portmap 0 _B BPDU Pass Portmap is 000000 _B 1 _B BPDU Pass Portmap is 111111 _B |

New Reserve Address Control Register 1

NRAC1 **Offset** **Reset Value**
New Reserve Address Control Register 1 **3E_H** **0000_H**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|---|---|
| MCA1 | MCA2 | NRMG | NRMS | MRMB | NRSG | NRSS | NRSB | NRCG | NRCS | NRCB | NRTG | NRTS | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | | |

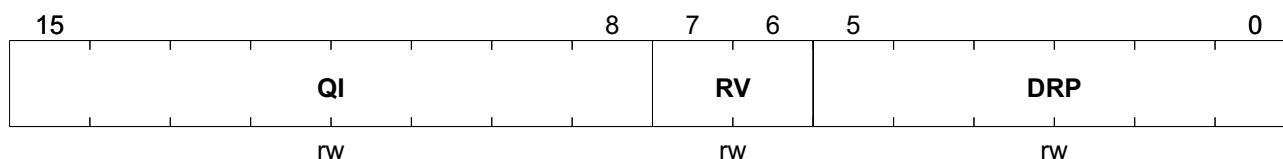
| Field | Bits | Type | Description |
|-------|-------|------|--|
| MCA1 | 15 | rw | Mac Control Action 1 Mac Control Action when OPCODE is 01 _H 0 _B The same as Mac Control Action when OPCODE is not 01 _H 1 _B Discard |
| MCA2 | 14:13 | rw | Mac Control Action 2 Mac Control Action when OPCODE is not 01 _H 00 _B Default Output Ports 01 _B Discard 10 _B If the receiving port is the CPU port, forward it to the default output ports. If the receiving port is not the CPU port, forward it to the CPU port 11 _B Forward to the default output ports except the CPU port |
| NRMG | 12 | rw | New Reserve Management for GXP 0 _B Do not identify as management packets 1 _B Identify as management packets |
| NRMS | 11 | rw | New Reserve Management for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 0 _B Do not identify as management packets 1 _B Identify as management packets |
| MRMB | 10 | rw | New Reserve Management for BPD 0 _B Do not identify as management packets 1 _B Identify as management packets |
| NRSG | 9 | rw | New Reserve Span for GXP 0 _B Do not identify as management packets 1 _B Identify as management packets |
| NRSS | 8 | rw | New Reserve Span for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 0 _B Do not identify as span packets 1 _B Identify as span packets |
| NRSB | 7 | rw | New Reserve SPAN for BPD 0 _B Do not identify as span packets 1 _B Identify as span packets |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| NRCG | 6 | rw | New Reserve Cross_VLAN for GXP 0 _B Follow VLAN 1 _B Cross VLAN |
| NRCS | 5 | rw | New Reserve Cross_VLAN. for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 0 _B Follow VLAN 1 _B Cross VLAN |
| NRCB | 4 | rw | New Reserve Cross_VLAN for BPD 0 _B Follow VLAN 1 _B Cross VLAN |
| NRTG | 3:2 | rw | New Reserve TXTAG for GXP 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| NRTS | 1:0 | rw | New Reserve TXTAG for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |

Hardware IGMP Control Register

| HIC | Offset | Reset Value |
|--------------------------------|-----------------|-------------------|
| Hardware IGMP Control Register | 3F _H | 7C80 _H |



| Field | Bits | Type | Description |
|-------|------|------|---|
| QI | 15:8 | rw | Query Interval The register is used to define Query_Interval when hardware based IGMP snooping function is enabled (000C _H , HISE). The automatically learned router port will be aged out if no IGMP Query frame received from the router port for (Query_Interval * Robust Variable) seconds. |

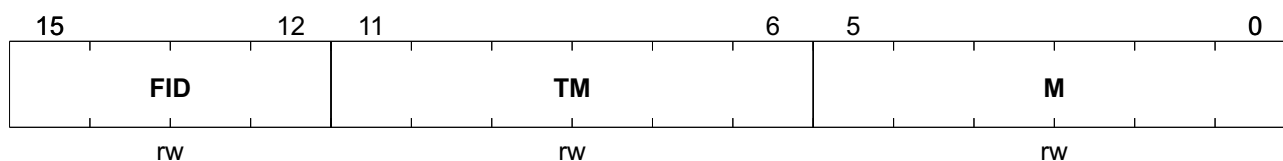
Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| RV | 7:6 | rw | Robust Variable The register is used to define Robust_Variable when hardware based IGMP snooping function is enabled (000C _H , HISE). 00 _B Reserved 01 _B 1 time 10 _B 2 times 11 _B 3 times |
| DRP | 5:0 | rw | Default Router Portmap The register is used to define Static Router Port when hardware based IGMP snooping function and default router port function are enabled (000C _H , HISE & HIDRE). |

4.2 EEPROM Extended Registers

VLAN Filter 0 Low

VF0L **Offset** **Reset Value**
VLAN Filter 0 Low **40_H** **003F_H**



| Field | Bits | Type | Description |
|-------|-------|------|---|
| FID | 15:12 | rw | FID The forwarding or learning group that the VID is assigned. |
| TM | 11:6 | rw | Tagged Member These bits indicate which ports associated with the VID should transmit tagged packets. Tagged Member[x] Description. 0 _B Port x should transmit untagged packets 1 _B Port x should transmit tagged packets |
| M | 5:0 | rw | Member These bits indicate which ports are the members of the VLAN. Member[x] Description. 0 _B Port x is not a VLAN member 1 _B Port x is a VLAN member |

Similar Registers

Table 58 VFxL Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|-----------------|-------------|
| VF1L | VLAN Filter 1 Low | 42 _H | |
| VF2L | VLAN Filter 2 Low | 44 _H | |
| VF3L | VLAN Filter 3Low | 46 _H | |
| VF4L | VLAN Filter 4 Low | 48 _H | |
| VF5L | VLAN Filter 5 Low | 4A _H | |
| VF6L | VLAN Filter 6 Low | 4C _H | |
| VF7L | VLAN Filter 7 Low | 4E _H | |
| VF8L | VLAN Filter 8 Low | 50 _H | |
| VF9L | VLAN Filter 9 Low | 52 _H | |
| VF10L | VLAN Filter 10 Low | 54 _H | |
| VF11L | VLAN Filter 11 Low | 56 _H | |
| VF12L | VLAN Filter 12 Low | 58 _H | |

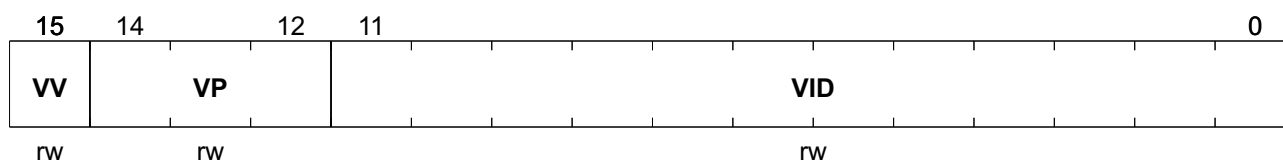
Registers Description

Table 58 VFxL Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|-----------------|-------------|
| VF13L | VLAN Filter 13 Low | 5A _H | |
| VF14L | VLAN Filter 14 Low | 5C _H | |
| VF15L | VLAN Filter 15 Low | 5E _H | |

VLAN Filter 0 High

| | | |
|---------------------------|-----------------------|-------------------------|
| VF0H | Offset | Reset Value |
| VLAN Filter 0 High | 41_H | 8001_H |



| Field | Bits | Type | Description |
|-------|-------|------|---|
| VV | 15 | rw | VLAN_Valid 0 _B VLAN filter is not valid 1 _B VLAN Filter is valid |
| VP | 14:12 | rw | VLAN PRI It indicates the VLAN priority associated with VID. |
| VID | 11:0 | rw | VID It indicates the VLAN ID that is associated with FID, Tagged Member, Member and VLAN PRI. |

Similar Registers

All VFxH registers have the same structure and characteristics, see [VF0H](#).
The offset addresses of the other VFxH registers are listed in [Table 59](#).

Table 59 VFxH Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------|-----------------|-------------|
| VF1H | VLAN Filter 1 High | 43 _H | |
| VF2H | VLAN Filter 2 High | 45 _H | |
| VF3H | VLAN Filter 3 High | 47 _H | |
| VF4H | VLAN Filter 4 High | 49 _H | |
| VF5H | VLAN Filter 5 High | 4B _H | |
| VF6H | VLAN Filter 6 High | 4D _H | |
| VF7H | VLAN Filter 7 High | 4F _H | |
| VF8H | VLAN Filter 8 High | 51 _H | |
| VF9H | VLAN Filter 9 High | 53 _H | |
| VF10H | VLAN Filter 10 High | 55 _H | |

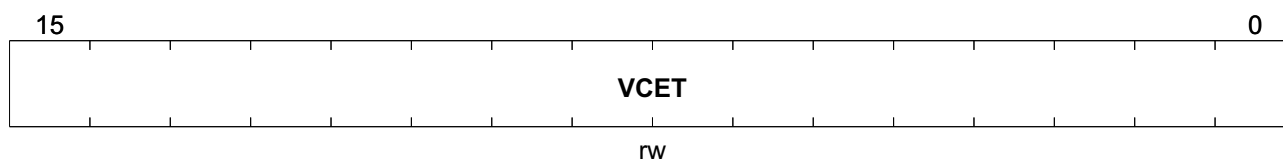
Registers Description

Table 59 VFXH Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------|-----------------|-------------|
| VF11H | VLAN Filter 11 High | 57 _H | |
| VF12H | VLAN Filter 12 High | 59 _H | |
| VF13H | VLAN Filter 13 High | 5B _H | |
| VF14H | VLAN Filter 14 High | 5D _H | |
| VF15H | VLAN Filter 15 High | 5F _H | |

Type Filter 0

| | | |
|---------------|-----------------|--------------------|
| TF0 | Offset | Reset Value |
| Type Filter 0 | 60 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|--------------------------------|
| VCET | 15:0 | rw | Value Compared with Ether-Type |

Similar Registers

All TFX registers have the same structure and characteristics, see [TF0](#).

The offset addresses of the other TFX registers are listed in [Table 60](#).

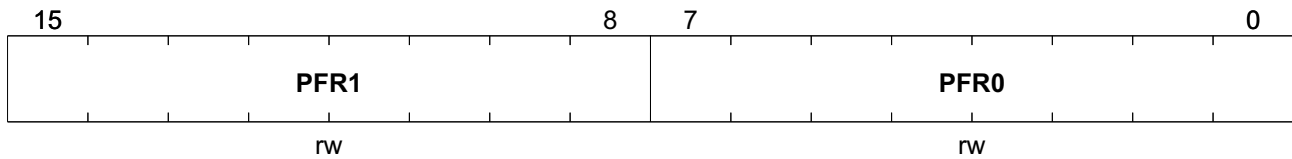
Table 60 TFX Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|-----------------|-------------|
| TF1 | Type Filter 1 | 61 _H | |
| TF2 | Type Filter 2 | 62 _H | |
| TF3 | Type Filter 3 | 63 _H | |
| TF4 | Type Filter 4 | 64 _H | |
| TF5 | Type Filter 5 | 65 _H | |
| TF6 | Type Filter 6 | 66 _H | |
| TF7 | Type Filter 7 | 67 _H | |

Protocol Filter 1 and 0

| | | |
|-------------------------|-----------------|--------------------|
| PF_1_0 | Offset | Reset Value |
| Protocol Filter 1 and 0 | 68 _H | 0000 _H |

Registers Description



| Field | Bits | Type | Description |
|-------|------|------|--|
| PFR1 | 15:8 | rw | Value Compared with Protocol in IP Header (Protocol Filter 1, 3, 5, 7) |
| PFR0 | 7:0 | rw | Value Compared with Protocol in IP Header (Protocol Filter 0, 2, 4, 6) |

Similar Registers

All PFx registers have the same structure and characteristics, see [PF_1_0](#).

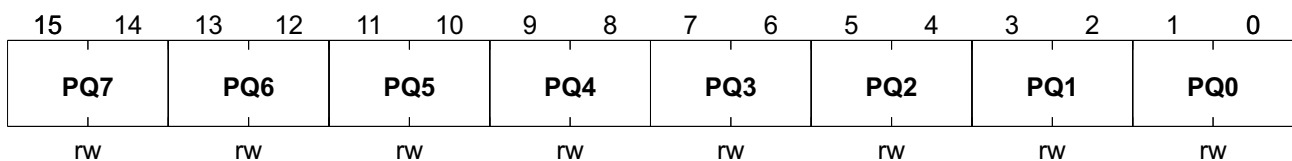
The offset addresses of the other PFX registers are listed in [Table 61](#).

Table 61 PFX Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|-------------------------|-----------------|-------------|
| PF_3_2 | Protocol Filter 3 and 2 | 68 _H | |
| PF_5_4 | Protocol Filter 5 and 4 | 69 _H | |
| PF_7_6 | Protocol Filter 7 and 6 | 6A _H | |

Service Priority Mapping 0

| SPM0 | Offset | Reset Value |
|----------------------------|-----------------|-------------------|
| Service Priority Mapping 0 | 6C _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|-------|------|---|
| PQ7 | 15:14 | rw | Priority Queue 7 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000111 _B . |
| PQ6 | 13:12 | rw | Priority Queue 6 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000110 _B . |
| PQ5 | 11:10 | rw | Priority Queue 5 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000101 _B . |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| PQ4 | 9:8 | rw | Priority Queue 4 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000100 _B . |
| PQ3 | 7:6 | rw | Priority Queue 3 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000011 _B . |
| PQ2 | 5:4 | rw | Priority Queue 2 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000010 _B . |
| PQ1 | 3:2 | rw | Priority Queue 1 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000001 _B . |
| PQ0 | 1:0 | rw | Priority Queue 0 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000000 _B . 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |

Service Priority Mapping 1

| | | |
|-----------------------------------|-----------------------|-------------------------|
| SPM1 | Offset | Reset Value |
| Service Priority Mapping 1 | 6D_H | 0000_H |

| | | | | | | | | | | | | | | | |
|------------|----|------------|----|------------|----|------------|---|------------|---|------------|---|------------|---|------------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PQF | | PQE | | PQD | | PQC | | PQB | | PQA | | PQ9 | | PQ8 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

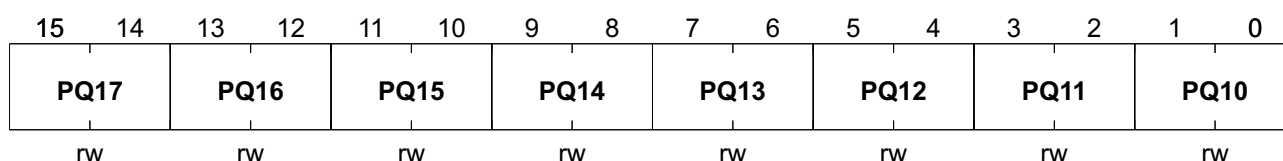
| Field | Bits | Type | Description |
|-------|-------|------|---|
| PQF | 15:14 | rw | Priority Queue F The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001111 _B . |
| PQE | 13:12 | rw | Priority Queue E The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001110 _B . |
| PQD | 11:10 | rw | Priority Queue D The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001101 _B . |
| PQC | 9:8 | rw | Priority Queue C The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001100 _B . |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| PQB | 7:6 | rw | Priority Queue B The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001011 _B |
| PQA | 5:4 | rw | Priority Queue A The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001010 _B |
| PQ9 | 3:2 | rw | Priority Queue 9 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001001 _B |
| PQ8 | 1:0 | rw | Priority Queue 8 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001000 _B |

Service Priority Mapping 2

SPM2 **Offset**
6E_H **Reset Value**
0000_H
Service Priority Mapping 2



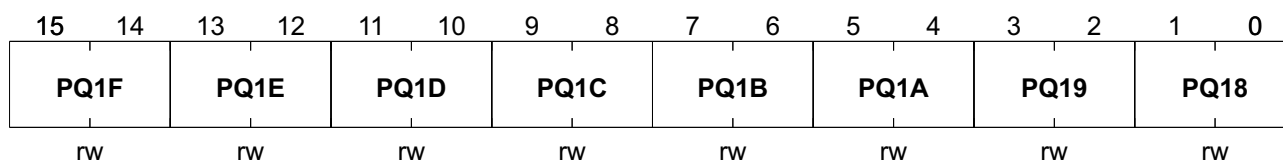
| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ17 | 15:14 | rw | Priority Queue 17 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010111 _B |
| PQ16 | 13:12 | rw | Priority Queue 16 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010110 _B |
| PQ15 | 11:10 | rw | Priority Queue 15 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010101 _B |
| PQ14 | 9:8 | rw | Priority Queue 14 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010100 _B |
| PQ13 | 7:6 | rw | Priority Queue 13 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010011 _B |
| PQ12 | 5:4 | rw | Priority Queue 12 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010010 _B |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| PQ11 | 3:2 | rw | Priority Queue 11 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010001 _B |
| PQ10 | 1:0 | rw | Priority Queue 10 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010000 _B |

Service Priority Mapping 3

| | | |
|-----------------------------------|-----------------------|-------------------------|
| SPM3 | Offset | Reset Value |
| Service Priority Mapping 3 | 6F_H | 0000_H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ1F | 15:14 | rw | Priority Queue 1F The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011111 _B |
| PQ1E | 13:12 | rw | Priority Queue 1E The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011110 _B |
| PQ1D | 11:10 | rw | Priority Queue 1D The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011101 _B |
| PQ1C | 9:8 | rw | Priority Queue 1C The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011100 _B |
| PQ1B | 7:6 | rw | Priority Queue 1B The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011011 _B |
| PQ1A | 5:4 | rw | Priority Queue 1A The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011010 _B |
| PQ19 | 3:2 | rw | Priority Queue 19 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011001 _B |
| PQ18 | 1:0 | rw | Priority Queue 18 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011000 _B |

Registers Description

Service Priority Mapping 4

SPM4 **Offset** **Reset Value**
Service Priority Mapping 4 **70_H** **0000_H**

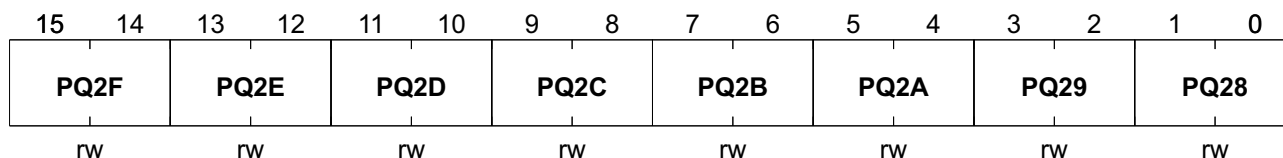
| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PQ27 | PQ26 | PQ25 | PQ24 | PQ23 | PQ22 | PQ21 | PQ20 | | | | | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | | | | | | | | |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ27 | 15:14 | rw | Priority Queue 27 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100111 _B |
| PQ26 | 13:12 | rw | Priority Queue 26 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100110 _B |
| PQ25 | 11:10 | rw | Priority Queue 25 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100101 _B |
| PQ24 | 9:8 | rw | Priority Queue 24 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100100 _B |
| PQ23 | 7:6 | rw | Priority Queue 23 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100011 _B |
| PQ22 | 5:4 | rw | Priority Queue 22 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100010 _B |
| PQ21 | 3:2 | rw | Priority Queue 21 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100001 _B |
| PQ20 | 1:0 | rw | Priority Queue 20 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100000 _B |

Service Priority Mapping 5

SPM5 **Offset** **Reset Value**
Service Priority Mapping 5 **71_H** **0000_H**

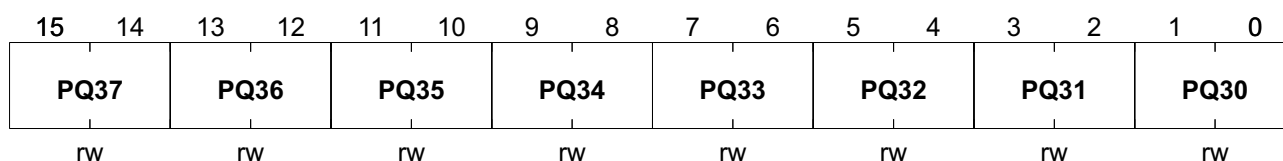
Registers Description



| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ2F | 15:14 | rw | Priority Queue 2F The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101111 _B |
| PQ2E | 13:12 | rw | Priority Queue 2E The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101110 _B |
| PQ2D | 11:10 | rw | Priority Queue 2D The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101101 _B |
| PQ2C | 9:8 | rw | Priority Queue 2C The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101100 _B |
| PQ2B | 7:6 | rw | Priority Queue 2B The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101011 _B |
| PQ2A | 5:4 | rw | Priority Queue 2A The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101010 _B |
| PQ29 | 3:2 | rw | Priority Queue 29 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101001 _B |
| PQ28 | 1:0 | rw | Priority Queue 28 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101000 _B |

Service Priority Mapping 6

| | | |
|-----------------------------------|-----------------------|-------------------------|
| SPM6 | Offset | Reset Value |
| Service Priority Mapping 6 | 72_H | 0000_H |

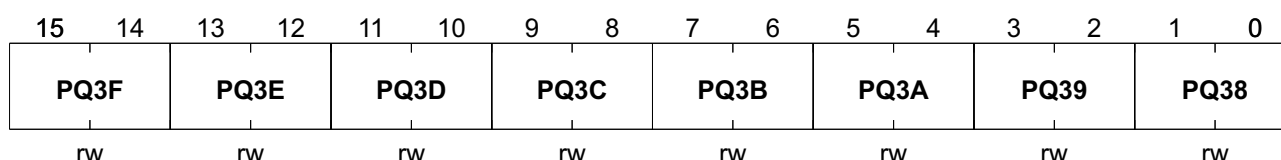


Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ37 | 15:14 | rw | Priority Queue 37 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110111 _B |
| PQ36 | 13:12 | rw | Priority Queue 36 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110110 _B |
| PQ35 | 11:10 | rw | Priority Queue 35 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110101 _B |
| PQ34 | 9:8 | rw | Priority Queue 34 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110100 _B |
| PQ33 | 7:6 | rw | Priority Queue 33 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110011 _B |
| PQ32 | 5:4 | rw | Priority Queue 32 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110010 _B |
| PQ31 | 3:2 | rw | Priority Queue 31 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110001 _B |
| PQ30 | 1:0 | rw | Priority Queue 30 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110000 _B |

Service Priority Mapping 7

| | | |
|-----------------------------------|-----------------------|-------------------------|
| SPM7 | Offset | Reset Value |
| Service Priority Mapping 7 | 73_H | 0000_H |



| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ3F | 15:14 | rw | Priority Queue 3F The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111111 _B |
| PQ3E | 13:12 | rw | Priority Queue 3E The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111110 _B |

Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| PQ3D | 11:10 | rw | Priority Queue 3D The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111101 _B |
| PQ3C | 9:8 | rw | Priority Queue 3C The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111100 _B |
| PQ3B | 7:6 | rw | Priority Queue 3B The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111011 _B |
| PQ3A | 5:4 | rw | Priority Queue 3A The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111010 _B |
| PQ39 | 3:2 | rw | Priority Queue 39 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111001 _B |
| PQ38 | 1:0 | rw | Priority Queue 38 The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111000 _B |

Reserve Action for 0180C2000001~0180C2000000

| RA_01_00 | Offset | Reset Value |
|---|-----------------|-------------------|
| Reserve Action for 0180C2000001~0180C2000000 | 74 _H | 0000 _H |

| | | | | | | | | | | | | | | | |
|--------------|--------------|-------------|-------------|--------------------|------------------|--------------|--------------|-------------|-------------|--------------------|------------------|----|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RA01 _VA* | RA01 _SP* | RA01 _MG | RA01 _CV | RA01 _TX TAG | RA01 _AC T | RA00 _VA* | RA00 _SP* | RA00 _MG | RA00 _CV | RA00 _TX TAG | RA00 _AC T | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | | |

| Field | Bits | Type | Description |
|------------|------|------|--|
| RA01_VALID | 15 | rw | Valid bit for 0180C2000001 0 _B Not Valid 1 _B Valid |
| RA01_SPAN | 14 | rw | Span bit for 0180C2000001 0 _B Doesn't identify as the span packet 1 _B Identify as the span packet |
| RA01_MG | 13 | rw | Management bit for 0180C2000001 0 _B Doesn't identify as the management packet 1 _B Identify as the management packet |
| RA01_CV | 12 | rw | Cross_VLAN bit for 0180C2000001 0 _B Doesn't identify as the cross_VLAN packet 1 _B Identify as the cross_VLAN packet |

Registers Description

| Field | Bits | Type | Description |
|------------|-------|------|--|
| RA01_TXTAG | 11:10 | rw | TXTAG bit for 0180C2000001 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| RA01_ACT | 9:8 | rw | Action bit for 0180C2000001 00 _B Portmap is 111111 _B 01 _B Portmap is 000000 _B 10 _B Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port 11 _B Portmap contains all the ports, excluding the CPU port |
| RA00_VALID | 7 | rw | Valid bit for 0180C2000000 0 _B Not Valid 1 _B Valid |
| RA00_SPAN | 6 | rw | Span bit for 0180C2000000 0 _B Doesn't identify as the span packet 1 _B Identify as the span packet |
| RA00_MG | 5 | rw | Management bit for 0180C2000000 0 _B Doesn't identify as the management packet 1 _B Identify as the management packet |
| RA00_CV | 4 | rw | Cross_VLAN bit for 0180C2000000 0 _B Doesn't identify as the cross_VLAN packet 1 _B Identify as the cross_VLAN packet |
| RA00_TXTAG | 3:2 | rw | TXTAG bit for 0180C2000000 00 _B System Default Tag 01 _B Unmodified 10 _B Always Tagged 11 _B Always Untagged |
| RA00_ACT | 1:0 | rw | Action bit for 0180C2000000 00 _B Portmap is 111111 _B 01 _B Portmap is 000000 _B 10 _B Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port 11 _B Portmap contains all the ports, excluding the CPU port |

Similar Registers

All RAx registers have the same structure and characteristics, see [RA_01_00](#).
The offset addresses of the other RAx registers are listed in [Table 62](#).

Table 62 RAx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-----------------|-------------|
| RA_03_02 | Reserve Action for 0180C2000003~0180C2000002 | 75 _H | |
| RA_05_04 | Reserve Action for 0180C2000005~0180C2000004 | 76 _H | |

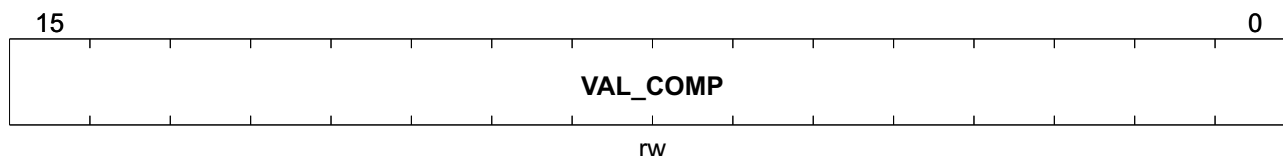
Registers Description
Table 62 RAx Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|-----------------|-------------|
| RA_07_06 | Reserve Action for 0180C2000007~0180C2000006 | 77 _H | |
| RA_09_08 | Reserve Action for 0180C2000009~0180C2000008 | 78 _H | |
| RA_0B_0A | Reserve Action for 0180C200000B~0180C200000A | 79 _H | |
| RA_0D_0C | Reserve Action for 0180C200000D~0180C200000C | 7A _H | |
| RA_0F_0E | Reserve Action for 0180C200000F~0180C200000E | 7B _H | |
| RA_11_10 | Reserve Action for 0180C2000011~0180C2000010 | 7C _H | |
| RA_13_12 | Reserve Action for 0180C2000013~0180C2000012 | 7D _H | |
| RA_15_14 | Reserve Action for 0180C2000015~0180C2000014 | 7E _H | |
| RA_17_16 | Reserve Action for 0180C2000017~0180C2000016 | 7F _H | |
| RA_19_18 | Reserve Action for 0180C2000019~0180C2000018 | 80 _H | |
| RA_1B_1A | Reserve Action for 0180C200001B~0180C200001A | 81 _H | |
| RA_1D_1C | Reserve Action for 0180C200001D~0180C200001C | 82 _H | |
| RA_1F_1E | Reserve Action for 0180C200001F~0180C200001E | 83 _H | |
| RA_21_20 | Reserve Action for 0180C2000021~0180C2000020 | 84 _H | |
| RA_23_22 | Reserve Action for 0180C2000023~0180C2000022 | 85 _H | |
| RA_25_24 | Reserve Action for 0180C2000025~0180C2000024 | 86 _H | |
| RA_27_26 | Reserve Action for 0180C2000027~0180C2000026 | 87 _H | |
| RA_29_28 | Reserve Action for 0180C2000029~0180C2000028 | 88 _H | |
| RA_2B_2A | Reserve Action for 0180C200002B~0180C200002A | 89 _H | |
| RA_2D_2C | Reserve Action for 0180C200002D~0180C200002C | 8A _H | |
| RA_2F_2E | Reserve Action for 0180C200002F~0180C200002E | 8B _H | |

Registers Description

TCP/UDP Filter 0

TUF0 Offset **8C_H** Reset Value **0000_H**
TCP/UDP Filter 0



| Field | Bits | Type | Description |
|----------|------|------|---|
| VAL_COMP | 15:0 | rw | Value Compared with the Destination Port Number in the TCP/UDP Header |

Similar Registers

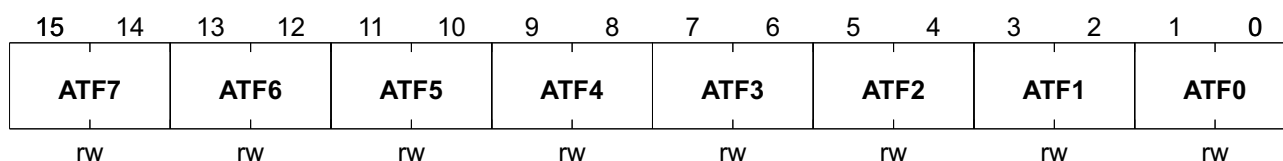
All TUFx registers have the same structure and characteristics, see [TUF0](#).
The offset addresses of the other TUFx registers are listed in [Table 65](#).

Table 63 TUFx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|-----------------|-------------|
| TUF1 | TCP/UDP Filter 1 | 8D _H | |
| TUF2 | TCP/UDP Filter 2 | 8E _H | |
| TUF3 | TCP/UDP Filter 3 | 8F _H | |
| TUF4 | TCP/UDP Filter 4 | 90 _H | |
| TUF5 | TCP/UDP Filter 5 | 91 _H | |
| TUF6 | TCP/UDP Filter 6 | 92 _H | |
| TUF7 | TCP/UDP Filter 7 | 93 _H | |

Type Filter Action

TFA Offset **94_H** Reset Value **0000_H**
Type Filter Action



Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| ATF7 | 15:14 | rw | Action for Type Filter 7 See register 0094 _H , ATF0 for more detail. |
| ATF6 | 13:12 | rw | Action for Type Filter 6 See register 0094 _H , ATF0 for more detail. |
| ATF5 | 11:10 | rw | Action for Type Filter 5 See register 0094 _H , ATF0 for more detail. |
| ATF4 | 9:8 | rw | Action for Type Filter 4 See register 0094 _H , ATF0 for more detail. |
| ATF3 | 7:6 | rw | Action for Type Filter 3 See register 0094 _H , ATF0 for more detail. |
| ATF2 | 5:4 | rw | Action for Type Filter 2 See register 0094 _H , ATF0 for more detail. |
| ATF1 | 3:2 | rw | Action for Type Filter 1 See register 0094 _H , ATF0 for more detail. |
| ATF0 | 1:0 | rw | Action for Type Filter 0 00 _B Type Portmap is Default Output Ports 01 _B Type Portmap is 000000 _B 10 _B Type Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports , excluding the CPU port 11 _B Type Portmap contains Default Output Ports , excluding the CPU port |

Protocol Filter Action

| PFA | Offset | Reset Value |
|------------------------|-----------------|-------------------|
| Protocol Filter Action | 95 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|-------|------|---|
| APF7 | 15:14 | rw | Action for Protocol Filter 7 See register 0095 _H , APF0 for more detail. |
| APF6 | 13:12 | rw | Action for Protocol Filter 6 See register 0095 _H , APF0 for more detail. |
| APF5 | 11:10 | rw | Action for Protocol Filter 5 See register 0095 _H , APF0 for more detail. |
| APF4 | 9:8 | rw | Action for Protocol Filter 4 See register 0095 _H , APF0 for more detail. |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| APF3 | 7:6 | rw | Action for Protocol Filter 3 See register 0095 _H , APF0 for more detail. |
| APF2 | 5:4 | rw | Action for Protocol Filter 2 See register 0095 _H , APF0 for more detail. |
| APF1 | 3:2 | rw | Action for Protocol Filter 1 See register 0095 _H , APF0 for more detail. |
| APF0 | 1:0 | rw | Action for Protocol Filter 0 00 _B Protocol Portmap is Default Output Ports 01 _B Protocol Portmap is 000000 _B 10 _B Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports , excluding the CPU port 11 _B Protocol Portmap contains Default Output Ports , excluding the CPU port |

TCP/UDP Action 0

| | | |
|-------------------------|-----------------------|-------------------------|
| TUA0 | Offset | Reset Value |
| TCP/UDP Action 0 | 96_H | 0000_H |

| | | | | | | | | | | | | | | | |
|-------|----|-------|----|-------|----|-------|---|-------|---|-------|---|-------|---|-------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ATUF3 | | TUPF3 | | ATUF2 | | TUPF2 | | ATUF1 | | TUPF1 | | ATUF0 | | TUPF0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| ATUF3 | 15:14 | rw | Action for TCP/UDP Filter 3. See register 0096 _H , ATUF0 for more detail. |
| TUPF3 | 13:12 | rw | TCP/UDP PRI for TCP/UDP Filter 3 See register 0096 _H , TUPF0 for more detail. |
| ATUF2 | 11:10 | rw | Action for TCP/UDP Filter 2 See register 0096 _H , ATUF0 for more detail. |
| TUPF2 | 9:8 | rw | TCP/UDP PRI for TCP/UDP Filter 2 See register 0096 _H , TUPF0 for more detail. |
| ATUF1 | 7:6 | rw | Action for TCP/UDP Filter 1 See register 0096 _H , ATUF0 for more detail. |
| TUPF1 | 5:4 | rw | TCP/UDP PRI for TCP/UDP Filter 1 See register 0096 _H , TUPF0 for more detail. |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| ATUF0 | 3:2 | rw | Action for TCP/UDP Filter 0 00 _B Protocol Portmap is Default Output Ports 01 _B Protocol Portmap is 000000 _B 10 _B Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports , excluding the CPU port 11 _B Protocol Portmap contains Default Output Ports , excluding the CPU port |
| TUPF0 | 1:0 | rw | TCP/UDP PRI for TCP/UDP Filter 0 00 _B Queue 0 01 _B Queue 1 10 _B Queue 2 11 _B Queue 3 |

TCP/UDP Action 1

| | | |
|------------------|-----------------|-------------------|
| TUA1 | Offset | Reset Value |
| TCP/UDP Action 1 | 97 _H | 0000 _H |

| | | | | | | | | | | | | | | | |
|-------|----|-------|----|-------|----|-------|---|-------|---|-------|---|-------|---|-------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ATUF7 | | TUPF7 | | ATUF6 | | TUPF6 | | ATUF5 | | TUPF5 | | ATUF4 | | TUPF4 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| ATUF7 | 15:14 | rw | Action for TCP/UDP Filter 7 See register 0096 _H , ATUF0 for more detail. |
| TUPF7 | 13:12 | rw | TCP/UDP PRI for TCP/UDP Filter 7 See register 0096 _H , TUPF0 for more detail. |
| ATUF6 | 11:10 | rw | Action for TCP/UDP Filter 6 See register 0096 _H , ATUF0 for more detail. |
| TUPF6 | 9:8 | rw | TCP/UDP PRI for TCP/UDP Filter 6 See register 0096 _H , TUPF0 for more detail. |
| ATUF5 | 7:6 | rw | Action for TCP/UDP Filter 5 See register 0096 _H , ATUF0 for more detail. |
| TUPF5 | 5:4 | rw | TCP/UDP PRI for TCP/UDP Filter 5 See register 0096 _H , TUPF0 for more detail. |
| ATUF4 | 3:2 | rw | Action for TCP/UDP Filter 4 See register 0096 _H , ATUF0 for more detail. |
| TUPF4 | 1:0 | rw | TCP/UDP PRI for TCP/UDP Filter 4 See register 0096 _H , TUPF0 for more detail. |

Registers Description

TCP/UDP Action 2

TUA2 **Offset** **Reset Value**
TCP/UDP Action 2 **98_H** **0000_H**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|------|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Res | | COMP | | P5I | P4I | P3I | P2I | P1I | P0I | P5T | P4T | P3T | P2T | P1T | P0T |
| r | | rw | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

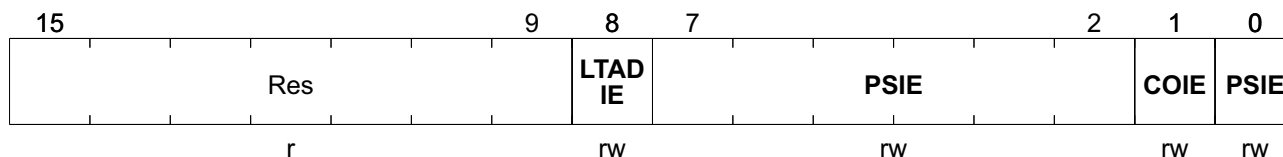
| Field | Bits | Type | Description |
|-------|-------|------|--|
| Res | 15:14 | r | Reserved |
| COMP | 13:12 | rw | Compare TCP/UDP Source Port or Destination Port 00 _B Do not Compare 01 _B Compare Destination Port 10 _B Compare Source Port 11 _B Compare Destination Port or Source Port |
| P5I | 11 | rw | Port 5 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P4I | 10 | rw | Port 4 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P3I | 9 | rw | Port 3 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P2I | 8 | rw | Port 2 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P1I | 7 | rw | Port 1 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P0I | 6 | rw | Port 0 IP over TCP/UDP 0 _B Use TCP/UDP field when packets contain both TCP/UDP and IP 1 _B Use IP field when packets contain both TCP/UDP and IP |
| P5T | 5 | rw | Port 5 TCP/UDP PRIEN 0 _B Do not use TCP/UDP priority 1 _B Use TCP/UDP priority |
| P4T | 4 | rw | Port 4 TCP/UDP PRIEN 0 _B Do not use TCP/UDP priority 1 _B Use TCP/UDP priority |
| P3T | 3 | rw | Port 3 TCP/UDP PRIEN 0 _B Do not use TCP/UDP priority 1 _B Use TCP/UDP priority |

Registers Description

| Field | Bits | Type | Description |
|----------|------|------|---|
| INS_PROT | 3 | rw | Insert Special Tag if Protocol field matches with pre-defined rules. 0 _B Doesn't insert 1 _B Insert |
| INS_TU | 2 | rw | Insert Special Tag if Port field matches with pre-defined rules. 0 _B Doesn't insert 1 _B Insert |
| INS_MC | 1 | rw | Insert Special Tag in MAC Control Packet. 0 _B Doesn't insert 1 _B Insert |
| INS_DEF | 0 | rw | Insert Special Tag in the packets except those packets defined in bit 8 ~ 1. 0 _B Doesn't insert 1 _B Insert |

Interrupt Enable Register

| IE | Offset | Reset Value |
|---------------------------|-----------------|-------------------|
| Interrupt Enable Register | 9A _H | 0000 _H |



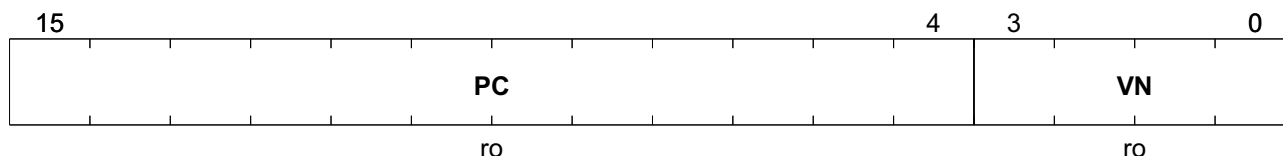
| Field | Bits | Type | Description |
|--------|------|------|---|
| Res | 15:9 | r | Reserved |
| LTADIE | 8 | rw | Leaning Table Access Done Interrupt Enable 0 _B Interrupt disable 1 _B Interrupt enable |
| PSIE | 7:2 | rw | Port Security Interrupt Enable It's a per port setting 0 _B Interrupt disable 1 _B Interrupt enable |
| COIE | 1 | rw | Counter Overflow Interrupt Enable 0 _B Interrupt disable 1 _B Interrupt enable |
| PSIE | 0 | rw | Port Status Interrupt Enable 0 _B Interrupt disable 1 _B Interrupt enable |

Interrupt Status Register

Registers Description

Chip Identifier 0

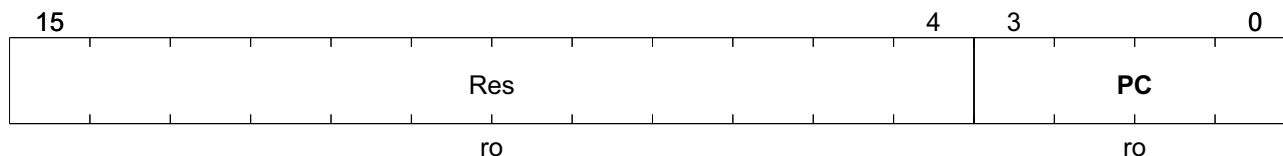
CI0 **Offset** **Reset Value**
Chip Identifier 0 **A0_H** **1023_H**



| Field | Bits | Type | Description |
|-------|------|------|--------------------|
| PC | 15:4 | ro | Product Code[11:0] |
| VN | 3:0 | ro | Version Number |

Chip Identifier 1

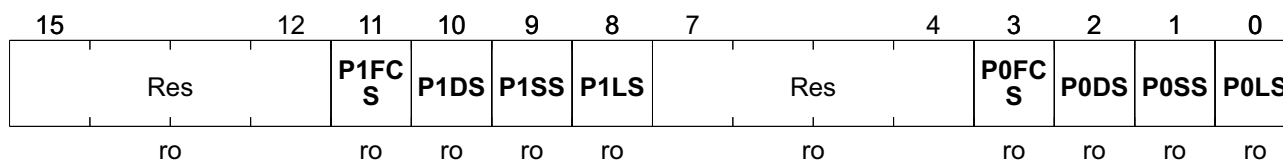
CI1 **Offset** **Reset Value**
Chip Identifier 1 **A1_H** **0007_H**



| Field | Bits | Type | Description |
|-------|------|------|-----------------------|
| Res | 15:4 | ro | Reserved |
| PC | 3:0 | ro | Product Code[15:12] |

Port Status 0

PS0 **Offset** **Reset Value**
Port Status 0 **A2_H** **0000_H**



Registers Description

| Field | Bits | Type | Description |
|-------|-------|------|--|
| Res | 15:12 | ro | Reserved |
| P1FCS | 11 | ro | Port 1 Flow Control Status 0 _B Port 1 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 1 enabled the Full Flow Control/Half Back Pressure Function |
| P1DS | 10 | ro | Port 1 Duplex Status 0 _B Port 1 operates in the Half Duplex 1 _B Port 1 operates in the Full Duplex |
| P1SS | 9 | ro | Port 1 Speed Status 0 _B Port 1 operates in the 10M 1 _B Port 1 operates in the 100M |
| P1LS | 8 | ro | Port 1 Link Status 0 _B Port 1 links down 1 _B Port 1 links up |
| Res | 7:4 | ro | Reserved |
| P0FCS | 3 | ro | Port 0 Flow Control Status 0 _B Port 0 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 0 enabled the Full Flow Control/Half Back Pressure Function |
| P0DS | 2 | ro | Port 0 Duplex Status 0 _B Port 0 operates in the Half Duplex 1 _B Port 0 operates in the Full Duplex |
| P0SS | 1 | ro | Port 0 Speed Status 0 _B Port 0 operates in the 10M 1 _B Port 0 operates in the 100M |
| P0LS | 0 | ro | Port 0 Link Status 0 _B Port 0 links down 1 _B Port 0 links up |

Port Status 1

| | | |
|----------------------|-----------------------|-------------------------|
| PS1 | Offset | Reset Value |
| Port Status 1 | A3_H | 0000_H |

| | | | | | | | | | | | | | | |
|--------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|---|-----|---|--------------|-------------|-------------|-------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | | 4 | 3 | 2 | 1 | 0 |
| P4FCS | P4DS | P4SS | P4LS | P3FCS | P3DS | P3SS | P3LS | | Res | | P2FCS | P2DS | P2SS | P2LS |
| ro | ro | ro | ro | ro | ro | ro | ro | | ro | | ro | ro | ro | ro |

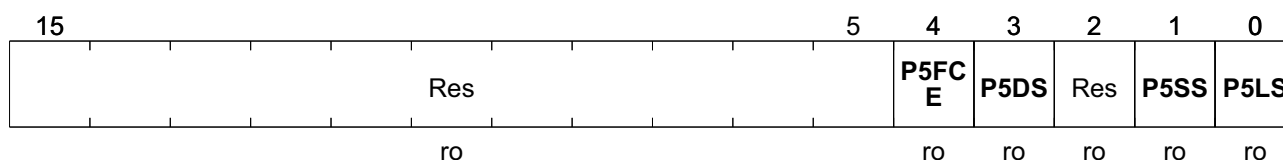
| Field | Bits | Type | Description |
|-------|------|------|--|
| P4FCS | 15 | ro | Port 4 Flow Control Status 0 _B Port 4 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 4 enabled the Full Flow Control/Half Back Pressure Function |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| P4DS | 14 | ro | Port 4 Duplex Status 0 _B Port 4 operates in the Half Duplex 1 _B Port 4 operates in the Full Duplex |
| P4SS | 13 | ro | Port 4 Speed Status 0 _B Port 4 operates in the 10M 1 _B Port 4 operates in the 100M |
| P4LS | 12 | ro | Port 4 Link Status 0 _B Port 4 links down 1 _B Port 4 links up |
| P3FCS | 11 | ro | Port 3 Flow Control Status 0 _B Port 3 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 3 enabled the Full Flow Control/Half Back Pressure Function |
| P3DS | 10 | ro | Port 3 Duplex Status 0 _B Port 3 operates in the Half Duplex 1 _B Port 3 operates in the Full Duplex |
| P3SS | 9 | ro | Port 3 Speed Status 0 _B Port 3 operates in the 10M 1 _B Port 3 operates in the 100M |
| P3LS | 8 | ro | Port 3 Link Status 0 _B Port 3 links down 1 _B Port 3 links up. |
| Res | 7:4 | ro | Reserved |
| P2FCS | 3 | ro | Port 2 Flow Control Status 0 _B Port 2 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 2 enabled the Full Flow Control/Half Back Pressure Function |
| P2DS | 2 | ro | Port 2 Duplex Status 0 _B Port 2 operates in the Half Duplex 1 _B Port 2 operates in the Full Duplex |
| P2SS | 1 | ro | Port 2 Speed Status 0 _B Port 2 operates in the 10M 1 _B Port 2 operates in the 100M |
| P2LS | 0 | ro | Port 2 Link Status 0 _B Port 2 links down 1 _B Port 2 links up |

Port Status 2

PS2 **Offset** **Reset Value**
Port Status 2 **A4_H** **0000_H**

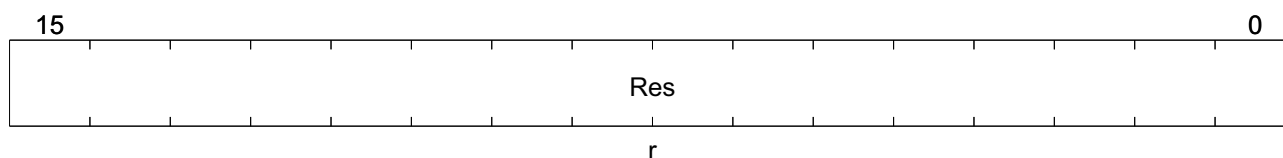


Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:5 | ro | Reserved |
| P5FCE | 4 | ro | Port 5 Flow Control Enable 0 _B Port 5 disables the Full Flow Control/Half Back Pressure Function 1 _B Port 5 enabled the Full Flow Control/Half Back Pressure Function |
| P5DS | 3 | ro | Port 5 Duplex Status 0 _B Port 5 operates in the Half Duplex 1 _B Port 5 operates in the Full Duplex |
| Res | 2 | ro | Reserved |
| P5SS | 1 | ro | Port 5 Speed Status 0 _B Port 5 operates in the 10M 1 _B Port 5 operates in the 100M |
| P5LS | 0 | ro | Port 5 Link Status 0 _B Port 5 links down 1 _B Port 5 links up |

Port Status 3

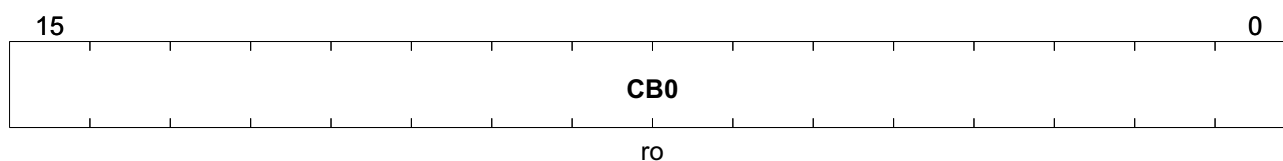
PS3 **Offset** **Reset Value**
Port Status 3 **A5_H** **0000_H**



| Field | Bits | Type | Description |
|-------|------|------|-----------------|
| Res | 15:0 | r | Reserved |

Cable Broken 0

CB0 **Offset** **Reset Value**
Cable Broken 0 **A6_H** **0000_H**



Registers Description

| Field | Bits | Type | Description |
|--------------|-------------|-------------|--------------------|
| CB0 | 15:0 | ro | Reserved |

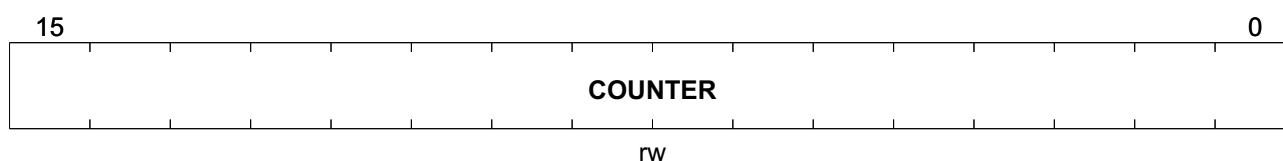
Registers Description

Table 64 CLx Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------------------------|------------------|-------------|
| CL8 | Port 2 Receive Packet Byte Count Low | C2 _H | |
| CL9 | Port 3 Receive Packet Byte Count Low | C6 _H | |
| CL10 | Port 4 Receive Packet Byte Count Low | C8 _H | |
| CL11 | Port 5 Receive Packet Byte Count Low | CA _H | |
| CL12 | Port 0 Transmit Packet Count Low | CC _H | |
| CL13 | Port 1 Transmit Packet Count Low | D0 _H | |
| CL14 | Port 2 Transmit Packet Count Low | D4 _H | |
| CL15 | Port 3 Transmit Packet Count Low | D8 _H | |
| CL16 | Port 4 Transmit Packet Count Low | DA _H | |
| CL17 | Port 5 Transmit Packet Count Low | DC _H | |
| CL18 | Port 0 Transmit Packet Byte Count Low | DE _H | |
| CL19 | Port 1 Transmit Packet Byte Count Low | E2 _H | |
| CL20 | Port 2 Transmit Packet Byte Count Low | E6 _H | |
| CL21 | Port 3 Transmit Packet Byte Count Low | EA _H | |
| CL22 | Port 4 Transmit Packet Byte Count Low | EC _H | |
| CL23 | Port 5 Transmit Packet Byte Count Low | EE _H | |
| CL24 | Port 0 Collision Count Low | F0 _H | |
| CL25 | Port 1 Collision Count Low | F4 _H | |
| CL26 | Port 2 Collision Count Low | F8 _H | |
| CL27 | Port 3 Collision Count Low | FC _H | |
| CL28 | Port 4 Collision Count Low | FE _H | |
| CL29 | Port 5 Collision Count Low | 100 _H | |
| CL30 | Port 0 Error Count Low | 102 _H | |
| CL31 | Port 1 Error Count Low | 106 _H | |
| CL32 | Port 2 Error Count Low | 10A _H | |
| CL33 | Port 3 Error Count Low | 10E _H | |
| CL34 | Port 4 Error Count Low | 110 _H | |
| CL35 | Port 5 Error Count Low | 112 _H | |

Counter High 0

| | | |
|---|-----------------------|-------------------------|
| CH0 | Offset | Reset Value |
| Port 0 Receive Packet Counter High | A9_H | 0000_H |



Registers Description

| Field | Bits | Type | Description |
|---------|------|------|----------------|
| COUNTER | 15:0 | rw | Counter[31:16] |

Similar Registers

All CHx registers have the same structure and characteristics, see [CH0](#).
The offset addresses of the other CLH registers are listed in [Table 65](#).

Table 65 CHx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|------------------|-------------|
| CH1 | Port 1 Receive Packet Counter High | AD _H | |
| CH2 | Port 2 Receive Packet Counter High | B1 _H | |
| CH3 | Port 3 Receive Packet Counter High | B5 _H | |
| CH4 | Port 4 Receive Packet Counter High | B7 _H | |
| CH5 | Port 5 Receive Packet Counter High | B9 _H | |
| CH6 | Port 0 Receive Packet Byte Count High | BB _H | |
| CH7 | Port 1 Receive Packet Byte Count High | BF _H | |
| CH8 | Port 2 Receive Packet Byte Count High | C3 _H | |
| CH9 | Port 3 Receive Packet Byte Count High | C7 _H | |
| CH10 | Port 4 Receive Packet Byte Count High | C9 _H | |
| CH11 | Port 5 Receive Packet Byte Count High | CB _H | |
| CH12 | Port 0 Transmit Packet Count High | CD _H | |
| CH13 | Port 1 Transmit Packet Count High | D1 _H | |
| CH14 | Port 2 Transmit Packet Count High | D5 _H | |
| CH15 | Port 3 Transmit Packet Count High | D9 _H | |
| CH16 | Port 4 Transmit Packet Count High | DB _H | |
| CH17 | Port 5 Transmit Packet Count High | DD _H | |
| CH18 | Port 0 Transmit Packet Byte Count High | DF _H | |
| CH19 | Port 1 Transmit Packet Byte Count High | E3 _H | |
| CH20 | Port 2 Transmit Packet Byte Count High | E7 _H | |
| CH21 | Port 3 Transmit Packet Byte Count High | EB _H | |
| CH22 | Port 4 Transmit Packet Byte Count High | ED _H | |
| CH23 | Port 5 Transmit Packet Byte Count High | EF _H | |
| CH24 | Port 0 Collision Count High | F1 _H | |
| CH25 | Port 1 Collision Count High | F5 _H | |
| CH26 | Port 2 Collision Count High | F9 _H | |
| CH27 | Port 3 Collision Count High | FD _H | |
| CH28 | Port 4 Collision Count High | FF _H | |
| CH29 | Port 5 Collision Count High | 101 _H | |
| CH30 | Port 0 Error Count High | 103 _H | |
| CH31 | Port 1 Error Count High | 107 _H | |
| CH32 | Port 2 Error Count High | 10B _H | |
| CH33 | Port 3 Error Count High | 10F _H | |

Registers Description

Table 65 CHx Registers (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|-------------------------|------------------|-------------|
| CH34 | Port 4 Error Count High | 111 _H | |
| CH35 | Port 5 Error Count High | 113 _H | |

Over-Flow Flag 0

| | | |
|-------------------------|------------------------|-------------------------|
| OFF0 | Offset | Reset Value |
| Over-Flow Flag 0 | 114_H | 0000_H |

| | | | | | | | | | | | | | | | |
|-------------------------|-----|-------------------------|-----|-------------------------|-----|-------------------------|-------------|-------------|-------------|-----|-------------|-----|-------------|-----|-------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P3_B C | Res | P2_B C | Res | P1_B C | Res | P0_B C | P5_C | P4_C | P3_C | Res | P2_C | Res | P1_C | Res | P0_C |
| lhsc | ro | lhsc | ro | lhsc | ro | lhsc | lhsc | lhsc | lhsc | ro | lhsc | ro | lhsc | ro | lhsc |

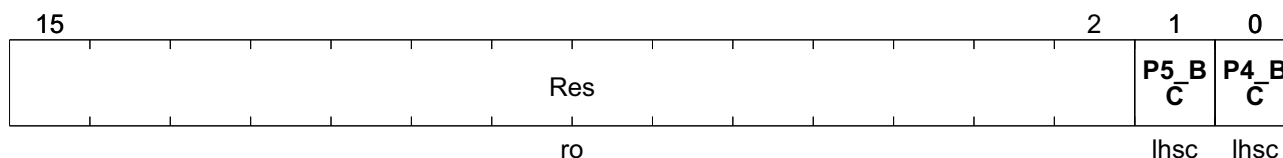
| Field | Bits | Type | Description |
|-------|------|------|--|
| P3_BC | 15 | lhsc | Overflow of Port 3 Receive Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 14 | ro | Reserved |
| P2_BC | 13 | lhsc | Overflow of Port 2 Receive Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 12 | ro | Reserved |
| P1_BC | 11 | lhsc | Overflow of Port 1 Receive Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 10 | ro | Reserved |
| P0_BC | 9 | lhsc | Overflow of Port 0 Receive Packet Byte Count 0 _B No overflow 1 _B Overflow |
| P5_C | 8 | lhsc | Overflow of Port 5 Receive Packet Count 0 _B No overflow 1 _B Overflow |
| P4_C | 7 | lhsc | Overflow of Port 4 Receive Packet Count 0 _B No overflow 1 _B Overflow |
| P3_C | 6 | lhsc | Overflow of Port 3 Receive Packet Count 0 _B No overflow 1 _B Overflow |
| Res | 5 | ro | Reserved |
| P2_C | 4 | lhsc | Overflow of Port 2 Receive Packet Count 0 _B No overflow 1 _B Overflow |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| P3_BC | 15 | lhsc | Overflow of Port 3 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 14 | ro | Reserved |
| P2_BC | 13 | lhsc | Overflow of Port 2 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 12 | ro | Reserved |
| P1_BC | 11 | lhsc | Overflow of Port 1 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |
| Res | 10 | ro | Reserved |
| P0_BC | 9 | lhsc | Overflow of Port 0 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |
| P5_C | 8 | lhsc | Overflow of Port 5 Transmit Packet Count 0 _B No overflow 1 _B Overflow |
| P4_C | 7 | lhsc | Overflow of Port 4 Transmit Packet Count 0 _B No overflow 1 _B Overflow |
| P3_C | 6 | lhsc | Overflow of Port 3 Transmit Packet Count 0 _B No overflow 1 _B Overflow |
| Res | 5 | ro | Reserved |
| P2_C | 4 | lhsc | Overflow of Port 2 Transmit Packet Count 0 _B No overflow 1 _B Overflow |
| Res | 3 | ro | Reserved |
| P1_C | 2 | lhsc | Overflow of Port 1 Transmit Packet Count 0 _B No overflow 1 _B Overflow |
| Res | 1 | ro | Reserved |
| P0_C | 0 | lhsc | Overflow of Port 0 Transmit Packet Count 0 _B No overflow 1 _B Overflow |

Over-Flow Flag 3

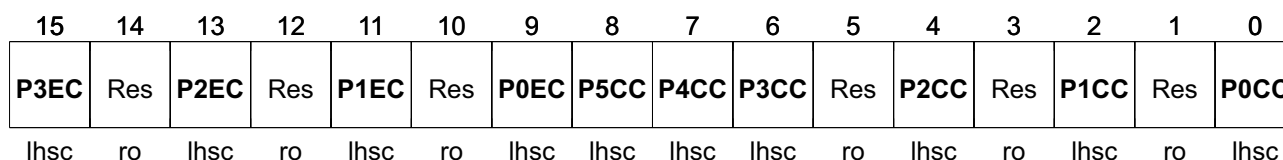
| | | |
|-------------------------|------------------------|-------------------------|
| OFF3 | Offset | Reset Value |
| Over-Flow Flag 3 | 117_H | 0000_H |



| Field | Bits | Type | Description |
|-------|------|------|---|
| Res | 15:2 | ro | Reserved |
| P5_BC | 1 | lhsc | Overflow of Port 5 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |
| P4_BC | 0 | lhsc | Overflow of Port 4 Transmit Packet Byte Count 0 _B No overflow 1 _B Overflow |

Over-Flow Flag 4

| | | |
|-------------------------|------------------------|-------------------------|
| OFF4 | Offset | Reset Value |
| Over-Flow Flag 4 | 118_H | 0000_H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| P3EC | 15 | lhsc | Overflow of Port 3 Error Count 0 _B No overflow 1 _B Overflow |
| Res | 14 | ro | Reserved |
| P2EC | 13 | lhsc | Overflow of Port 2 Error Count 0 _B No overflow 1 _B Overflow |
| Res | 12 | ro | Reserved |
| P1EC | 11 | lhsc | Overflow of Port 1 Error Count 0 _B No overflow 1 _B Overflow |
| Res | 10 | ro | Reserved |
| P0EC | 9 | lhsc | Overflow of Port 0 Error Count 0 _B No overflow 1 _B Overflow |

Registers Description

HSL **Offset**
Hardware Setting Low Register **130_H** **Reset Value**
0000_H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|-----|----|----|----|----|------|-----|------|----|----|----|----|----|----|
| H | BO | DAF | BP | DB | GM | RM | P4IT | GFC | P4FM | DC | CA | AC | AN | | |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|---|
| H | 15 | ro | Reserved |
| BO | 14 | ro | Bond |
| DAF | 13 | ro | Disable Samurai-6I/6IX (ADM6996I/IX) Function |
| BP | 12 | ro | BPEN |
| DB | 11 | ro | 16/32 Bit Data Bus |
| GM | 10 | ro | GPSI Mode |
| RM | 9 | ro | RMII Mode |
| P4IT | 8:7 | ro | Port 4 Interface Type |
| GFC | 6 | ro | Global Flow Control |
| P4FM | 5 | ro | Port 4 Fiber Mode |
| DC | 4 | ro | Dual Color |
| CA | 3:2 | ro | Chip Address |
| AC | 1 | ro | Auto-Crossover |
| AN | 0 | ro | Auto-Negotiation |

Hardware Setting High Register

HSH **Offset**
Hardware Setting High Register **131_H** **Reset Value**
0000_H

| 15 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|------|-----------|------|-----------|------|-----|-----|-----|----|----|----|
| Res | LTBR | LLTB R | CTBR | HITB R | DBBR | P5M | P4M | CFG | | | |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

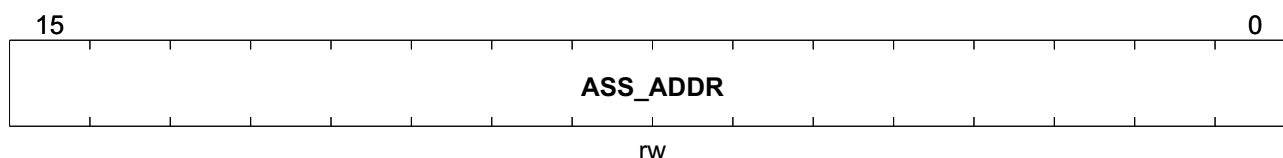
| Field | Bits | Type | Description |
|-------|-------|------|---|
| Res | 15:10 | ro | Reserved |
| LTBR | 9 | ro | Learning Table Bist Result 0 _B Work 1 _B Do not Work |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| LLTBR | 8 | ro | Linklist Table Bist Result (Linklist Table does not do bist test in normal mode) 0 _B Work 1 _B Do not Work |
| CTBR | 7 | ro | Control Table Bist Result 0 _B Work 1 _B Do not Work |
| HITBR | 6 | ro | Hardware IGMP Table Bist Result 0 _B Work 1 _B Do not Work |
| DBBR | 5 | ro | Data Buffer Bist Result 0 _B Work 1 _B Do not Work |
| P5M | 4:3 | ro | P5 Mode 00 _B GPSI 01 _B RMII 10 _B MII |
| P4M | 2:1 | ro | P4 Mode 00 _B Port 4 uses inner PHY 01 _B Port 4 uses MII 10 _B Reserved 11 _B Port 4 isolated PHY |
| CFG | 0 | ro | CFG |

Assign Address [15:0] Register

| | | |
|--------------------------------|------------------|--------------------|
| AA1 | Offset | Reset Value |
| Assign Address [15:0] Register | 132 _H | 0000 _H |



| Field | Bits | Type | Description |
|----------|------|------|-----------------------|
| ASS_ADDR | 15:0 | rw | Assign Address [15:0] |

Assign Address [31:16] Register

| | | |
|---------------------------------|------------------|--------------------|
| AA2 | Offset | Reset Value |
| Assign Address [31:16] Register | 133 _H | 0000 _H |

Registers Description



| Field | Bits | Type | Description |
|----------|------|------|------------------------|
| ASS_ADDR | 15:0 | rw | Assign Address [31:16] |

Assign Address [47:32] Register

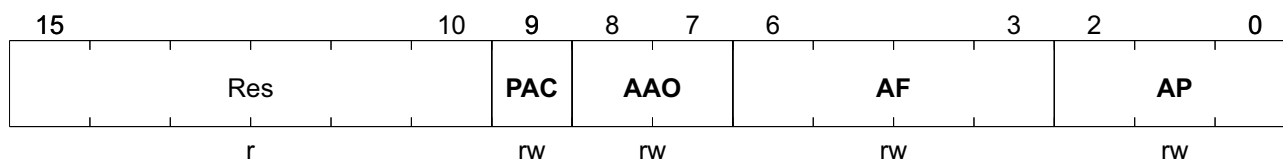
| | | |
|---------------------------------|------------------|--------------------|
| AA3 | Offset | Reset Value |
| Assign Address [47:32] Register | 134 _H | 0000 _H |



| Field | Bits | Type | Description |
|----------|------|------|------------------------|
| ASS_ADDR | 15:0 | rw | Assign Address [47:32] |

Assign Option Register

| | | |
|------------------------|------------------|--------------------|
| AO | Offset | Reset Value |
| Assign Option Register | 135 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|-------|------|-------------|
| Res | 15:10 | r | Reserved |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| PAC | 9 | rw | Pause Address Change It is useful only when assign address is used for PAUSE source address 0 _B All the ports use this assign address as the source address of the PAUSE commands 1 _B Port 0 uses {assign address[47:3], 000 _B } as the source address of the PAUSE commands. Port 1 uses {assign address[47:3], 001 _B } as the source address of the PAUSE commands. Port 2 uses {assign address[47:3], 010 _B } as the source address of the PAUSE commands. Port 3 uses {assign address[47:3], 011 _B } as the source address of the PAUSE commands. Port 4 uses {assign address[47:3], 100 _B } as the source address of the PAUSE commands. Port 5 uses {assign address[47:3], 101 _B } as the source address of the PAUSE commands. |
| AAO | 8:7 | rw | Assign Address Option 00 _B Assign address is useless 01 _B Assign address is used for PAUSE source address 10 _B Assign address is used for assign lock address or the monitor address 11 _B Assign address is used for PAUSE source address |
| AF | 6:3 | rw | Assign Fid It is used for assign lock FID. |
| AP | 2:0 | rw | Assign Port It is used for the port that the user wants to assign or for the monitor port. |

Mirror Register 0

| MIRR0 | Offset | Reset Value |
|-------------------|------------------|-------------------|
| Mirror Register 0 | 136 _H | 0000 _H |

| | | | | | | | | | | | | | | | |
|------|----|------|----|------|----|------|---|------|---|------|---|------|---|------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P3TM | | P3RM | | P2TM | | P2RM | | P1TM | | P1RM | | P0TM | | P0RM | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| P3TM | 15:14 | rw | Port 3 Transmit Mirror Option See register 0136 _H , P0TM for more detail. |
| P3RM | 13:12 | rw | Port 3 Receive Mirror Option See register 0136 _H , P0RM for more detail. |
| P2TM | 11:10 | rw | Port 2 Transmit Mirror Option See register 0136 _H , P0TM for more detail. |
| P2RM | 9:8 | rw | Port 2 Receive Mirror Option See register 0136 _H , P0RM for more detail. |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| P1TM | 7:6 | rw | Port 1 Transmit Mirror Option See register 0136 _H , P0TM for more detail. |
| P1RM | 5:4 | rw | Port 1 Receive Mirror Option See register 0136 _H , P0RM for more detail. |
| P0TM | 3:2 | rw | Port 0 Transmit Mirror Option 00 _B Do not be mirrored 01 _B The traffic transmitted from Port 0 is mirrored 10 _B The traffic with DA = assign address transmitted from Port 0 is mirrored 11 _B The traffic with SA = assign address transmitted from Port 0 is mirrored |
| P0RM | 1:0 | rw | Port 0 Receive Mirror Option 00 _B Do not be mirrored 01 _B The traffic received on Port 0 is mirrored 10 _B The traffic with DA = assign address received on Port 0 is mirrored 11 _B The traffic with SA = assign address received on Port 0 is mirrored |

Mirror Register 1

| MIRR1 | Offset | Reset Value |
|-------------------|------------------|-------------------|
| Mirror Register 1 | 137 _H | 0000 _H |

| | | | | | | | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|----|----|----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ME | MCA | MRA | MPA | MLA | MSA | Res | ETUP | P5TM | P5RM | P4TM | P4RM | | | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

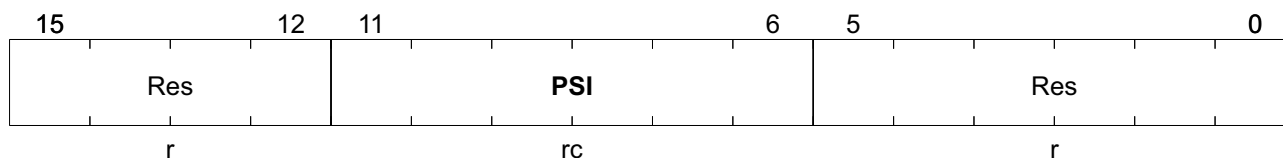
| Field | Bits | Type | Description |
|-------|------|------|---|
| ME | 15 | rw | Mirror Enable 0 _B Disable 1 _B Enable |
| MCA | 14 | rw | Mirror CRC Also 0 _B Do not mirror 1 _B Mirror |
| MRA | 13 | rw | Mirror RXER Also 0 _B Do not mirror 1 _B Mirror |
| MPA | 12 | rw | Mirror PAUSE Also 0 _B Do not mirror 1 _B Mirror |
| MLA | 11 | rw | Mirror Long Also 0 _B Do not mirror 1 _B Mirror |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| MSA | 10 | rw | Mirror Short Also 0 _B Do not mirror 1 _B Mirror |
| Res | 9 | rw | Reserved |
| ETUP | 8 | rw | Enable Transmit Unmonitored Packet to the Mirror Port 0 _B Mirror port only mirrors the mirrored packets 1 _B Mirror port also receives packets that are not mirrored but their output ports also contain the mirror port |
| P5TM | 7:6 | rw | Port 5 Transmit Mirror Option See register 0136 _H , P0TM for more detail. |
| P5RM | 5:4 | rw | Port 5 Receive Mirror Option See register 0136 _H , P0RM for more detail. |
| P4TM | 3:2 | rw | Port 4 Transmit Mirror Option See register 0136 _H , P0TM for more detail. |
| P4RM | 1:0 | rw | Port 4 Receive Mirror Option See register 0136 _H , P0RM for more detail. |

Security Violation Port

| | | |
|--------------------------------|------------------------|-------------------------|
| SVP | Offset | Reset Value |
| Security Violation Port | 138_H | 0000_H |

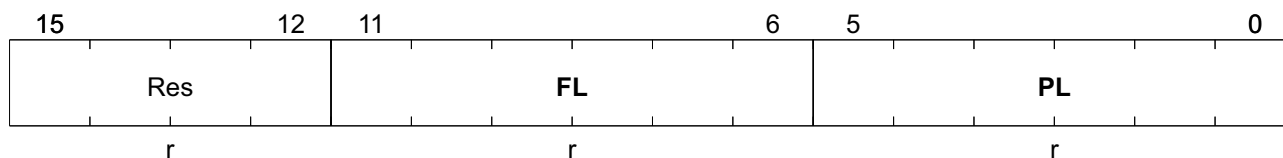


| Field | Bits | Type | Description |
|-------|-------|------|--|
| Res | 15:12 | r | Reserved |
| PSI | 11:6 | rc | Port Source Intrusion 0 _B Source Intrusion did not happen 1 _B Source Intrusion happened |
| Res | 5:0 | r | Reserved |

Security Status 0

| | | |
|--------------------------|------------------------|-------------------------|
| SS0 | Offset | Reset Value |
| Security Status 0 | 139_H | 0000_H |

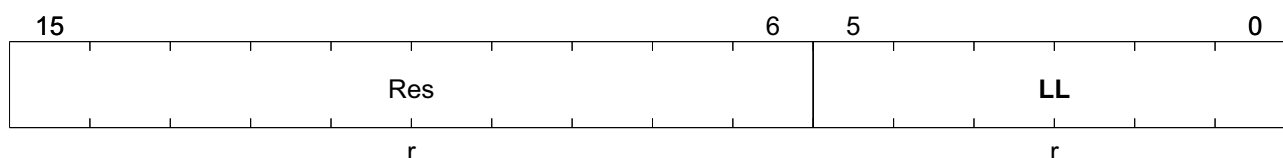
Registers Description



| Field | Bits | Type | Description |
|-------|-------|------|---|
| Res | 15:12 | r | Reserved |
| FL | 11:6 | r | First Lock 0_B Port did not lock the address 1_B Port locked the address |
| PL | 5:0 | r | Port Locked 0_B Port did not close 1_B Port closed because of source violation |

Security Status 1

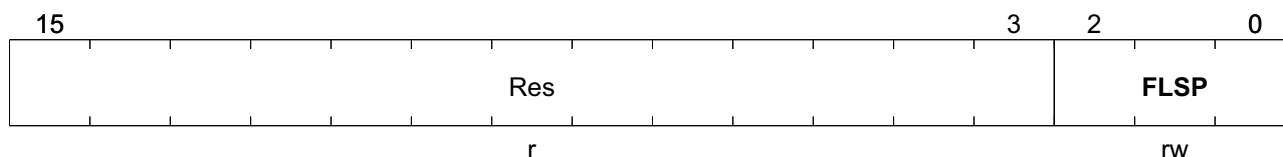
| | | |
|-------------------|------------------|--------------------|
| SS1 | Offset | Reset Value |
| Security Status 1 | 13A _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:6 | r | Reserved |
| LL | 5:0 | r | Link Lock 0_B Link Lock did not happen 1_B Link Lock happened |

First Lock Address Search

| | | |
|---------------------------|------------------|--------------------|
| FLAS | Offset | Reset Value |
| First Lock Address Search | 13B _H | 0000 _H |



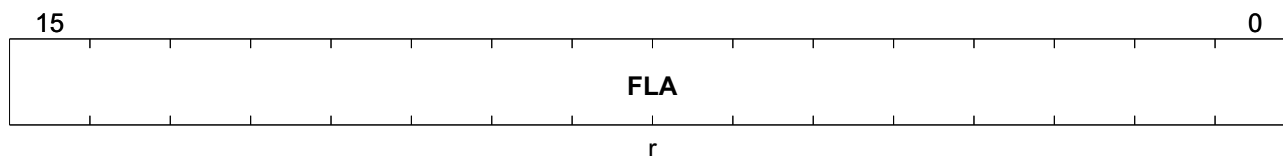
Registers Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:3 | r | Reserved |
| FLSP | 2:0 | rw | First Lock Search Port Users could write this register to get the lock address and the lock FID (returned in the 13C _H , 13D _H , 13E _H , 13F _H) associated with the port. 000 _B Search the address and FID locked on the port 0 001 _B Search the address and FID locked on the port 1 010 _B Search the address and FID locked on the port 1 011 _B Search the address and FID locked on the port 1 100 _B Search the address and FID locked on the port 1 101 _B Search the address and FID locked on the port 1 |

Registers Description

First Lock Address [15:0]

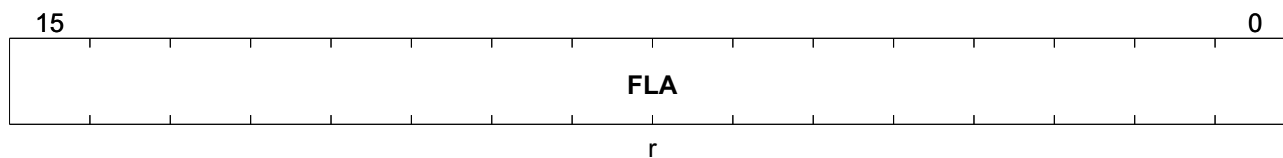
| | | |
|---------------------------|------------------|--------------------|
| FLA1 | Offset | Reset Value |
| First Lock Address [15:0] | 13C _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|---------------------------|
| FLA | 15:0 | r | First Lock Address [15:0] |

First Lock Address [31:16]

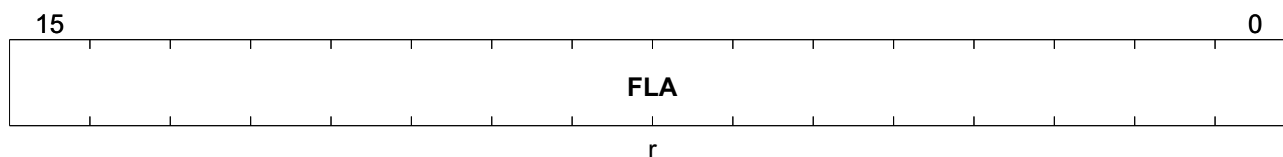
| | | |
|----------------------------|------------------|--------------------|
| FLA2 | Offset | Reset Value |
| First Lock Address [31:16] | 13D _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|----------------------------|
| FLA | 15:0 | r | First Lock Address [31:16] |

First Lock Address [47:32]

| | | |
|----------------------------|------------------|--------------------|
| FLA3 | Offset | Reset Value |
| First Lock Address [47:32] | 13E _H | 0000 _H |

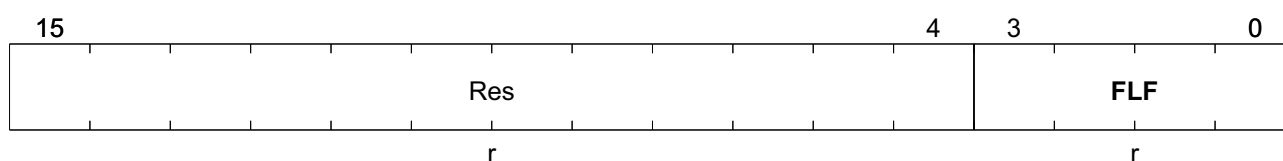


Registers Description

| Field | Bits | Type | Description |
|-------|------|------|----------------------------|
| FLA | 15:0 | r | First Lock Address [47:32] |

First Lock FID

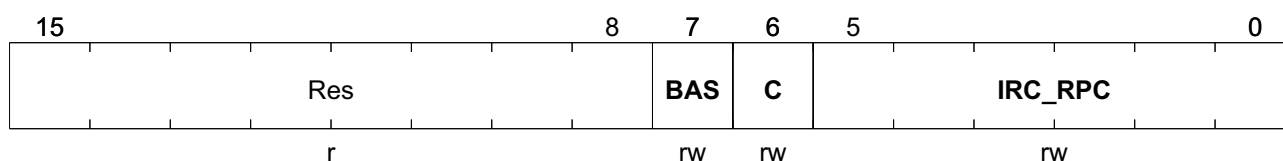
| | | |
|----------------|------------------|--------------------|
| FLF | Offset | Reset Value |
| First Lock FID | 13F _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|----------------|
| Res | 15:4 | r | Reserved |
| FLF | 3:0 | r | First Lock FID |

Counter Control Low Register

| | | |
|------------------------------|------------------|--------------------|
| CCL | Offset | Reset Value |
| Counter Control Low Register | 140 _H | 0000 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| Res | 15:8 | r | Reserved |
| BAS | 7 | rw | Busy/Access Start 0 _B The counter control is free 1 _B The counter control is busy, or users should write 1 _B into this bit to start the access when the engine is free |
| C | 6 | rw | Counter 0 _B Indirect Read Counter 1 _B Renew Port Counter |

Registers Description

| Field | Bits | Type | Description |
|---------|------|------|--|
| IRC_RPC | 5:0 | rw | Indirect Read Counter It means the counter address Renew Port Counter It means the counters on each port to renew |

| Field | Bits | Type | Description |
|---------|------|------|-----------------|
| COUNTER | 15:0 | r | Counter [31:16] |

4.4 PHY Registers

PHY Control Register of Port 0

| | | |
|--------------------------------|------------------|-------------------|
| PHY_C0 | Offset | Reset Value |
| PHY Control Register of Port 0 | 200 _H | 3100 _H |

| | | | | | | | | | | | | | | | | |
|--------|------|----------|------|-----|-----|----------|------|---------|----------|---|--|--|--|--|--|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | | | | | | 0 |
| RST | LPBK | SPEED_L* | ANEN | PDN | ISO | ANEN_RST | DPLX | COLT ST | SPEED_M* | | | | | | | Res |
| rw, sc | rw | rw | rw | rw | rw | rw, sc | rw | rw | ro | | | | | | | |

| Field | Bits | Type | Description |
|-----------|------|--------|--|
| RST | 15 | rw, sc | RESET Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values. The software reset process takes $25 \leq t_{\text{rs}}$ to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete. 0 _B Normal operation 1 _B PHY Reset |
| LPBK | 14 | rw | Loop Back Enable This bit controls the PHY loopback operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit 12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register. 0 _B Disable Loopback mode 1 _B Enable loopback mode |
| SPEED_LSB | 13 | rw | Speed Selection LSB, 0.6, 0.13 Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). If it is fiber mode, 0.13 is always 1. Any write to this bit will have no effect. 00 _B 10 Mbit/s 01 _B 100 Mbit/s 10 _B 1000 Mbit/s 11 _B Reserved |

Registers Description

| Field | Bits | Type | Description |
|-----------|------|--------|---|
| ANEN | 12 | rw | Auto Negotiation Enable This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the RECANEN pin detects a logic 1 input level in Twisted-Pair Mode. If it is set when fiber mode is configured, any write to this bit will be ignored . 0 _B Disable Auto negotiation process 1 _B Enable auto negotiation process |
| PDN | 11 | rw | Power Down Enable Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY into power down mode. During the power down mode, TXP/TXN and all LED outputs are tristated and the MII interfaces are isolated. 0 _B Normal Operation 1 _B Power Down |
| ISO | 10 | rw | Isolate PHY from Network Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the PHY does not respond to TXD, TXEN and TXER inputs, and it presents a high impedance on its TXC, RXC, CRSDV, RXER, RXD , COL and CRS outputs. 0 _B Normal Operation 1 _B Isolate PHY from MII |
| ANEN_RST | 9 | rw, sc | Restart Auto Negotiation Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced. 0 _B Normal Operation 1 _B Restart Auto Negotiation Process |
| DPLX | 8 | rw | Duplex Mode If auto negotiation is disabled, this bit determines the duplex mode for the link. 0 _B Half Duplex mode 1 _B Full Duplex mode |
| COLTST | 7 | rw | Collision Test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN. 0 _B Disable COL signal test 1 _B Enable COL signal test |
| SPEED_MSB | 6 | ro | Speed Selection MSB Set to 0 all the time indicate that the PHY does not support 1000 Mbit/s function. |

Similar Registers

All PHY_Cx registers have the same structure and characteristics, see [PHY_C0](#).
The offset addresses of the other PHY_Cx registers are listed in [Table 66](#).

Registers Description

Table 66 PHY_Cx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------------------|------------------|-------------|
| PHY_C1 | PHY Control Register of Port 1 | 220 _H | |
| PHY_C2 | PHY Control Register of Port 2 | 240 _H | |
| PHY_C3 | PHY Control Register of Port 3 | 260 _H | |
| PHY_C4 | PHY Control Register of Port 4 | 280 _H | |

PHY Status Register of Port 0

| | | |
|--------------------------------------|------------------------|-------------------------|
| PHY_S0 | Offset | Reset Value |
| PHY Status Register of Port 0 | 201_H | 7849_H |

| | | | | | | | | | | | | | | | |
|---------------|----------------|----------------|---------------|---------------|---------------|---|-----|---|-----------------|----------------|----------------|-----------------|-------------|------------|----------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAP_T4 | CAP_TXF | CAP_TXH | CAP_TF | CAP_TH | CAP_T2 | | Res | | CAP_SUPR | AN_COMP | REM_FLT | CAP_ANEG | LINK | JAB | EXTR EG |
| ro | ro | ro | ro | ro | ro | | | | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|----------|------|------|--|
| CAP_T4 | 15 | ro | 100Base-T4 Capable Set to 0 all the time to indicate that the PHY does not support 100Base-T4 |
| CAP_TXF | 14 | ro | 100Base-X Full Duplex Capable Set to 1 all the time to indicate that the PHY does support Full Duplex mode |
| CAP_TXH | 13 | ro | 100Base-X Half Duplex Capable Set to 1 all the time to indicate that the PHY does support Half Duplex mode |
| CAP_TF | 12 | ro | 10M Full Duplex Capable TP : Set to 1 all the time to indicate that the PHY does support 10M Full Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Full Duplex mode |
| CAP_TH | 11 | ro | 10M Half Duplex Capable TP : Set to 1 all the time to indicate that the PHY does support 10M Half Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Half Duplex mode |
| CAP_T2 | 10 | ro | 100Base-T2 Capable Set to 0 all the time to indicate that the PHY does not support 100Base-T2 |
| CAP_SUPR | 6 | ro | MF Preamble Suppression Capable This bit is hardwired to 1 indicating that the PHY accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification. |

Registers Description

| Field | Bits | Type | Description |
|----------|------|------|--|
| AN_COMP | 5 | ro | Auto Negotiation Complete If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected. 0 _B Auto Negotiation process not completed 1 _B Auto Negotiation process completed |
| REM_FLT | 4 | ro | Remote Fault Detect This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05 _H) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read. 0 _B Remote Fault not detected 1 _B Remote Fault detected |
| CAP_ANEG | 3 | ro | Auto Negotiation Ability TP : This bit is set to 1 all the time, indicating that PHY is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that PHY is not capable of auto negotiation in Fiber Mode. 0 _B Not capable of auto negotiation 1 _B Capable of auto negotiation |
| LINK | 2 | ro | Link Status This bit reflects the current state of the link – test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status 0 _B Link is down 1 _B Link is up |
| JAB | 1 | ro | Jabber Detect 0 _B Jabber condition not detected 1 _B Jabber condition detected |
| EXTREG | 0 | ro | Extended Capability This bit defaults to 1, indicating that the PHY implements extended registers. 0 _B No extended register set 1 _B Extended register set |

Similar Registers

All PHY_Sx registers have the same structure and characteristics, see [PHY_S0](#).

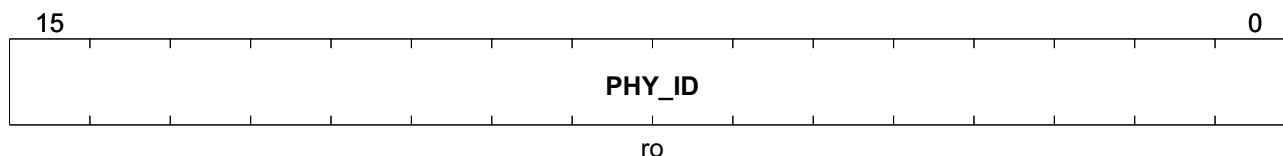
The offset addresses of the other PHY_Sx registers are listed in [Table 67](#).

Table 67 PHY_Sx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|-------------------------------|------------------|-------------|
| PHY_S1 | PHY Status Register of Port 1 | 221 _H | |
| PHY_S2 | PHY Status Register of Port 2 | 241 _H | |
| PHY_S3 | PHY Status Register of Port 3 | 261 _H | |
| PHY_S4 | PHY Status Register of Port 4 | 281 _H | |

PHY Identifier Register of Port 0 (A)

| | | |
|---------------------------------------|------------------|--------------------|
| PHY_I0_A | Offset | Reset Value |
| PHY Identifier Register of Port 0 (A) | 202 _H | 0302 _H |



| Field | Bits | Type | Description |
|--------|------|------|--------------|
| PHY_ID | 15:0 | ro | IEEE Address |

Similar Registers

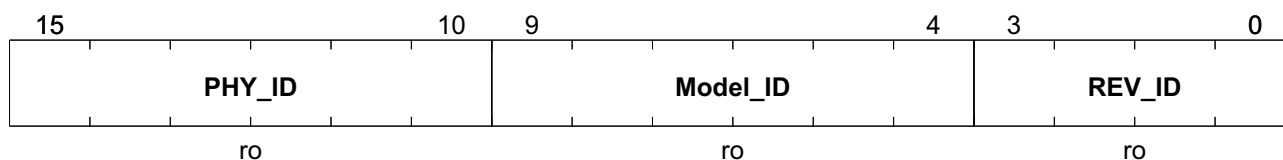
All PHY_Ix_A registers have the same structure and characteristics, see [PHY_I0_A](#).
The offset addresses of the other PHY_Ix_A registers are listed in [Table 68](#).

Table 68 PHY_Ix_A Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------------------------|------------------|-------------|
| PHY_I1_A | PHY Identifier Register of Port 1 (A) | 222 _H | |
| PHY_I2_A | PHY Identifier Register of Port 2 (A) | 242 _H | |
| PHY_I3_A | PHY Identifier Register of Port 3 (A) | 262 _H | |
| PHY_I4_A | PHY Identifier Register of Port 4 (A) | 282 _H | |

PHY Identifier Register of Port 0 (B)

| | | |
|---------------------------------------|------------------|--------------------|
| PHY_I0_B | Offset | Reset Value |
| PHY Identifier Register of Port 0 (B) | 203 _H | 6071 _H |



| Field | Bits | Type | Description |
|----------|-------|------|-------------------|
| PHY_ID | 15:10 | ro | IEEE Address |
| Model_ID | 9:4 | ro | IEEE Model No. |
| REV_ID | 3:0 | ro | IEEE Revision No. |

Similar Registers

All PHY_Ix_B registers have the same structure and characteristics, see [PHY_I0_B](#).
The offset addresses of the other PHY_Ix_B registers are listed in [Table 69](#).

Table 69 PHY_Ix_B Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------------------------|------------------|-------------|
| PHY_I1_B | PHY Identifier Register of Port 1 (B) | 223 _H | |
| PHY_I2_B | PHY Identifier Register of Port 2 (B) | 243 _H | |
| PHY_I3_B | PHY Identifier Register of Port 3 (B) | 263 _H | |
| PHY_I4_B | PHY Identifier Register of Port 4 (B) | 283 _H | |

Auto Negotiation Advertisement Register of Port 0

| | | |
|--|------------------------|-------------------------|
| ANAP0 | Offset | Reset Value |
| Auto Negotiation Advertisement Register of Port 0 | 204_H | 05E1_H |

| | | | | | | | | | | | | | | | |
|----|-----|----|-----|---------|-------|----|--------|--------|--------|--------|---|--|--|----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | | | 0 |
| NP | Res | RF | Res | ASM_DIR | PAUSE | T4 | TX_FDX | TX_HDX | 10_FDX | 10_HDX | | | | SF | |
| ro | | ro | | rw | rw | ro | rw | rw | rw | rw | | | | ro | |

| Field | Bits | Type | Description |
|---------|------|------|--|
| NP | 15 | ro | Next Page This bit defaults to 1, indicating that PHY is next page capable |
| RF | 13 | ro | Remote Fault This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner. 0 _B No remote fault has been detected 1 _B Remote Fault has been detected |
| ASM_DIR | 11 | rw | Asymmetric Pause Direction Bit[11:10] Capability 00 _B No Pause 01 _B Symmetric PAUSE 10 _B Asymmetric PAUSE toward Link Partner 11 _B Both Symmetric PAUSE and Asymmetric PAUSE toward local device |
| PAUSE | 10 | rw | Pause Operation for Full Duplex Value on PAUREC will be stored in this bit during power on reset. |
| T4 | 9 | ro | Technology Ability for 100Base-T4 Defaults to 0. |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|--|
| TX_FDX | 8 | rw | 100Base-TX Full Duplex 0 _B Not capable of 100M Full duplex operation 1 _B Capable of 100M Full duplex operation |
| TX_HDX | 7 | rw | 100Base-TX Half Duplex 0 _B Not capable of 100M operation 1 _B Capable of 100M operation |
| 10_FDX | 6 | rw | 10BASE-T Full Duplex 0 _B Not capable of 10M full duplex operation 1 _B Capable of 10M Full Duplex operation |
| 10_HDX | 5 | rw | 10Base-T Half Duplex <i>Note: Bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.</i> 0 _B Not capable of 10M operation 1 _B Capable of 10M operation |
| SF | 4:0 | ro | Selector Field These 5 bits are hardwired to 00001 _B , indicating that the PHY supports IEEE 802.3 CSMA/CD. |

Similar Registers

All ANAPx registers have the same structure and characteristics, see [ANAP0](#).

The offset addresses of the other ANAPx registers are listed in [Table 70](#).

Table 70 ANAPx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|------------------|-------------|
| ANAP1 | Auto Negotiation Advertisement Register of Port 1 | 224 _H | |
| ANAP2 | Auto Negotiation Advertisement Register of Port 2 | 244 _H | |
| ANAP3 | Auto Negotiation Advertisement Register of Port 3 | 264 _H | |
| ANAP4 | Auto Negotiation Advertisement Register of Port 4 | 284 _H | |

Auto Negotiation Link Partner Ability Register of Port 0

| | | |
|---|------------------------|-------------------------|
| ANLPA0 | Offset | Reset Value |
| Auto Negotiation Link Partner Ability Register of Port 0 | 205_H | 01E1_H |

| | | | | | | | | | | | | | | | | |
|-----------|-----|----|-----|------------|------------|-----------|------------|------------|------------|------------|---|--|--|--|----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | | | | 0 |
| NPAG E | ACK | RF | Res | LP_D IR | LP_P AU | LP_T 4 | LP_F DX | LP_H DX | LP_F 10 | LP_H 10 | | | | | SF | |
| ro | ro | ro | | ro | ro | ro | ro | ro | ro | ro | | | | | ro | |

Registers Description

| Field | Bits | Type | Description |
|--------|------|------|---|
| NPAGE | 15 | ro | Next Page 0 _B Not capable of next page function 1 _B Capable of next page function |
| ACK | 14 | ro | Acknowledge 0 _B Not acknowledged 1 _B Link Partner acknowledges reception of the ability data word |
| RF | 13 | ro | Remote Fault 0 _B No remote fault has been detected 1 _B Remote Fault has been detected |
| LP_DIR | 11 | ro | Link Partner Asymmetric Pause Direction |
| LP_PAU | 10 | ro | Link Partner Pause CapabilityValue on PAUREC Will be stored in this bit during power on reset. |
| LP_T4 | 9 | ro | Link Partner Technology Ability For 100Base-T4Defaults to 0. |
| LP_FDX | 8 | ro | 100Base-TX Full Duplex 0 _B Not capable of 100M Full duplex operation 1 _B Capable of 100M Full duplex operation |
| LP_HDX | 7 | ro | 100Base-TX Half Duplex 0 _B Not capable of 100M operation 1 _B Capable of 100M operation |
| LP_F10 | 6 | ro | 10BASE-T Full Duplex 0 _B Not capable of 10M full duplex operation 1 _B Capable of 10M Full Duplex operation |
| LP_H10 | 5 | ro | 10Base-T Half Duplex 0 _B Not capable of 10M operation 1 _B Capable of 10M operation |
| SF | 4:0 | ro | Selector Field Encoding Definitions |

Similar Registers

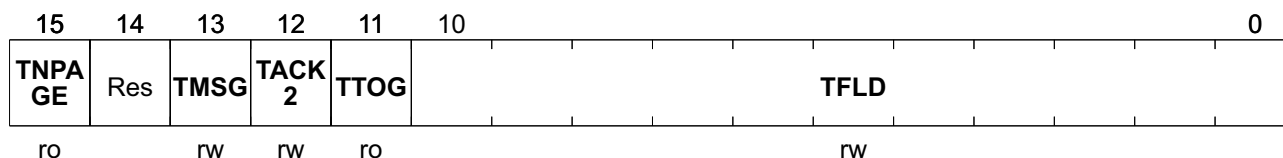
All ANLPAX registers have the same structure and characteristics, see [ANLPA0](#).

The offset addresses of the other ANLPAX registers are listed in [Table 71](#).

Table 71 ANLPAX Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--|------------------|-------------|
| ANLPA1 | Auto Negotiation Link Partner Ability Register of Port 1 | 225 _H | |
| ANLPA2 | Auto Negotiation Link Partner Ability Register of Port 2 | 245 _H | |
| ANLPA3 | Auto Negotiation Link Partner Ability Register of Port 3 | 265 _H | |
| ANLPA4 | Auto Negotiation Link Partner Ability Register of Port 4 | 285 _H | |

Registers Description



| Field | Bits | Type | Description |
|--------|------|------|---|
| TNPAGE | 15 | ro | Transmit Next Page Transmit Code Word Bit 15 |
| TMSG | 13 | rw | Transmit Message Page Transmit Code Word Bit 13 |
| TACK2 | 12 | rw | Transmit Acknowledge 2 Transmit Code Word Bit 12 |
| TTOG | 11 | ro | Transmit Toggle Transmit Code Word Bit 11 |
| TFLD | 10:0 | rw | Transmit Message Field Transmit Code Word Bit 10..0 |

Similar Registers

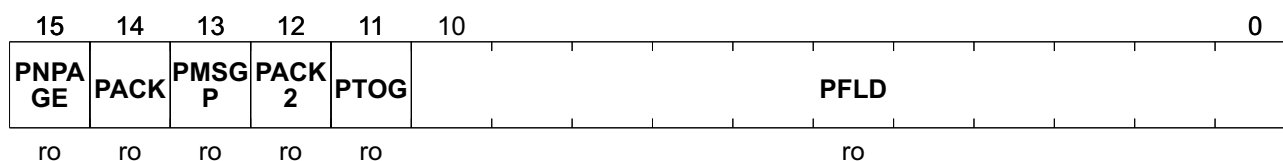
All NPTx registers have the same structure and characteristics, see [NPT0](#).
The offset addresses of the other NPTx registers are listed in [Table 73](#).

Table 73 NPTx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------------------------|------------------|-------------|
| NPT1 | Next Page Transmit Register of Port 1 | 227 _H | |
| NPT2 | Next Page Transmit Register of Port 2 | 247 _H | |
| NPT3 | Next Page Transmit Register of Port 3 | 267 _H | |
| NPT4 | Next Page Transmit Register of Port 4 | 287 _H | |

Link Partner Next Page Register of Port 0

| | | |
|--|------------------------|-------------------------|
| LPNP0 | Offset | Reset Value |
| Link Partner Next Page Register of Port 0 | 208_H | 0000_H |



| Field | Bits | Type | Description |
|--------|------|------|---|
| PNPAGE | 15 | ro | Link Partner Next Page Receive Code Word Bit 15 |

Registers Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| PACK | 14 | ro | Link Partner Acknowledge Receive Code Word Bit 14 |
| PMSGP | 13 | ro | Link Partner Message Page Receive Code Word Bit 13 |
| PACK2 | 12 | ro | Link Partner Acknowledge 2 Receive Code Word Bit 12 |
| PTOG | 11 | ro | Link Partner Toggle Receive Code Word Bit 11 |
| PFLD | 10:0 | ro | Link Partner Message Field Receive Code Word Bit 11 |

Similar Registers

All LPNPx registers have the same structure and characteristics, see [LPNP0](#).
The offset addresses of the other LPNPx registers are listed in [Table 74](#).

Table 74 LPNPx Registers

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---|------------------|-------------|
| LPNP1 | Link Partner Next Page Register of Port 1 | 228 _H | |
| LPNP2 | Link Partner Next Page Register of Port 2 | 248 _H | |
| LPNP3 | Link Partner Next Page Register of Port 3 | 268 _H | |
| LPNP4 | Link Partner Next Page Register of Port 4 | 288 _H | |

5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

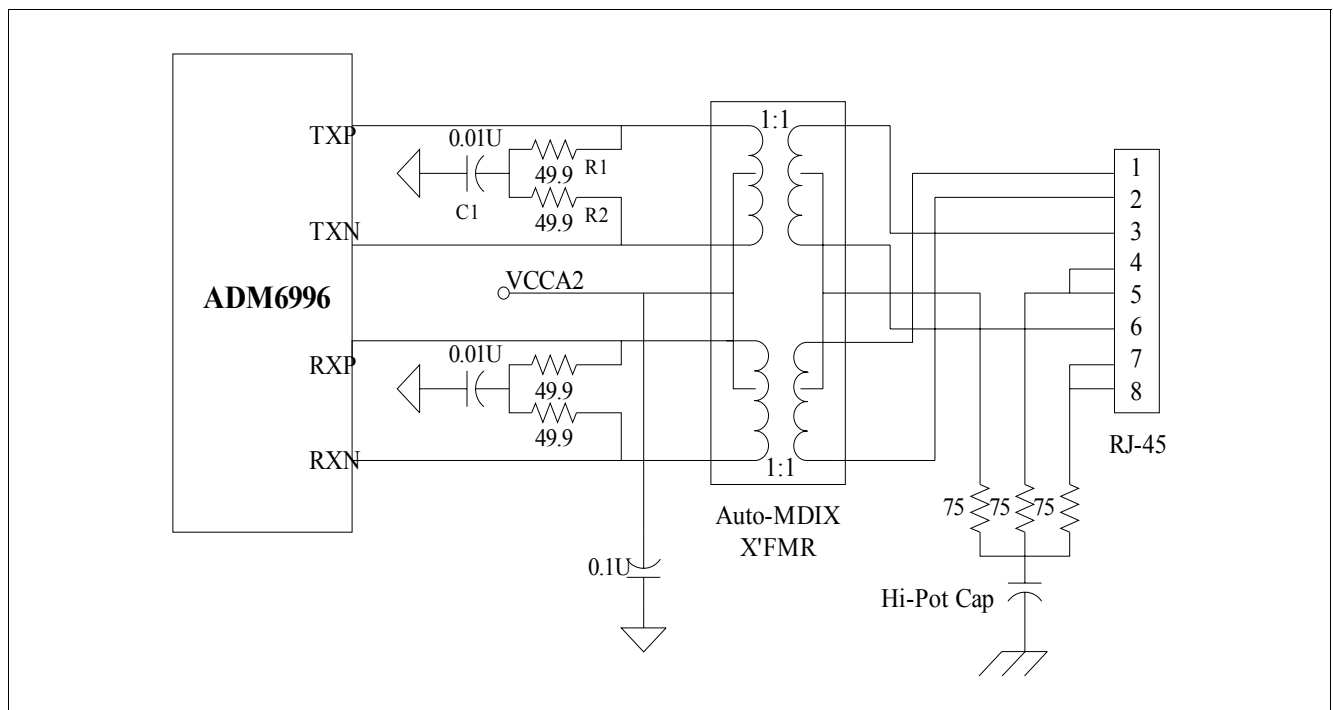


Figure 15 TP Interface

Transformer requirements:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2

Users can change the TX/RX pin for easy layout but do not change the polarity. Samurai-6I/6IX (ADM6996I/IX) supports auto polarity on the receiving side.

5.1.2 FX Interface

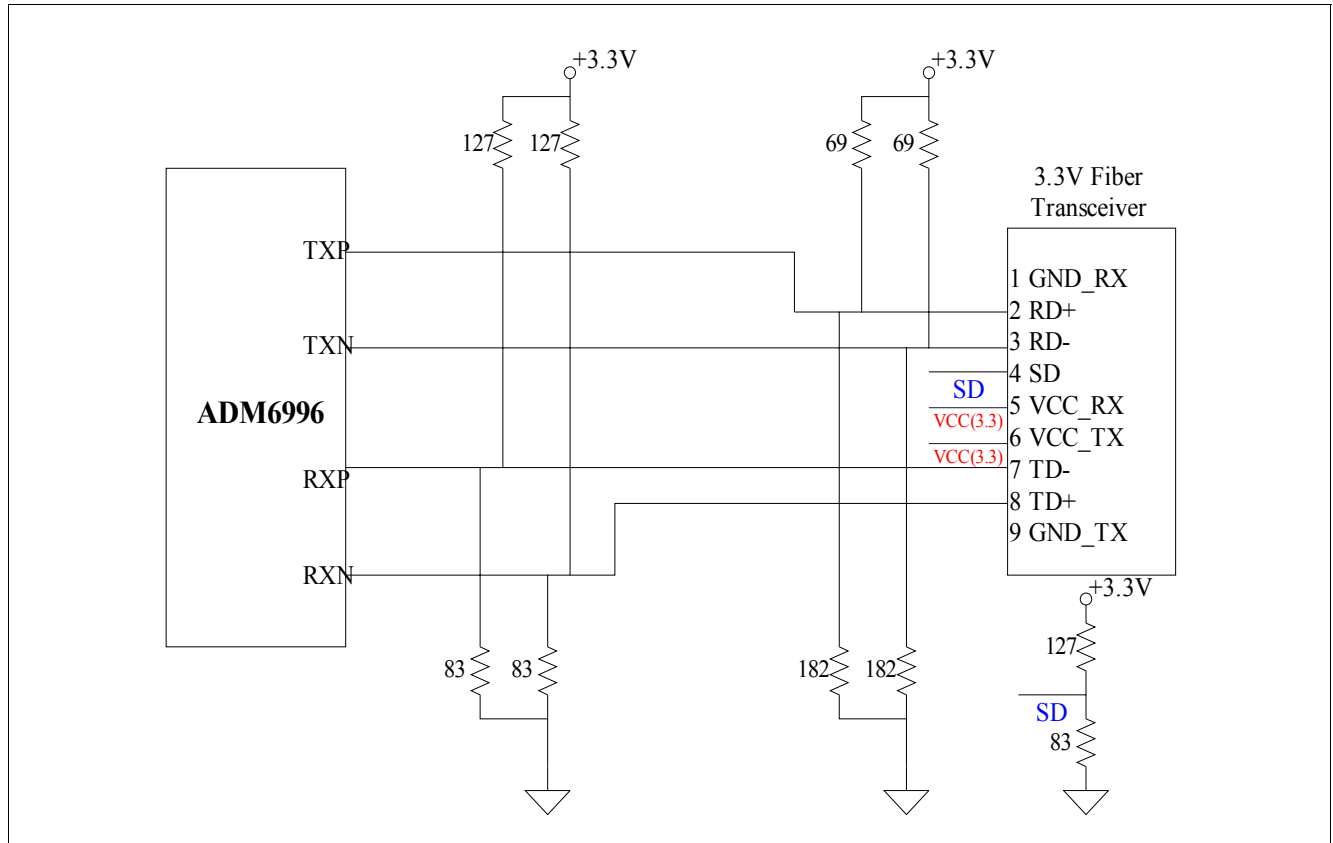


Figure 16 FX Interface

5.2 DC Characterization

Table 75 Power Consumption

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Power consumption when all twisted pair ports are linked at 100 Mbit/s. | P_{100M_5TP} | — | 980 | — | mW | Under EEPROM Register 29 _H = C000 _H , and 30 _H = 985 _H |
| Power consumption when all twisted pair ports are linked at 10 Mbit/s (include transformer). | P_{10M_5TP} | — | 1450 | — | mW | Under EEPROM Register 29 _H = C000 _H , and 30 _H = 985 _H |
| Power consumption when all twisted pair ports are disconnected. | P_{DIS_5TP} | — | 500 | — | mW | Under EEPROM Register 29 _H = C000 _H , and 30 _H = 985 _H |

Electrical Specification

Table 76 Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|------------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| 3.3 V Power Supply for I/O pad | V_{CC30} | 2.97 | 3.3 | 3.63 | V | – |
| 3.3 V Power Supply for bias circuit | V_{CCBS} | 2.97 | 3.3 | 3.63 | V | – |
| 3.3 V Power Supply for A/D converter | V_{CCAD} | 2.97 | 3.3 | 3.63 | V | – |
| 1.8 V Power Supply for line driver | V_{CCA2} | 1.62 | 1.8 | 1.98 | V | – |
| 1.8 V Power Supply for PLL | V_{CCPLL} | 1.62 | 1.8 | 1.98 | V | – |
| 1.8 V Power Supply for Digital core | V_{CCIK} | 1.62 | 1.8 | 1.98 | V | – |
| Input Voltage | V_{IN} | -0.3 | – | $V_{CC30} + 0.3$ | V | – |
| Output Voltage | V_{out} | -0.3 | – | $V_{CC30} + 0.3$ | V | – |
| Maximum current for 3.3 V power supply | $I_{3.3VMAX}$ | – | – | 100 | mA | – |
| Maximum current for 1.8 V power supply (include transformer) | $I_{1.8VMAX}$ | – | – | 800 | mA | – |
| Storage Temperature | T_{STG} | -55 | – | 155 | °C | – |
| Thermal Resistance | θ_{JA} | | 33.0 | | °C/W | |
| | θ_{JC} | | 14.9 | | °C/W | |
| ESD Rating | ESD | 1.0 | – | – | kV | – |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 77 Recommended Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------------|-------------|--------|------|-------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| 3.3 V Power Supply for I/O pad | V_{CC30} | 3.135 | 3.3 | 3.465 | V | – |
| 3.3 V Power Supply for bias circuit | V_{CCBS} | 3.135 | 3.3 | 3.465 | V | – |
| 3.3 V Power Supply for A/D converter | V_{CCAD} | 3.135 | 3.3 | 3.465 | V | – |
| 1.8 V Power Supply for line driver | V_{CCA2} | 1.71 | 1.8 | 1.89 | V | – |
| 1.8 V Power Supply for PLL | V_{CCPLL} | 1.71 | 1.8 | 1.89 | V | – |
| 1.8 V Power Supply for Digital core | V_{CCIK} | 1.71 | 1.8 | 1.89 | V | – |

Table 77 Recommended Operating Conditions (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|----------|--------|------|----------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Input Voltage | V_{in} | 0 | – | V_{CC} | V | – |
| Junction Operating Temperature | T_j | 0 | 25 | 115 | °C | – |

Table 78 DC Electrical Characteristics for 3.3 V Operation¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|----------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input Low Voltage | V_{IL} | – | – | 0.8 | V | TTL |
| Input High Voltage | V_{IH} | 2.0 | – | – | V | TTL |
| Output Low Voltage | V_{OL} | – | – | 0.4 | V | TTL |
| Output High Voltage | V_{OH} | 2.4 | – | – | V | TTL |
| Input Pull-up/down Resistance | R_i | – | 50 | – | kΩ | $V_{IL} = 0\text{ V}$ or $V_{IH} = V_{cc3o}$ |

1) Under $V_{CC3O} = 2.97\text{V} \sim 3.63\text{ V}$, $T_j = 0\text{ °C} \sim 115\text{ °C}$

5.3 AC Characterization

5.3.1 XTAL/OSC Timing

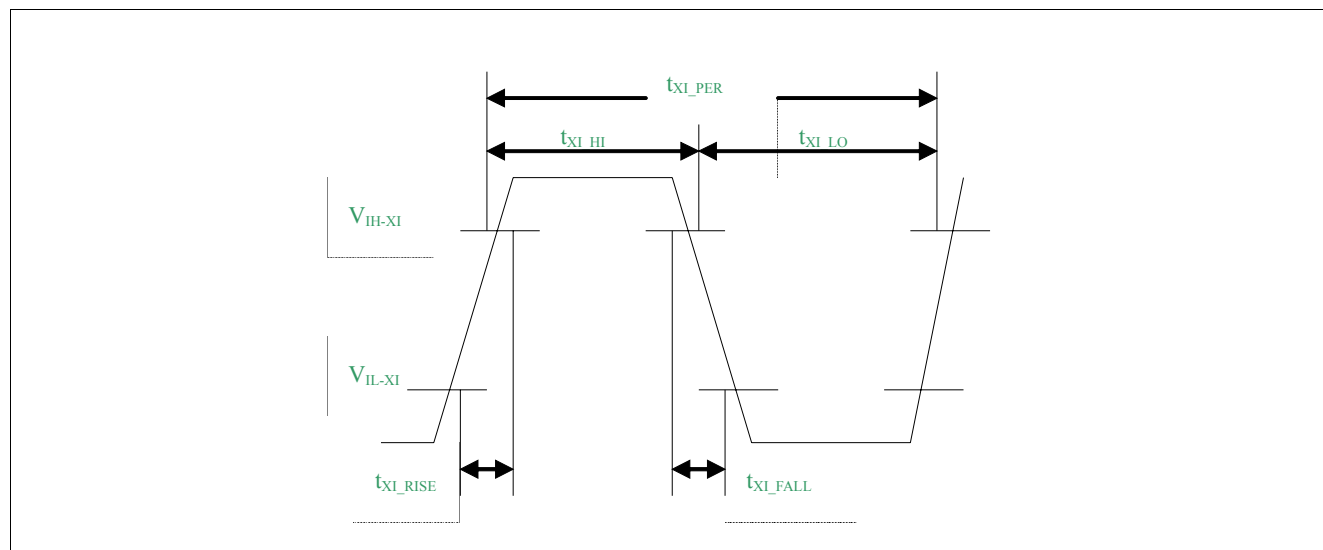


Figure 17 XTAL/OSC Timing

Table 79 XTAL/OSC Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------------|--------------|------|--------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| XI/OSCI Clock Period | t_{XI_PER} | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | — |
| XI/OSCI Clock High | t_{XI_HI} | 14 | 20.0 | — | ns | — |
| XI/OSCI Clock Low | t_{XI_LO} | 14 | 20.0 | — | ns | — |
| XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.) | t_{XI_RISE} | — | — | 4 | ns | — |
| XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max) | t_{XI_FALL} | — | — | 4 | ns | — |

5.3.2 Power On Reset

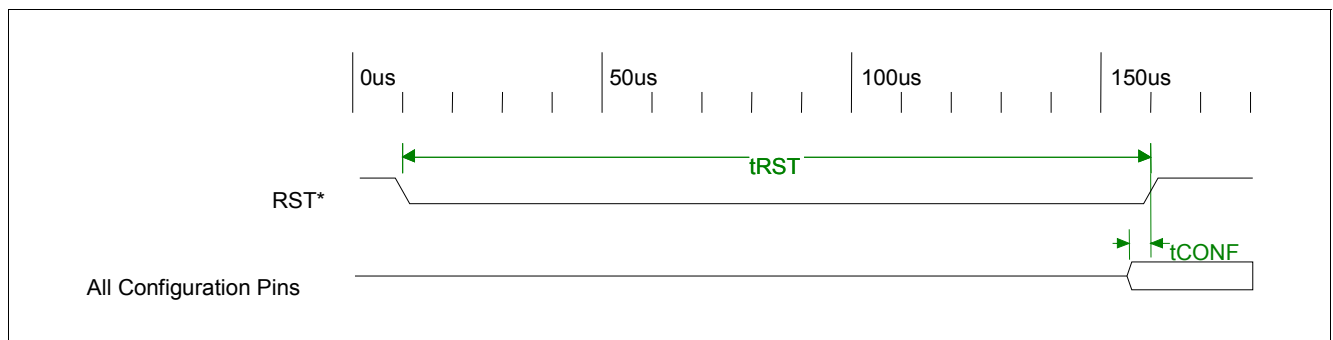


Figure 18 Power On Reset Timing

Table 80 Power On Reset Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| RST Low Period | t_{RST} | 100 | — | — | ms | — |
| Start of Idle Pulse Width | t_{CONF} | 100 | — | — | ns | — |

5.3.3 EEPROM Interface Timing

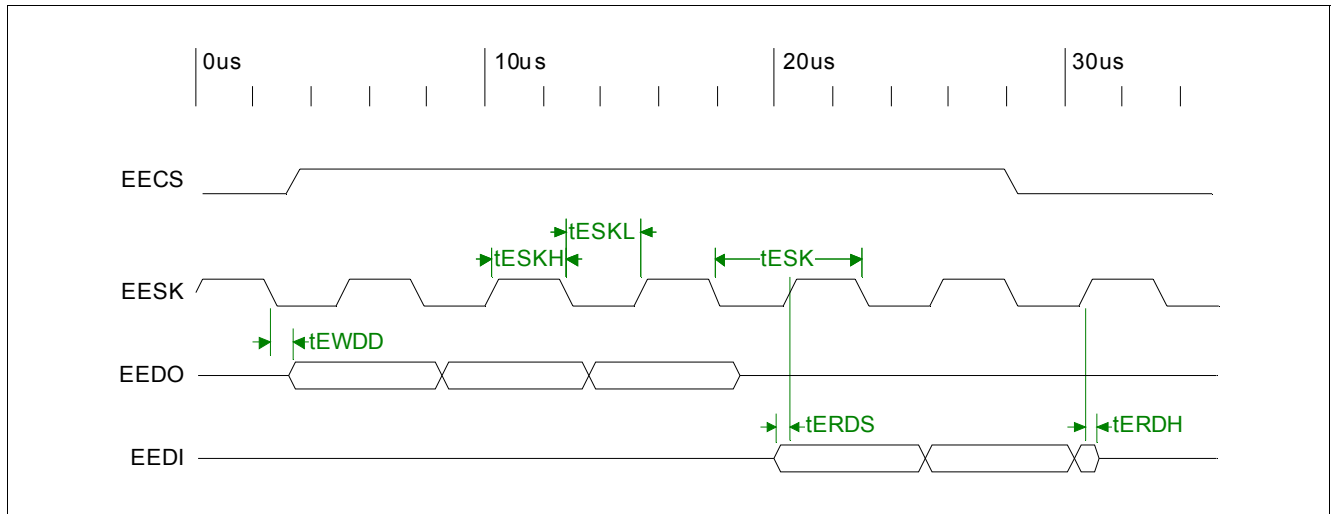


Figure 19 EEPROM Interface Timing

Table 81 EEPROM Interface Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| EESK Period | t_{ESK} | — | 5120 | — | ns | — |
| EESK Low Period | t_{ESKL} | 2550 | — | 2570 | ns | — |
| EESK High Period | t_{ESKH} | 2550 | — | 2570 | ns | — |
| EEDI to EESK Rising Setup Time | t_{ERDS} | 10 | — | — | ns | — |
| EEDI to EESK Rising Hold Time | t_{ERDH} | 10 | — | — | ns | — |
| EESK Falling to EDO Output Delay Time | t_{EWDD} | — | — | 20 | ns | — |

5.3.4 10Base-TX MII Input Timing

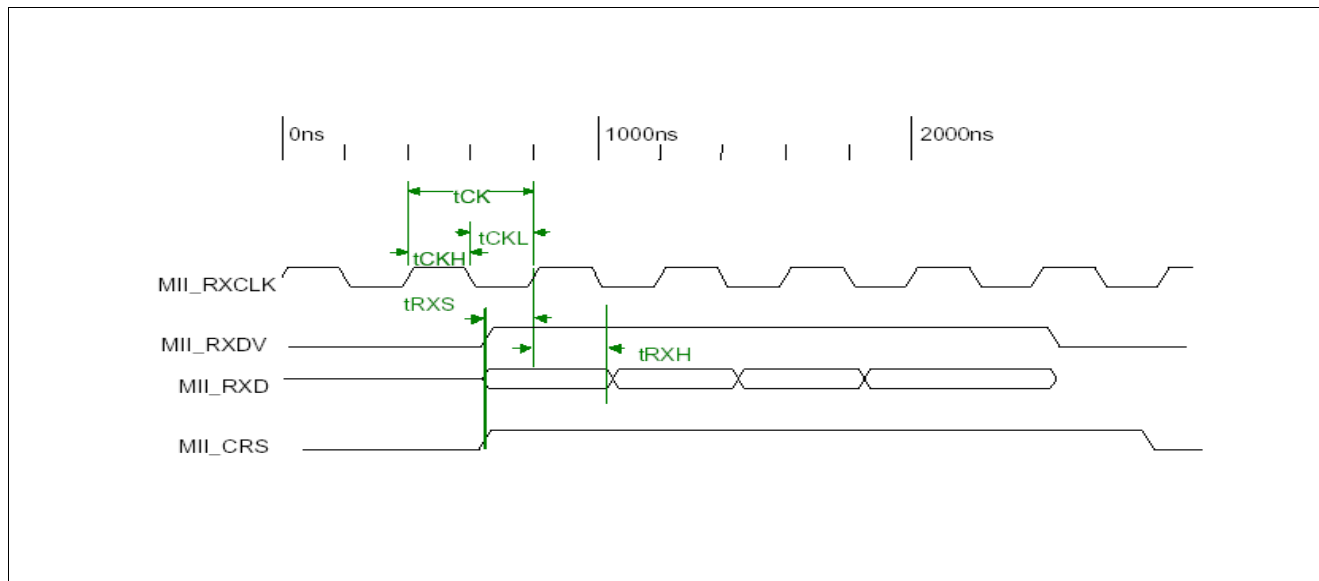


Figure 20 10Base-TX MII Input Timing

Table 82 10Base-TX MII Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_RXCLK Period | t_{CK} | – | 400 | – | ns | – |
| MII_RXCLK Low Period | t_{CKL} | 180 | – | 220 | ns | – |
| MII_RXCLK High Period | t_{CKH} | 180 | – | 220 | ns | – |
| MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising setup | t_{RXS} | 10 | – | – | ns | – |
| MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising hold | t_{RXH} | 10 | – | – | ns | – |

5.3.5 10Base-TX MII Output Timing

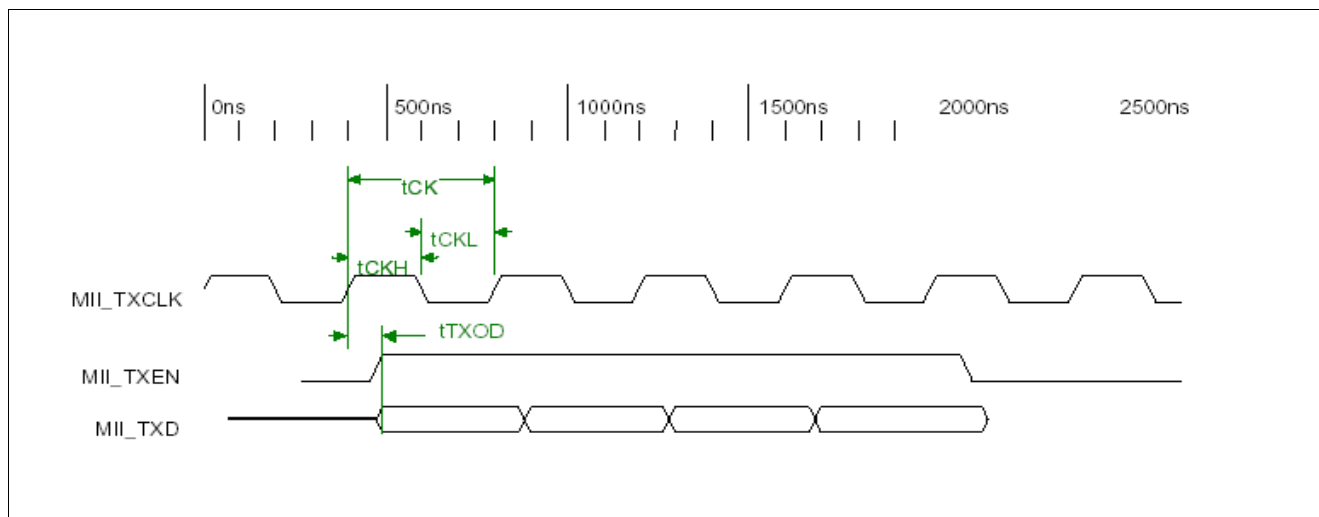


Figure 21 10Base-TX MII Output Timing

Table 83 10-Base-TX MII Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_TXCLK Period | t_{CK} | – | 400 | – | ns | – |
| MII_TXCLK Low Period | t_{CKL} | 180 | – | 220 | ns | – |
| MII_TXCLK High Period | t_{CKH} | 180 | – | 220 | ns | – |
| MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay | t_{TXOD} | 0 | – | 25 | ns | – |

5.3.6 100Base-TX MII Input Timing

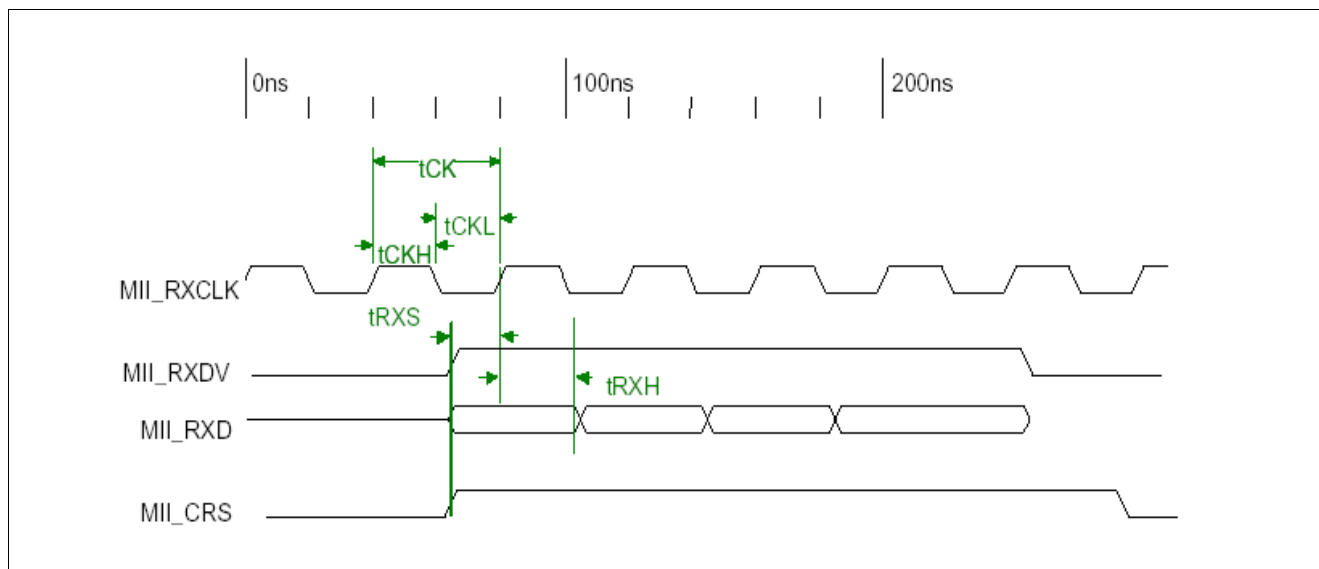


Figure 22 100Base-TX MII Input Timing

Table 84 100Base-TX MII Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_RXCLK Period | t_{CK} | – | 40 | – | ns | – |
| MII_RXCLK Low Period | t_{CKL} | 18 | – | 22 | ns | – |
| MII_RXCLK High Period | t_{CKH} | 18 | – | 22 | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup | t_{RXS} | 10 | – | – | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold | t_{RXH} | 10 | – | – | ns | – |

5.3.7 100Base-TX MII Output Timing

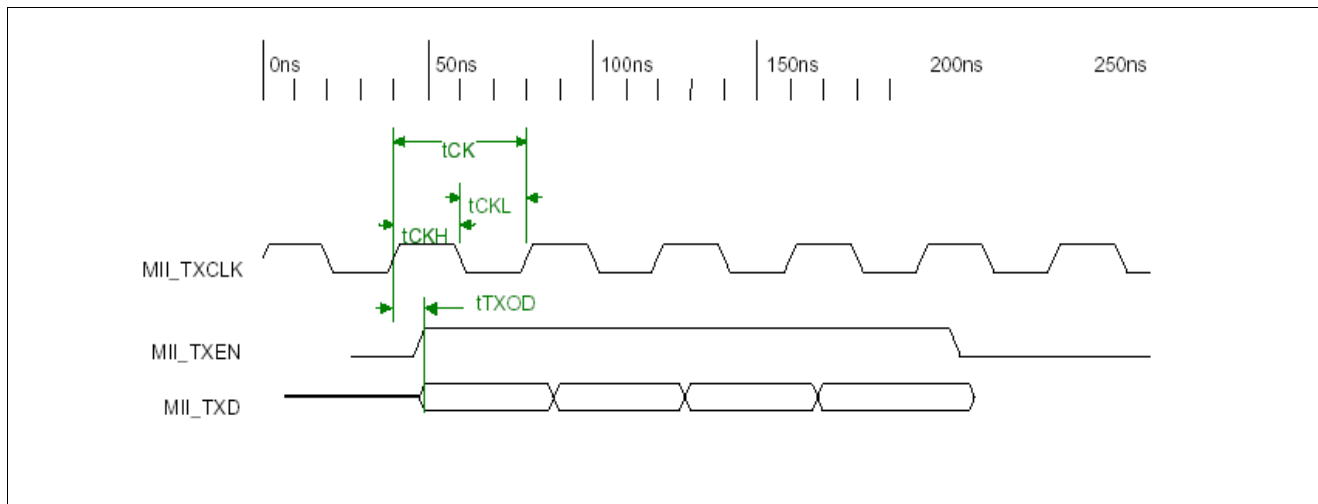


Figure 23 100Base-TX MII Output Timing

Table 85 100Base-TX MII Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MII_TXCLK Period | t_{CK} | – | 40 | – | ns | – |
| MII_TXCLK Low Period | t_{CKL} | 18 | – | 22 | ns | – |
| MII_TXCLK High Period | t_{CKH} | 18 | – | 22 | ns | – |
| MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay | t_{TXOD} | 0 | – | 25 | ns | – |

5.3.8 RMII REFCLK Input Timing

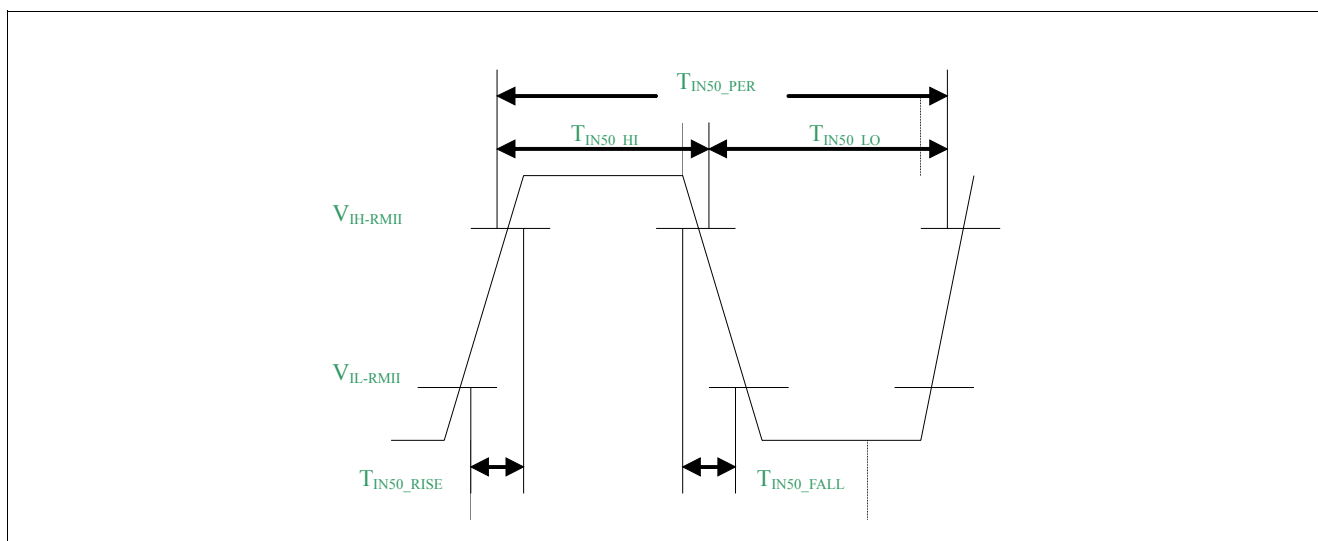


Figure 24 RMII REFCLK Input Timing

Table 86 RMII REFCLK Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|--------------|------|--------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| REFCLK Clock Period | t_{IN50_PER} | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | — |
| REFCLK Clock High | t_{IN50_HI} | 14 | 20.0 | — | ns | — |
| REFCLK Clock Low | t_{IN50_LO} | 14 | 20.0 | — | ns | — |
| REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.) | t_{IN50_RISE} | — | — | 2 | ns | — |
| REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max) | t_{IN50_FALL} | — | — | 2 | ns | — |

5.3.9 RMII REFCLK Output Timing

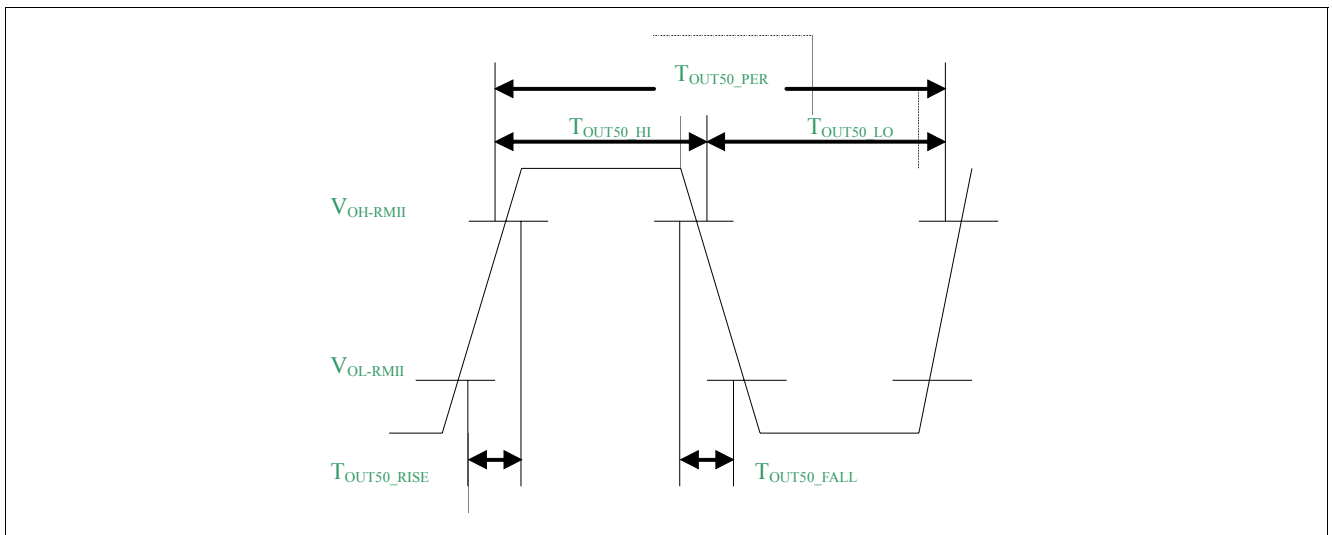


Figure 25 RMII REFCLK Output Timing

Table 87 RMII REFCLK Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-------------------|--------------|------|--------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| REFCLK Clock Period | t_{OUT50_PER} | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | — |
| REFCLK Clock High | t_{OUT50_HI} | 14 | 20.0 | 26 | ns | — |
| REFCLK Clock Low | t_{OUT50_LO} | 14 | 20.0 | 26 | ns | — |
| REFCLK Clock Rise Time, V_{OL} (max) to V_{OH} (min.) | t_{OUT50_RISE} | — | — | 2 | ns | — |
| REFCLK Clock Fall Time, V_{OH} (min.) to V_{OL} (max) | t_{OUT50_FALL} | — | — | 2 | ns | — |
| REFCLK Clock Jittering (p-p) | t_{OUT50_JIT} | — | 0.15 | — | ns | — |

5.3.10 Reduce MII Timing

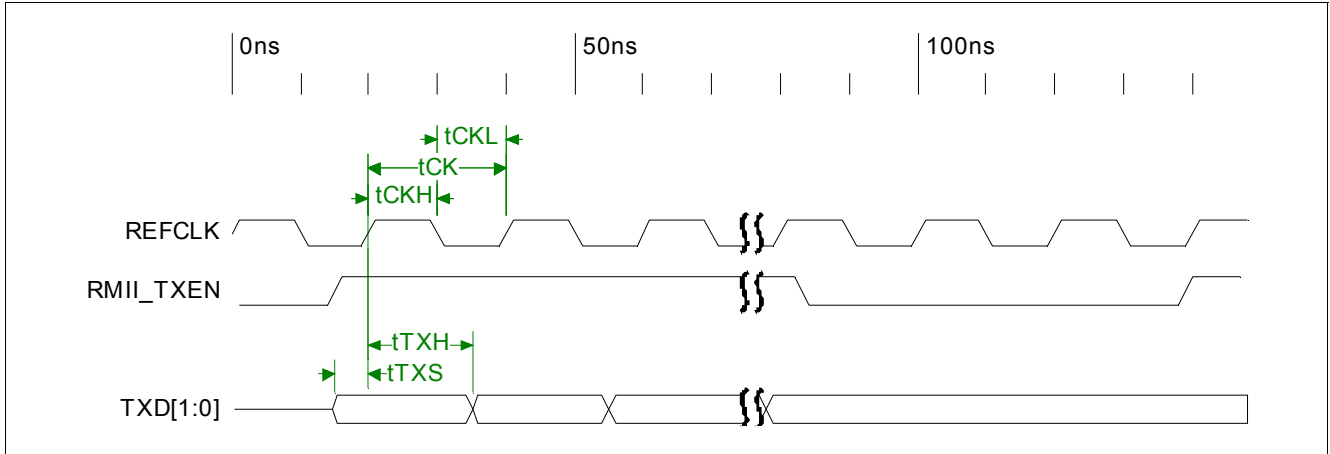


Figure 26 Reduce MII Timing (1 of 2)

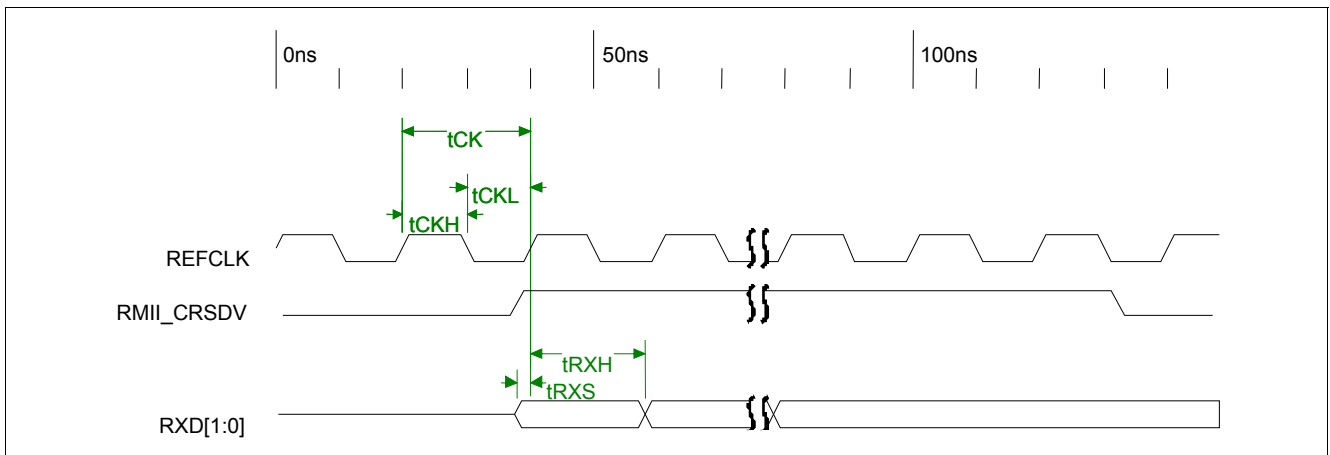


Figure 27 Reduce MII Timing (2 of 2)

Table 88 Reduce MII Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| RMII_REFCLK Period | t_{CK} | – | 20 | – | ns | – |
| RMII_REFCLK Low Period | t_{CKL} | – | 10 | – | ns | – |
| RMII_REFCLK High Period | t_{CKH} | – | 10 | – | ns | – |
| TXEN, TXD to REFCLK rising setup time | t_{TXS} | 4 | – | – | ns | – |
| TXE, TXD to REFCLK rising hold time | t_{TXH} | 2 | – | – | ns | – |
| CRSDV, RXD to REFCLK rising setup time | t_{RXS} | 4 | – | – | | – |
| CRSDV, RXD to REFCLK rising hold time | t_{RXH} | 2 | – | – | | – |

5.3.11 GPSI (7-wire) Input Timing

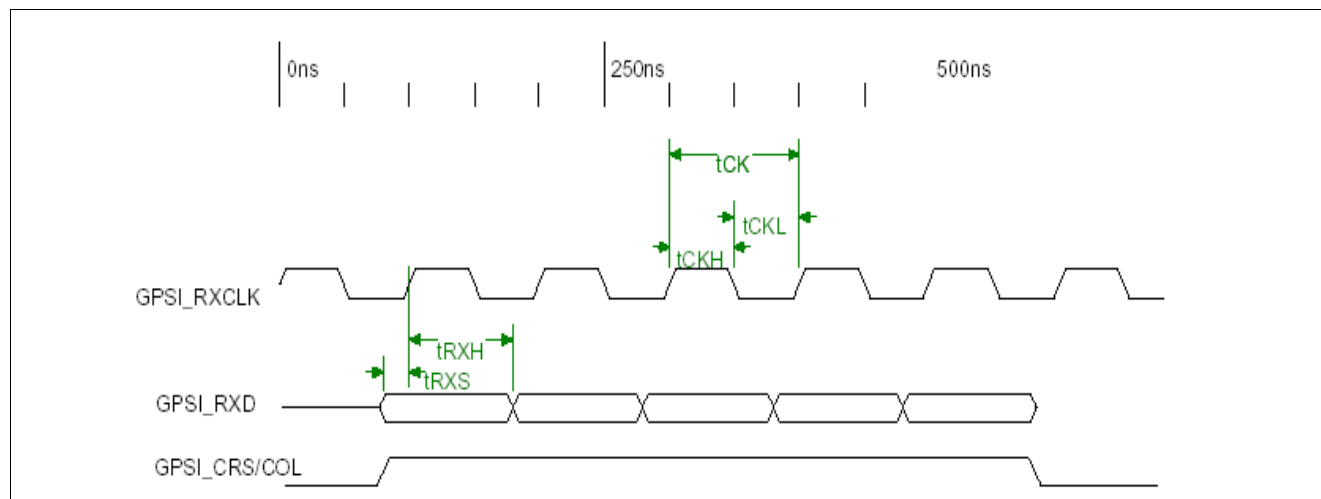


Figure 28 GPSI (7-wire) Input Timing

Table 89 GPSI (7-wire) Input Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| GPSI_RXCLK Period | t_{CK} | – | 100 | – | ns | – |
| GPSI_RXCLK Low Period | t_{CKL} | 40 | – | 60 | ns | – |
| GPSI_RXCLK High Period | t_{CKH} | 40 | – | 60 | ns | – |
| GPSI_RXD, GPSI_CRD/COL to GPSI_RXCLK Rising Setup Time | t_{RXS} | 10 | – | – | ns | – |
| GPSI_RXD, GPSI_CRD/COL to GPSI_RXCLK Rising HoldTime | t_{RXH} | 10 | – | – | ns | – |

5.3.12 GPSI (7-wire) Output Timing

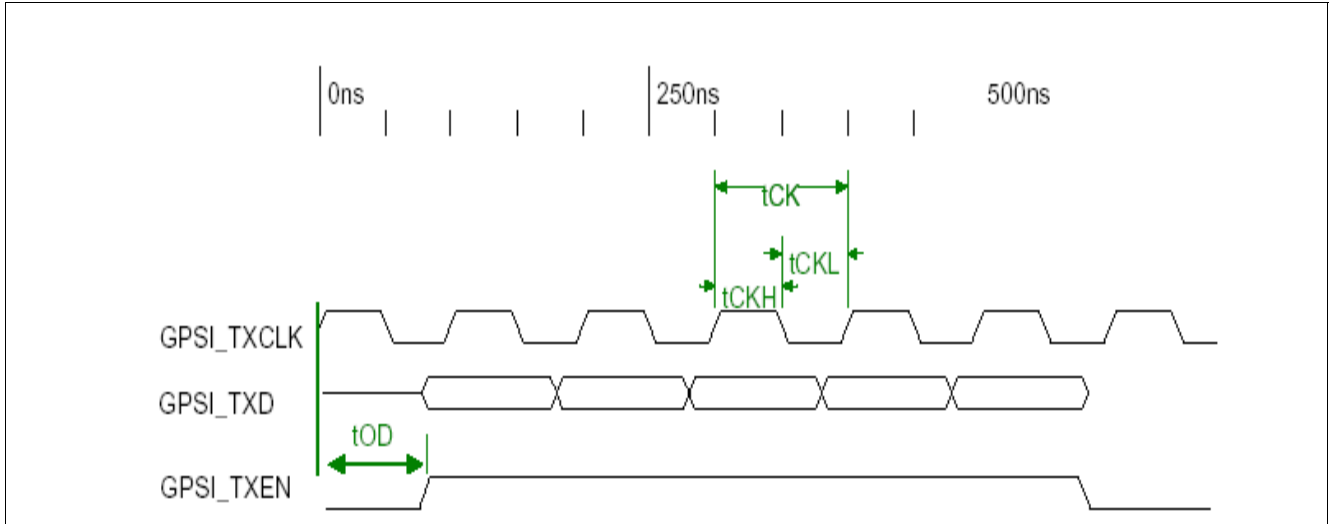


Figure 29 GPSI (7-wire) Output Timing

Table 90 GPSI (7-wire) Output Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| GPSI_TXCLK Period | t_{CK} | – | 100 | – | ns | – |
| GPSI_TXCLK Low Period | t_{CKL} | 40 | – | 60 | ns | – |
| GPSI_TXCLK High Period | t_{CKH} | 40 | – | 60 | ns | – |
| GPSI_TXCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay | t_{OD} | 50 | – | 70 | ns | – |

5.3.13 SDC/SDIO Timing

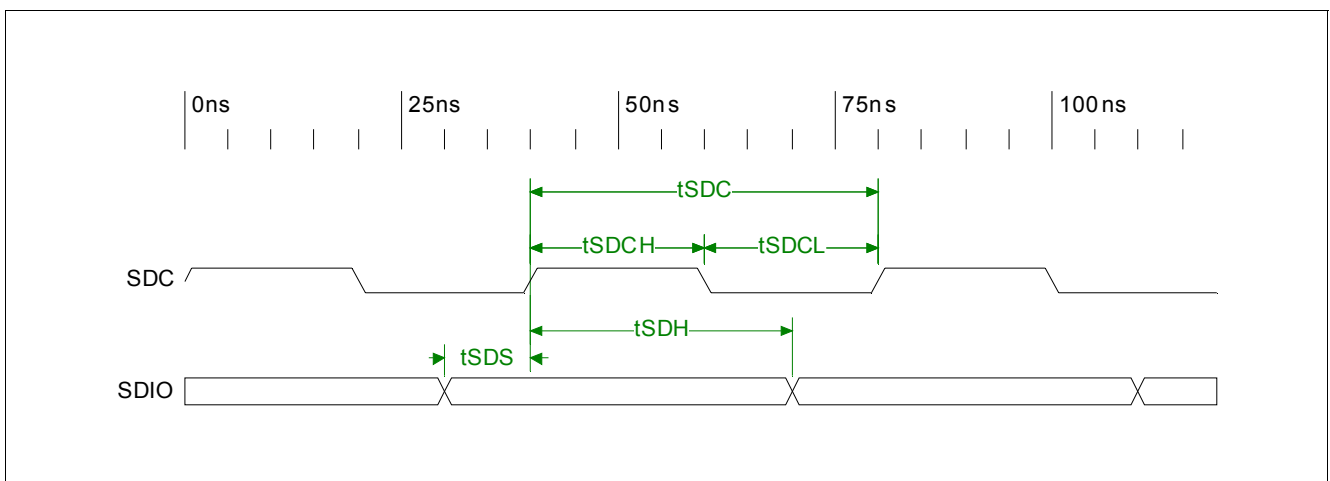


Figure 30 SDC/SDIO Timing

Table 91 SDC/SDIO Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SDC Period | t_{CK} | 20 | – | – | ns | – |
| SDC Low Period | t_{CKL} | 10 | – | – | ns | – |
| SDC High Period | t_{CKH} | 10 | – | – | ns | – |
| SDIO to SDC rising setup time on read/write cycle | t_{SDS} | 4 | – | – | ns | – |
| SDIO to SDC rising hold time on read/write cycle | t_{SDH} | 2 | – | – | ns | – |

6 Package Outlines

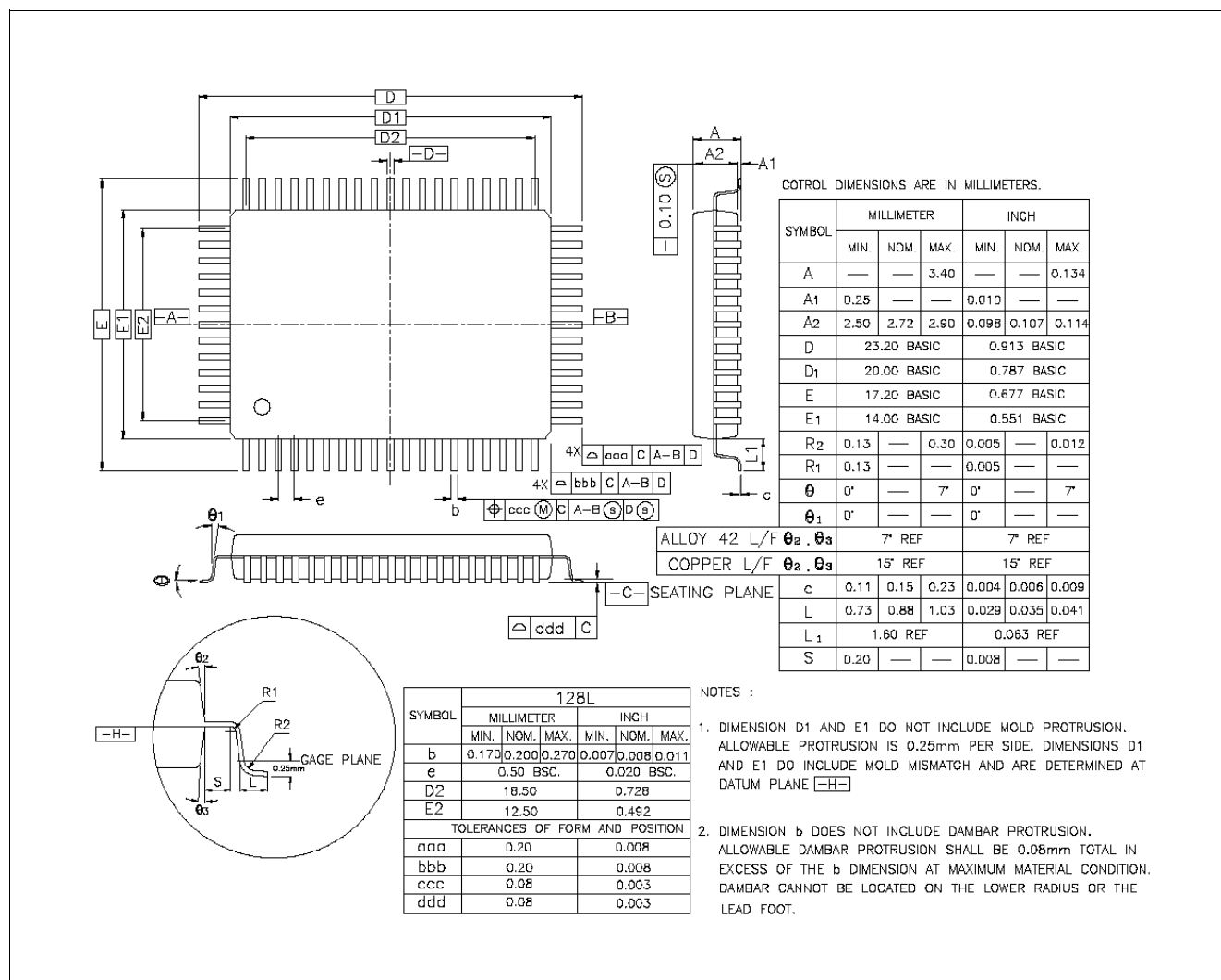


Figure 31 P-PQFP-128 Outside Dimension

6.1 Package Information

| Product Name | Product Type | Package |
|---|---|------------|
| 6-Port 10/100 Mbit/s Single Chip Ethernet Switch Controller | Samurai-6I/IX, ADM6996I/IX-AD-T-1, Version AD | P-PQFP-128 |

Terminology

B

BER Bit Error Rate

C

CFI Canonical Format Indicator

COL Collision

CRC Cyclic Redundancy Check

CRS Carrier Sense

CS Chip Select

D

DA Destination Address

DI Data Input

DO Data Output

E

EDI EEPROM Data Input

EDO EEPROM Data Output

EECS EEPROM Chip Select

EESK EEPROM Clock

ESD End of Stream Delimiter

F

FEFI Far End Fault Indication

FET Field Effect Transistor

FLP Fast Link Pulse

G

GND Ground

GPSI General Purpose Serial Interface

I

IPG Inter-Packet Gap

L

LF SR Linear Feedback Shift Register

M

MAC Media Access Controller

MDIX MDI Crossover

MII Media Independent Interface

N

NRZI Non Return to Zero Inverter

NRZ Non Return to Zero

P

PCS Physical Coding Sub-layer

PHY Physical Layer

PLL Phase Lock Loop

PMA Physical Medium Attachment

| | |
|----------|---|
| PMD | Physical Medium Dependent |
| Q | |
| QoS | Quality of Service |
| QFP | Quad Flat Package |
| R | |
| RST | Reset |
| RXCLK | Receive Clock |
| RXD | Receive Data |
| RXDV | Receive Data Valid |
| RXER | Receive Data Errors |
| RXN | Receive Negative (Analog receive differential signal) |
| RXP | Receive Positive (Analog receive differential signal) |
| S | |
| SA | Source Address |
| SOHO | Small Office Home Office |
| SSD | Start of Stream Delimiter |
| SQE | Signal Quality Error |
| T | |
| TOS | Type of Service |
| TP | Twisted Pair |
| TTL | Transistor Logic |
| TXCLK | Transmission Clock |
| TXD | Transmission Data |
| TXEN | Transmission Enable |
| TXN | Transmission Negative |
| TXP | Transmission Positive |

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