

74AC11

Triple 3-Input AND Gate

The AC11 contains three 3-input AND gates.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

74AC11

Triple 3-Input AND Gate

General Description

The AC11 contains three 3-input AND gates.

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA

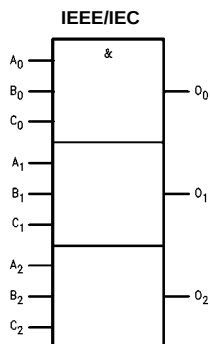
Ordering Code:

Order Number	Package Number	Package Description
74AC11SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC11SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC11MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC11MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC11PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

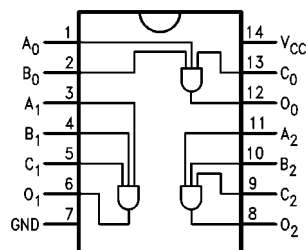
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n, C_n	Inputs
O_n	Outputs

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA I _{OH} = -24 mA I _{OH} = -24 mA (Note 3)	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 24 mA (Note 3)	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN} (Note 5)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 4)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V _{IN} = V _{CC} or GND	

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

AC Electrical Characteristics

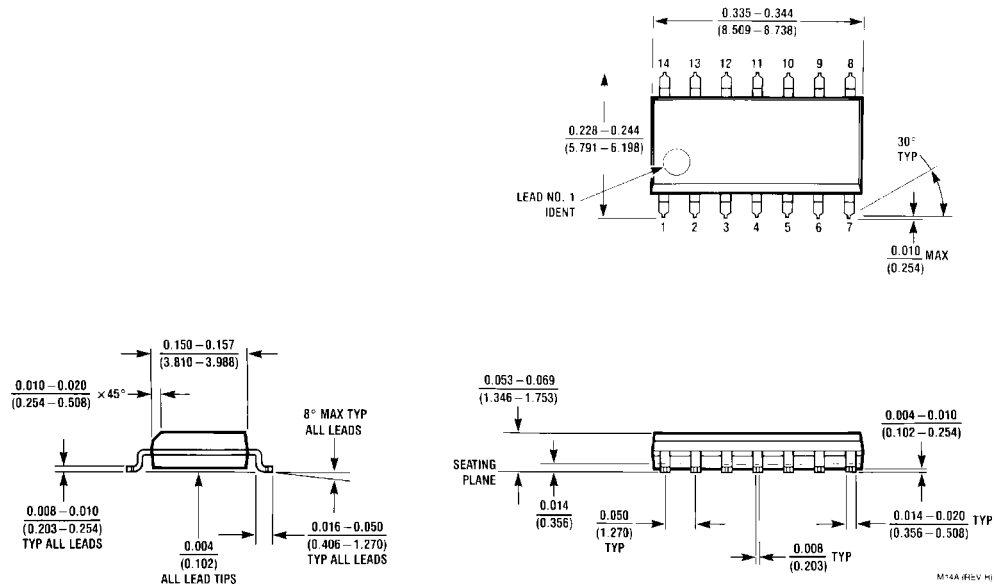
Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	1.5	5.5	9.5	1.0	10.0	ns
		5.0	1.5	4.0	8.0	1.0	8.5	
t _{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	9.5	ns
		5.0	1.5	4.0	7.0	1.0	7.5	

Note 6: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

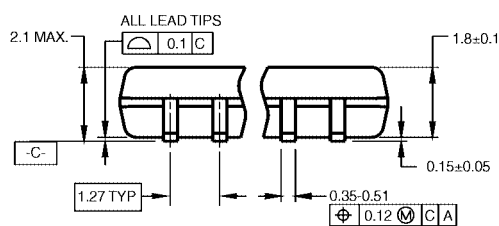
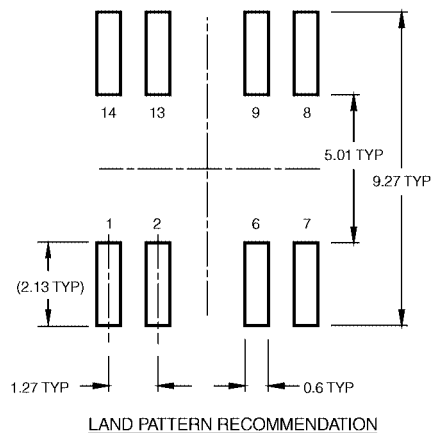
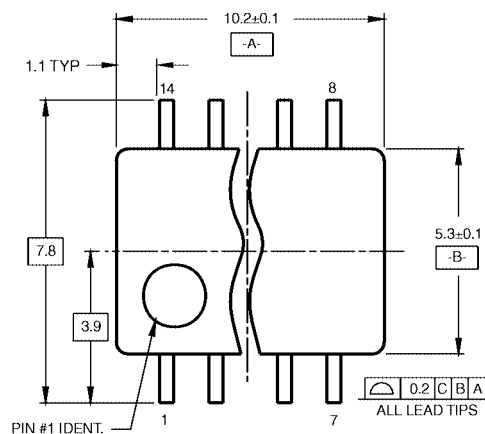
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	20.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

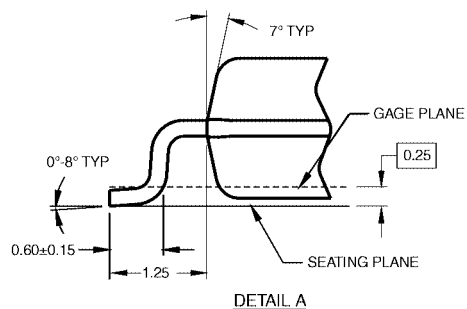
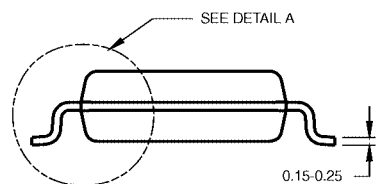


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

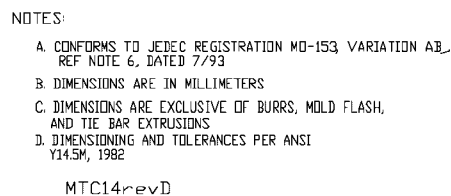


NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

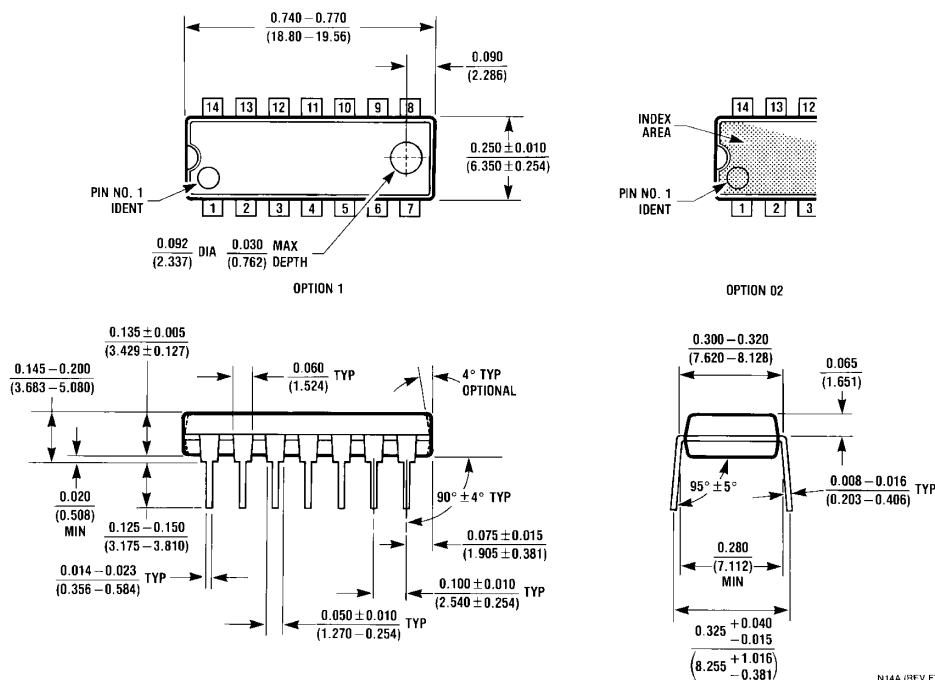
M14DRevB1

**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**



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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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