



# PCA9632

4-bit Fm+ I<sup>2</sup>C-bus low power LED driver

Rev. 5 — 27 July 2011

Product data sheet

## 1. General description

The PCA9632 is an I<sup>2</sup>C-bus controlled 4-bit LED driver optimized for Red/Green/Blue/Amber (RGBA) color mixing applications. The PCA9632 is a drop-in upgrade for the PCA9633 with 40× power reduction. In Individual brightness control mode, each LED output has its own 8-bit resolution (256 steps) fixed frequency Individual PWM controller that operates at 1.5625 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. In group dimming mode, each LED output has its own 6-bit resolution (64 steps) fixed frequency Individual PWM controller that operates at 6.25 kHz with a duty cycle that is adjustable from 0 % to 98.4 % to allow the LED to be set to a specific brightness value. A fifth 4-bit resolution (16 steps) Group PWM controller has a fixed frequency of 190 Hz that is used to dim all the LEDs with the same value.

While operating in the Blink mode, each LED output has its own 8-bit resolution (256 steps) fixed frequency Individual PWM controller that operates at 1.5625 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. Blink rate is controlled by the Group frequency setting that has 8-bit resolution (256 steps). The blink rate is adjustable between 24 Hz and once every 10.73 seconds. For Group frequency settings between 6 Hz and 24 Hz, the Group PWM has a 6-bit resolution (64 steps) with a duty cycle that is adjustable from 0 % to 98.4 %. For Group frequency settings between 6 Hz and 0.09 Hz (once in 10.73 seconds), the Group PWM has an 8-bit resolution (256 steps) with a duty cycle that is adjustable from 0 % to 99.6 %.

Each LED output can be off, on (no PWM control), set at its Individual PWM controller value or at both Individual and Group PWM controller values. The LED output driver is programmed to be either open-drain with a 25 mA current sink capability at 5 V or totem pole with a 25 mA sink, 10 mA source capability at 5 V. The PCA9632 operates with a supply voltage range of 2.3 V to 5.5 V and the outputs are 5.5 V tolerant. LEDs can be directly connected to the LED output (up to 25 mA, 5.5 V) or controlled with external drivers and a minimum amount of discrete components for larger current or higher voltage LEDs.

The PCA9632 is in the new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and more densely populated bus operation (up to 4000 pF).

Software programmable LED Group and three Sub Call I<sup>2</sup>C-bus addresses allow all or defined groups of PCA9632 devices to respond to a common I<sup>2</sup>C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I<sup>2</sup>C-bus commands.



The Software Reset (SWRST) Call allows the master to perform a reset of the PCA9632 through the I<sup>2</sup>C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set high-impedance. This allows an easy and quick way to reconfigure all device registers to the same condition.

## 2. Features and benefits

- 40× power reduction compared to PCA9633
- 4 LED drivers. Each output programmable at:
  - ◆ Off
  - ◆ On
  - ◆ Programmable LED brightness
  - ◆ Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus I<sup>2</sup>C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 1.5625 kHz PWM signal in Individual brightness mode
- 64-step (6-bit) linear programmable brightness for each LED output varying from fully off (default) to maximum brightness using a 6.25 kHz PWM signal in group dimming mode
- In group dimming mode, 16-step group brightness control allows global dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 1.5625 kHz PWM signal in group blinking mode
- 64-step group blinking with frequency programmable from 24 Hz to 6 Hz and duty cycle from 0 % to 98.4 %
- 256-step group blinking with frequency programmable from 6 Hz to 0.09 Hz (10.73 s) and duty cycle from 0 % to 99.6 %
- Four totem pole outputs (sink 25 mA and source 10 mA at 5 V) with software programmable open-drain LED outputs selection (default at high-impedance). No input function.
- 10-pin package option provides two hardware address pins allowing four devices to operate on the same bus
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Software Reset feature (SWRST Call) allows the device to be reset through the I<sup>2</sup>C-bus
- 400 kHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current of < 1 μA
- Operating power supply voltage range of 2.3 V to 5.5 V

- 5.5 V tolerant inputs
- -40 °C to +85 °C operation
- ESD protection exceeds 5000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, TSSOP10, HVSON8, HVSON10

### 3. Applications

- RGB or RGBA LED drivers for color mixing
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

### 4. Ordering information

Table 1. Ordering information

| Type number | Topside mark | Package |  | Version  |
|-------------|--------------|---------|--|----------|
|             |              | Name    | Description  |          |
| PCA9632DP1  | 9632         | TSSOP8  | plastic thin shrink small outline package; 8 leads; body width 3 mm                                    | SOT505-1 |
| PCA9632DP2  | 9632         | TSSOP10 | plastic thin shrink small outline package; 10 leads; body width 3 mm                                   | SOT552-1 |
| PCA9632TK   | 9632         | HVSON8  | plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm  | SOT908-1 |
| PCA9632TK2  | 9632         | HVSON10 | plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm | SOT650-1 |

### 5. Block diagram

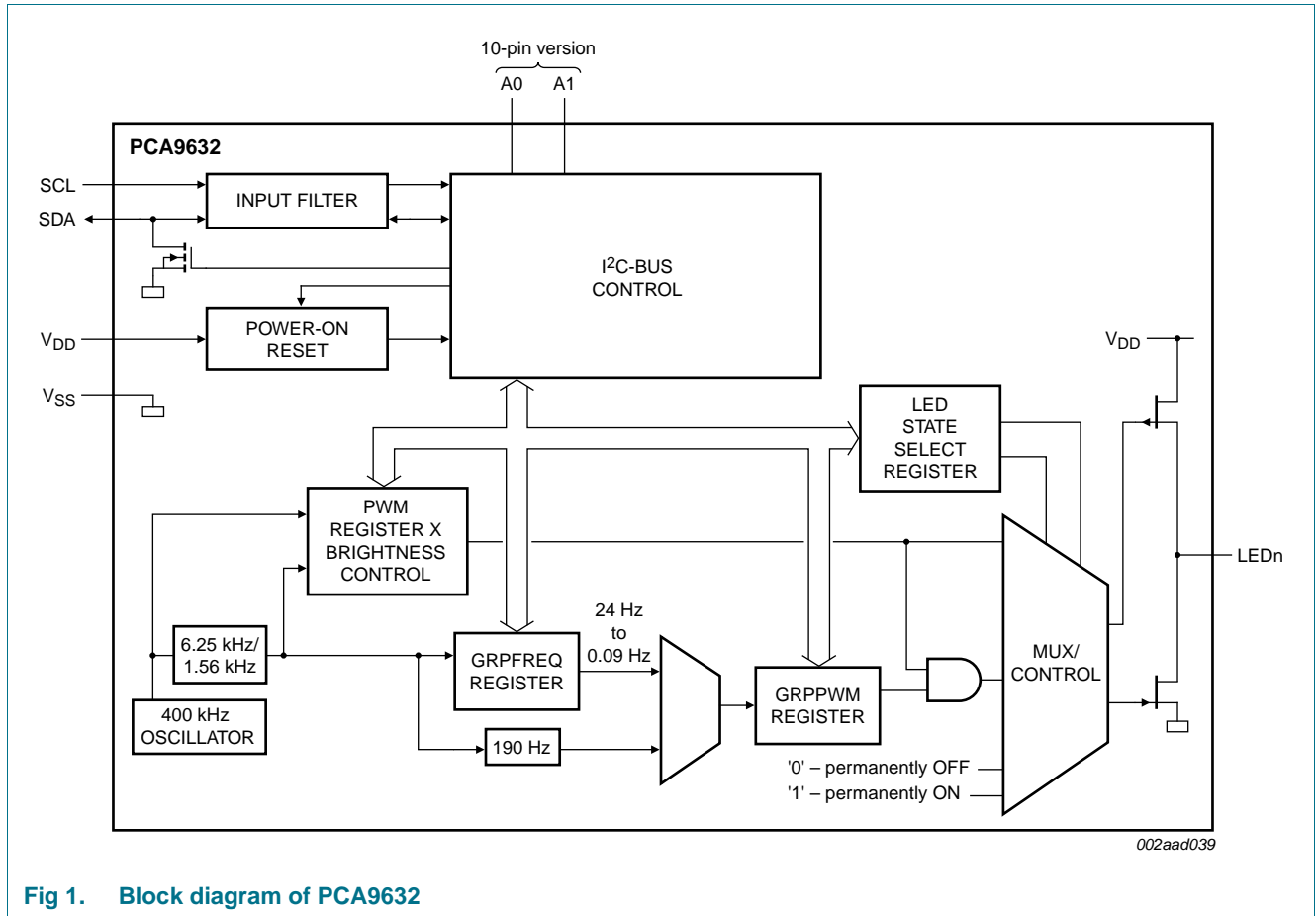
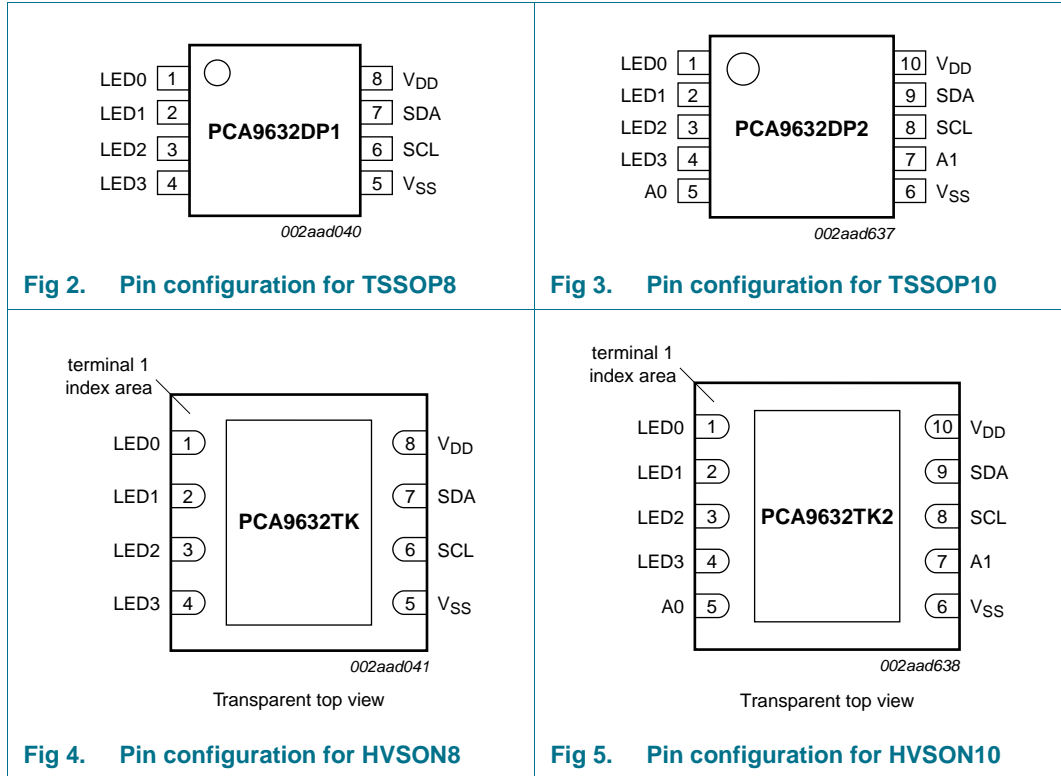


Fig 1. Block diagram of PCA9632

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description for TSSOP8 and HVSON8

| Symbol          | Pin              | Type         | Description       |
|-----------------|------------------|--------------|-------------------|
| LED0            | 1                | O            | LED driver 0      |
| LED1            | 2                | O            | LED driver 1      |
| LED2            | 3                | O            | LED driver 2      |
| LED3            | 4                | O            | LED driver 3      |
| V <sub>SS</sub> | 5 <sup>[1]</sup> | power supply | supply ground     |
| SCL             | 6                | I            | serial clock line |
| SDA             | 7                | I/O          | serial data line  |
| V <sub>DD</sub> | 8                | power supply | supply voltage    |

[1] HVSON8 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

**Table 3. Pin description for TSSOP10 and HVSON10**

| Symbol          | Pin              | Type         | Description       |
|-----------------|------------------|--------------|-------------------|
| LED0            | 1                | O            | LED driver 0      |
| LED1            | 2                | O            | LED driver 1      |
| LED2            | 3                | O            | LED driver 2      |
| LED3            | 4                | O            | LED driver 3      |
| A0              | 5                | I            | address input 0   |
| V <sub>SS</sub> | 6 <sup>[1]</sup> | power supply | supply ground     |
| A1              | 7                | I            | address input 1   |
| SCL             | 8                | I            | serial clock line |
| SDA             | 9                | I/O          | serial data line  |
| V <sub>DD</sub> | 10               | power supply | supply voltage    |

[1] HVSON10 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCA9632”](#).

### 7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

There are a maximum of 4 possible programmable addresses using the 2 hardware address pins for the 10-pin version and just one fixed address for the 8-pin version.

#### 7.1.1 Regular I<sup>2</sup>C-bus slave address

The I<sup>2</sup>C-bus slave address of the PCA9632 is shown in [Figure 6](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW (10-pin versions only).

**Remark:** Using reserved I<sup>2</sup>C-bus addresses will interfere with other devices, but only if the devices are on the bus and/or the bus will be open to other I<sup>2</sup>C-bus systems at some later date. In a closed system where the designer controls the address assignment these addresses can be used since the PCA9632 treats them like any other address. The LED All Call, Software Reset and PCA9564 or PCA9665 slave address (if on the bus) can never be used for individual device addresses.

- PCA9632 LED All Call address (1110 000) or Software Reset (0000 0110) which are active on start-up
- PCA9564 (0000 000) or PCA9665 (1110 000) slave address which is active on start-up
- ‘reserved for future use’ I<sup>2</sup>C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)

- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

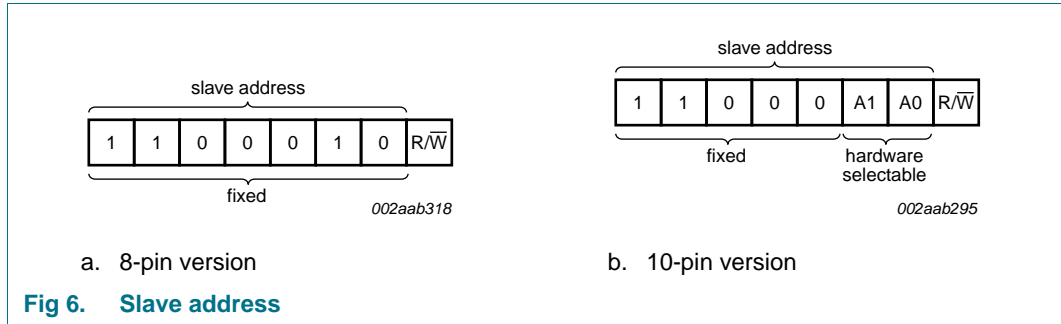


Fig 6. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

### 7.1.2 LED All Call I<sup>2</sup>C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I<sup>2</sup>C-bus (volatile programming)
- At power-up, LED All Call I<sup>2</sup>C-bus address is enabled. PCA9632 sends an ACK when E0h (R/W = 0) or E1h (R/W = 1) is sent by the master.

See [Section 7.3.8 “LED All Call I<sup>2</sup>C-bus address, ALLCALLADR”](#) for more detail.

**Remark:** The default LED All Call I<sup>2</sup>C-bus address (E0h or 1110 000) must not be used as a regular I<sup>2</sup>C-bus slave address since this address is enabled at power-up. All the PCA9632s on the I<sup>2</sup>C-bus will acknowledge the address if sent by the I<sup>2</sup>C-bus master.

### 7.1.3 LED Sub Call I<sup>2</sup>C-bus addresses

- 3 different I<sup>2</sup>C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001
  - SUBADR2 register: E4h or 1110 010
  - SUBADR3 register: E8h or 1110 100
- Programmable through I<sup>2</sup>C-bus (volatile programming)
- At power-up, Sub Call I<sup>2</sup>C-bus addresses are disabled. PCA9632 does not send an ACK when E2h (R/W = 0) or E3h (R/W = 1), E4h (R/W = 0) or E5h (R/W = 1), or E8h (R/W = 0) or E9h (R/W = 1) is sent by the master.

See [Section 7.3.7 “I<sup>2</sup>C-bus subaddress 1 to 3, SUBADR<sub>x</sub>”](#) for more detail.

**Remark:** The default LED Sub Call I<sup>2</sup>C-bus addresses may be used as regular I<sup>2</sup>C-bus slave addresses as long as they are disabled.

7.1.4 Software reset I<sup>2</sup>C-bus address

The address shown in [Figure 7](#) is used when a reset of the PCA9632 needs to be performed by the master. The Software Reset address (SWRST Call) must be used with  $R/\overline{W} = 0$ . If  $R/\overline{W} = 1$ , the PCA9632 does not acknowledge the SWRST. See [Section 7.5 “Software reset”](#) for more detail.

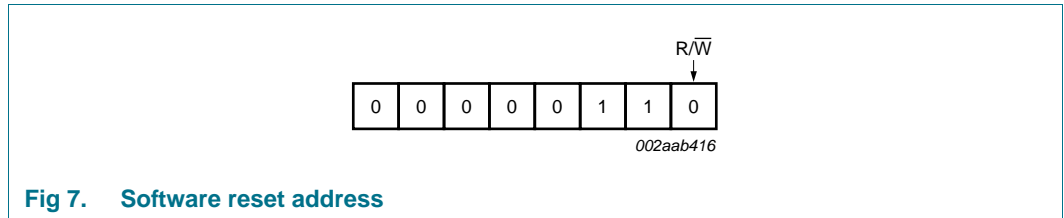


Fig 7. Software reset address

**Remark:** The Software Reset I<sup>2</sup>C-bus address is a reserved address and cannot be used as a regular I<sup>2</sup>C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9632, which will be stored in the Control register.

The lowest 4 bits are used as a pointer to determine which register will be accessed (D[3:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]). Bit 4 is unused and must be programmed with zero (0) for proper device operation.

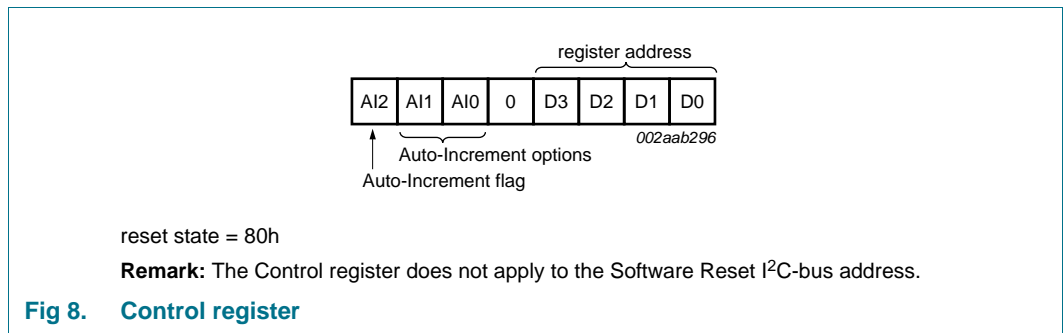


Fig 8. Control register

When the Auto-Increment flag is set (AI2 = 1), the four low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.



**Table 4. Auto-Increment options**

| AI2 | AI1 | AI0 | Function  |
|-----|-----|-----|---|
| 0   | 0   | 0   | no Auto-Increment   |
| 1   | 0   | 0   | Auto-Increment for all registers. D3, D2, D1, D0 roll over to '0000' after the last register (1100) is accessed.                                |
| 1   | 0   | 1   | Auto-Increment for Individual brightness registers only. D3, D2, D1, D0 roll over to '0010' after the last register (0101) is accessed.         |
| 1   | 1   | 0   | Auto-Increment for global control registers only. D3, D2, D1, D0 roll over to '0110' after the last register (0111) is accessed.                |
| 1   | 1   | 1   | Auto-Increment for individual and global control registers only. D3, D2, D1, D0 roll over to '0010' after the last register (0111) is accessed. |

**Remark:** Other combinations not shown in [Table 4](#) (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I<sup>2</sup>C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I<sup>2</sup>C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I<sup>2</sup>C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I<sup>2</sup>C-bus communication, for example, changing a color and global brightness at the same time.

Only the 4 least significant bits D[3:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[3:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0000 and 1100 (as defined in [Table 5](#)). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See [Table 4](#) for rollover values. For example, if the Control register = 1110 1000 (E8h), then the register addressing sequence will be (in hex):

08 → ... → 0C → 00 → ... → 07 → 02 → ... → 07 → 02 → ... → 07 → 02 → ... as long as the master keeps sending or reading data.

### 7.3 Register definitions

**Table 5. Register summary**

Only D[3:0] = 0000 to 1100 are allowed and will be acknowledged. D[3:0] = 1101, 1110, or 1111 are reserved and will not be acknowledged.

When writing to the Control register, bit 4 must be programmed with logic 0 for proper device operation.

| Register number (hex) | D3 | D2 | D1 | D0 | Name       | Type       | Function                                  |
|-----------------------|----|----|----|----|------------|------------|---|
| 00h                   | 0  | 0  | 0  | 0  | MODE1      | read/write | Mode register 1                           |
| 01h                   | 0  | 0  | 0  | 1  | MODE2      | read/write | Mode register 2                           |
| 02h                   | 0  | 0  | 1  | 0  | PWM0       | read/write | brightness control LED0                   |
| 03h                   | 0  | 0  | 1  | 1  | PWM1       | read/write | brightness control LED1                   |
| 04h                   | 0  | 1  | 0  | 0  | PWM2       | read/write | brightness control LED2                   |
| 05h                   | 0  | 1  | 0  | 1  | PWM3       | read/write | brightness control LED3                   |
| 06h                   | 0  | 1  | 1  | 0  | GRPPWM     | read/write | group duty cycle control                  |
| 07h                   | 0  | 1  | 1  | 1  | GRPFREQ    | read/write | group frequency                           |
| 08h                   | 1  | 0  | 0  | 0  | LEDOUT     | read/write | LED output state                          |
| 09h                   | 1  | 0  | 0  | 1  | SUBADR1    | read/write | I <sup>2</sup> C-bus subaddress 1         |
| 0Ah                   | 1  | 0  | 1  | 0  | SUBADR2    | read/write | I <sup>2</sup> C-bus subaddress 2         |
| 0Bh                   | 1  | 0  | 1  | 1  | SUBADR3    | read/write | I <sup>2</sup> C-bus subaddress 3         |
| 0Ch                   | 1  | 1  | 0  | 0  | ALLCALLADR | read/write | LED All Call I <sup>2</sup> C-bus address |

### 7.3.1 Mode register 1, MODE1

**Table 6. MODE1 - Mode register 1 (address 00h) bit description**

Legend: \* default value.

| Bit | Symbol  | Access    | Value | Description  |
|-----|---------|-----------|-------|--|
| 7   | AI2     | read only | 0     | Register Auto-Increment disabled                                       |
|     |         |           | 1*    | Register Auto-Increment enabled  |
| 6   | AI1     | read only | 0*    | Auto-Increment bit 1 = 0   |
|     |         |           | 1     | Auto-Increment bit 1 = 1   |
| 5   | AI0     | read only | 0*    | Auto-Increment bit 0 = 0   |
|     |         |           | 1     | Auto-Increment bit 0 = 1   |
| 4   | SLEEP   | R/W       | 0     | Normal mode <sup>[1]</sup> .   |
|     |         |           | 1*    | Low power mode. Oscillator off <sup>[2]</sup> .                        |
| 3   | SUB1    | R/W       | 0*    | PCA9632 does not respond to I <sup>2</sup> C-bus subaddress 1.         |
|     |         |           | 1     | PCA9632 responds to I <sup>2</sup> C-bus subaddress 1.                 |
| 2   | SUB2    | R/W       | 0*    | PCA9632 does not respond to I <sup>2</sup> C-bus subaddress 2.         |
|     |         |           | 1     | PCA9632 responds to I <sup>2</sup> C-bus subaddress 2.                 |
| 1   | SUB3    | R/W       | 0*    | PCA9632 does not respond to I <sup>2</sup> C-bus subaddress 3.         |
|     |         |           | 1     | PCA9632 responds to I <sup>2</sup> C-bus subaddress 3.                 |
| 0   | ALLCALL | R/W       | 0     | PCA9632 does not respond to LED All Call I <sup>2</sup> C-bus address. |
|     |         |           | 1*    | PCA9632 responds to LED All Call I <sup>2</sup> C-bus address.         |

[1] It takes 500  $\mu$ s max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500  $\mu$ s window.

[2] When the oscillator is off (Sleep mode), the LED outputs cannot be turned on, off or dimmed/blinked.

### 7.3.2 Mode register 2, MODE2

**Table 7. MODE2 - Mode register 2 (address 01h) bit description**

Legend: \* default value.

| Bit    | Symbol                | Access    | Value | Description   |
|--------|-----------------------|-----------|-------|---|
| 7      | -                     | read only | 0*    | reserved  |
| 6      | -                     | read only | 0*    | reserved  |
| 5      | DMBLNK                | R/W       | 0*    | Group control = dimming   |
|        |                       |           | 1     | Group control = blinking  |
| 4      | INVRT <sup>[1]</sup>  | R/W       | 0*    | Output logic state not inverted. Value to use when no external driver used. |
|        |                       |           | 1     | Output logic state inverted. Value to use when external driver used.        |
| 3      | OCH                   | R/W       | 0*    | Outputs change on STOP command <sup>[2]</sup>                               |
|        |                       |           | 1     | Outputs change on ACK.  |
| 2      | OUTDRV <sup>[1]</sup> | R/W       | 0*    | The 4 LED outputs are configured with an open-drain structure.              |
|        |                       |           | 1     | The 4 LED outputs are configured with a totem pole structure.               |
| 1 to 0 | OUTNE[1:0]            | R/W       | 01*   | unused  |

[1] See [Section 7.6 "Using the PCA9632 with and without external drivers"](#) for more details. Normal LEDs can be driven directly in either mode. Some newer LEDs include integrated Zener diodes to limit voltage transients, reduce EMI, protect the LEDs, and these must be driven only in the open-drain mode to prevent overheating the IC.

[2] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9632. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.

7.3.3 PWM registers 0 to 3, PWMx — Individual brightness control registers

**Table 8. PWM0 to PWM3 - PWM registers 0 to 3 (address 02h to 05h) bit description**  
 Legend: \* default value.

| Address | Register | Bit | Symbol    | Access | Value      | Description                |
|---------|----------|-----|-----------|--------|------------|----------------------------|
| 02h     | PWM0     | 7:0 | IDC0[7:0] | R/W    | 0000 0000* | PWM0 Individual Duty Cycle |
| 03h     | PWM1     | 7:0 | IDC1[7:0] | R/W    | 0000 0000* | PWM1 Individual Duty Cycle |
| 04h     | PWM2     | 7:0 | IDC2[7:0] | R/W    | 0000 0000* | PWM2 Individual Duty Cycle |
| 05h     | PWM3     | 7:0 | IDC3[7:0] | R/W    | 0000 0000* | PWM3 Individual Duty Cycle |

While operating in Individual brightness mode (LDRx = 10), a 1.5625 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). In this mode, all the 8 bits are used.

$$duty\ cycle = \frac{IDC_x[7:0]}{256} \tag{1}$$

E.g., if IDCx[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

While operating in group dimming mode, a 6.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 64 linear steps from 00h (0 % duty cycle = LED output off) to 3Fh (98.4 % duty cycle = LED output at maximum brightness). In this mode only the 6 MSBs are used (IDCx[7:2]). The 2 LSBs IDCx[1:0] are ignored. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

$$duty\ cycle = \frac{IDC_x[7:2],00}{256} \tag{2}$$

E.g., if IDCx[7:2] = 111111, then duty cycle = 1111 1100 / 256 = 252 / 256 = 98.4 %.

While operating in blink mode, a 1.5625 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). In this mode, all the 8 bits are used.

$$duty\ cycle = \frac{IDC_x[7:0]}{256} \tag{3}$$

E.g., if IDCx[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

7.3.4 Group duty cycle control, GRPPWM

**Table 9. GRPPWM - Group duty cycle control register (address 06h) bit description**  
 Legend: \* default value.

| Address | Register | Bit | Symbol   | Access | Value     | Description     |
|---------|----------|-----|----------|--------|-----------|-----------------|
| 06h     | GRPPWM   | 7:0 | GDC[7:0] | R/W    | 1111 1111 | GRPPWM register |

When DMBLNK bit (MODE2 register) is programmed with 0, a 190 Hz fixed frequency signal is superimposed with the 6.25 kHz Individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'don't care'.

In the group dimming mode (DMBLNK = 0) global brightness for the 4 outputs is controlled through 16 linear steps from 00h (0 % duty cycle = LED output off) to F0h (93.75 % duty cycle = maximum brightness). In this mode only the 4 MSBs of the GRPPWM[7:4] are used. Bits GRPPWM[3:0] are unused.

$$duty\ cycle = \frac{GDC[7:4],0000}{256} \tag{4}$$

E.g., if GDC[7:4] = 1111, then duty cycle = 1111 0000 / 256 = 240 / 256 = 93.75 %.

When DMBLNK bit is programmed with 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

In this mode, when GRPFREQ is programmed to provide a blinking with frequency programmable from 24 Hz to 6 Hz, GRPPWM[7:2] is used to provide 64-step duty cycle resolution from 0 % to 98.4 %. GRPPWM[1:0] bits are unused.

$$duty\ cycle = \frac{GDC[7:2],00}{256} \tag{5}$$

E.g., if GDC[7:2] = 111111, then duty cycle = 1111 1100 / 256 = 252 / 256 = 98.4 %.

When GRPFREQ is programmed to provide a blinking with frequency programmable from 6 Hz to 0.09 Hz (10.73 s), GRPPWM[7:0] is used to provide a 256-step duty cycle resolution from 0 % to 99.6 %. In this case, all the 8 bits of the GRPPWM register are used.

$$duty\ cycle = \frac{GDC[7:0]}{256} \tag{6}$$

E.g., if GDC[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

### 7.3.5 Group frequency, GRPFREQ

**Table 10. GRPFREQ - Group frequency register (address 07h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol    | Access | Value      | Description      |
|---------|----------|-----|-----------|--------|------------|------------------|
| 07h     | GRPFREQ  | 7:0 | GFRQ[7:0] | R/W    | 0000 0000* | GRPFREQ register |

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to logic 1. Value in this register is a 'don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 seconds).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{24} \text{ (in seconds)} \tag{7}$$

### 7.3.6 LED driver output state, LEDOUT

**Table 11. LEDOUT - LED driver output state register (address 08h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol | Access | Value | Description               |
|---------|----------|-----|--------|--------|-------|---------------------------|
| 08h     | LEDOUT   | 7:6 | LDR3   | R/W    | 00*   | LED3 output state control |
|         |          | 5:4 | LDR2   | R/W    | 00*   | LED2 output state control |
|         |          | 3:2 | LDR1   | R/W    | 00*   | LED1 output state control |
|         |          | 1:0 | LDR0   | R/W    | 00*   | LED0 output state control |

**LDRx = 00** — LED driver x is off (default power-up state).

**LDRx = 01** — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

**LDRx = 10** — LED driver x individual brightness can be controlled through its PWMx register.

**LDRx = 11** — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

### 7.3.7 I<sup>2</sup>C-bus subaddress 1 to 3, SUBADRx

**Table 12. SUBADR1 to SUBADR3 - I<sup>2</sup>C-bus subaddress registers 0 to 3 (address 09h to 0Bh) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol  | Access | Value     | Description                       |
|---------|----------|-----|---------|--------|-----------|-----------------------------------|
| 09h     | SUBADR1  | 7:1 | A1[7:1] | R/W    | 1110 001* | I <sup>2</sup> C-bus subaddress 1 |
|         |          | 0   | A1[0]   | R only | 0*        | reserved                          |
| 0Ah     | SUBADR2  | 7:1 | A2[7:1] | R/W    | 1110 010* | I <sup>2</sup> C-bus subaddress 2 |
|         |          | 0   | A2[0]   | R only | 0*        | reserved                          |
| 0Bh     | SUBADR3  | 7:1 | A3[7:1] | R/W    | 1110 100* | I <sup>2</sup> C-bus subaddress 3 |
|         |          | 0   | A3[0]   | R only | 0*        | reserved                          |

Subaddresses are programmable through the I<sup>2</sup>C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to logic 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I<sup>2</sup>C-bus subaddress are valid. The LSB in SUBADR<sub>x</sub> register is a read-only bit (0).

When SUBx is set to 1, the corresponding I<sup>2</sup>C-bus subaddress can be used during either an I<sup>2</sup>C-bus read or write sequence.

### 7.3.8 LED All Call I<sup>2</sup>C-bus address, ALLCALLADR

**Table 13. ALLCALLADR - LED All Call I<sup>2</sup>C-bus address register (address 0Ch) bit description**

Legend: \* default value.

| Address | Register   | Bit | Symbol  | Access | Value     | Description                                   |
|---------|------------|-----|---------|--------|-----------|---|
| 0Ch     | ALLCALLADR | 7:1 | AC[7:1] | R/W    | 1110 000* | ALLCALL I <sup>2</sup> C-bus address register |
|         |            | 0   | AC[0]   | R only | 0*        | reserved                                      |

The LED All Call I<sup>2</sup>C-bus address allows all the PCA9632s in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, power-up default state). This address is programmable through the I<sup>2</sup>C-bus and can be used during either an I<sup>2</sup>C-bus read or write sequence. The register address can be programmed as a sub call.

Only the 7 MSBs representing the All Call I<sup>2</sup>C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

### 7.4 Power-on reset

When power is applied to V<sub>DD</sub>, an internal power-on reset holds the PCA9632 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9632 registers and I<sup>2</sup>C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.

### 7.5 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved SWRST I<sup>2</sup>C-bus address '0000 011' with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The PCA9632 device(s) acknowledge(s) after seeing the SWRST Call address '0000 0110' (06h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.

4. Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
  - a. Byte 1 = A5h: the PCA9632 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9632 does not acknowledge it.
  - b. Byte 2 = 5Ah: the PCA9632 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9632 does not acknowledge it.

If more than 2 bytes of data are sent, the PCA9632 does not acknowledge any more.
5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the PCA9632 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t<sub>BUF</sub>).

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the PCA9632 (at any time) as a 'SWRST Call Abort'. The PCA9632 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

### 7.6 Using the PCA9632 with and without external drivers

The PCA9632 LED output drivers are 5.5 V only tolerant and can sink up to 25 mA at 5 V.

If the device needs to drive LEDs to a higher voltage and/or higher current, use of an external driver is required.

- INVRT bit (MODE2 register) can be used to keep the LED PWM control firmware the same (PWMx and GRPPWM values directly calculated from their respective formulas and the LED output state determined by LEDOUT register value) independently of the type of external driver.
- OUTDRV bit (MODE2 register) allows minimizing the amount of external components required to control the external driver (N-type or P-type device).

**Table 14. Use of INVRT and OUTDRV based on connection to the LEDn outputs**

| INVRT | OUTDRV | Direct connection to LEDn                                 |                                       | External N-type driver                                    |                             | External P-type driver                                    |                             |
|-------|--------|---|---------------------------------------|---|-----------------------------|---|-----------------------------|
|       |        | Firmware  | External pull-up resistor             | Firmware  | External pull-up resistor   | Firmware  | External pull-up resistor   |
| 0     | 0      | formulas and LED output state values apply <sup>[1]</sup> | LED current limiting R <sup>[1]</sup> | formulas and LED output state values inverted             | required                    | formulas and LED output state values apply                | required                    |
| 0     | 1      | formulas and LED output state values apply <sup>[1]</sup> | LED current limiting R <sup>[1]</sup> | formulas and LED output state values inverted             | not required                | formulas and LED output state values apply <sup>[3]</sup> | not required <sup>[3]</sup> |
| 1     | 0      | formulas and LED output state values inverted             | LED current limiting R                | formulas and LED output state values apply                | required                    | formulas and LED output state values inverted             | required                    |
| 1     | 1      | formulas and LED output state values inverted             | LED current limiting R                | formulas and LED output state values apply <sup>[2]</sup> | not required <sup>[2]</sup> | formulas and LED output state values inverted             | not required                |

[1] Correct configuration when LEDs directly connected to the LEDn outputs (connection to V<sub>DD</sub> through current limiting resistor).

[2] Optimum configuration when external N-type (NPN, NMOS) driver used.

[3] Optimum configuration when external P-type (PNP, PMOS) driver used.



Table 15. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits

| LEDOUT  | INVRT | OUTDRV | Upper transistor (V <sub>DD</sub> to LEDn) | Lower transistor (LEDn to V <sub>SS</sub> ) | LEDn state   |
|---|-------|--------|--|---|--|
| 00  | 0     | 0      | off  | off   | high-Z <sup>[1]</sup>  |
| LED driver off                                      | 0     | 1      | on   | off   | V <sub>DD</sub>  |
|   | 1     | 0      | off  | on  | V <sub>SS</sub>  |
|   | 1     | 1      | off  | on  | V <sub>SS</sub>  |
| 01  | 0     | 0      | off  | on  | V <sub>SS</sub>  |
| LED driver on                                       | 0     | 1      | off  | on  | V <sub>SS</sub>  |
|   | 1     | 0      | off  | off   | high-Z <sup>[1]</sup>  |
|   | 1     | 1      | on   | off   | V <sub>DD</sub>  |
| 10<br>Individual<br>brightness<br>control           | 0     | 0      | off  | Individual PWM (non-inverted)               | V <sub>SS</sub> or high-Z <sup>[1]</sup> = PWMx value                        |
|   | 0     | 1      | Individual PWM (non-inverted)              | Individual PWM (non-inverted)               | V <sub>SS</sub> or V <sub>DD</sub> = PWMx value                              |
|   | 1     | 0      | off  | Individual PWM (inverted)                   | high-Z <sup>[1]</sup> or V <sub>SS</sub> = 1 – PWMx value                    |
|   | 1     | 1      | Individual PWM (inverted)                  | Individual PWM (inverted)                   | V <sub>DD</sub> or V <sub>SS</sub> = 1 – PWMx value                          |
| 11<br>Individual +<br>group<br>dimming/<br>blinking | 0     | 0      | off  | Individual + Group PWM (non-inverted)       | V <sub>SS</sub> or high-Z <sup>[1]</sup> = PWMx/GRPPWM values                |
|   | 0     | 1      | Individual PWM (non-inverted)              | Individual PWM (non-inverted)               | V <sub>SS</sub> or V <sub>DD</sub> = PWMx/GRPPWM values                      |
|   | 1     | 0      | off  | Individual + Group PWM (inverted)           | high-Z <sup>[1]</sup> or V <sub>SS</sub> = (1 – PWMx) or (1 – GRPPWM) values |
|   | 1     | 1      | Individual PWM (inverted)                  | Individual PWM (inverted)                   | V <sub>DD</sub> or V <sub>SS</sub> = (1 – PWMx) or (1 – GRPPWM) values       |

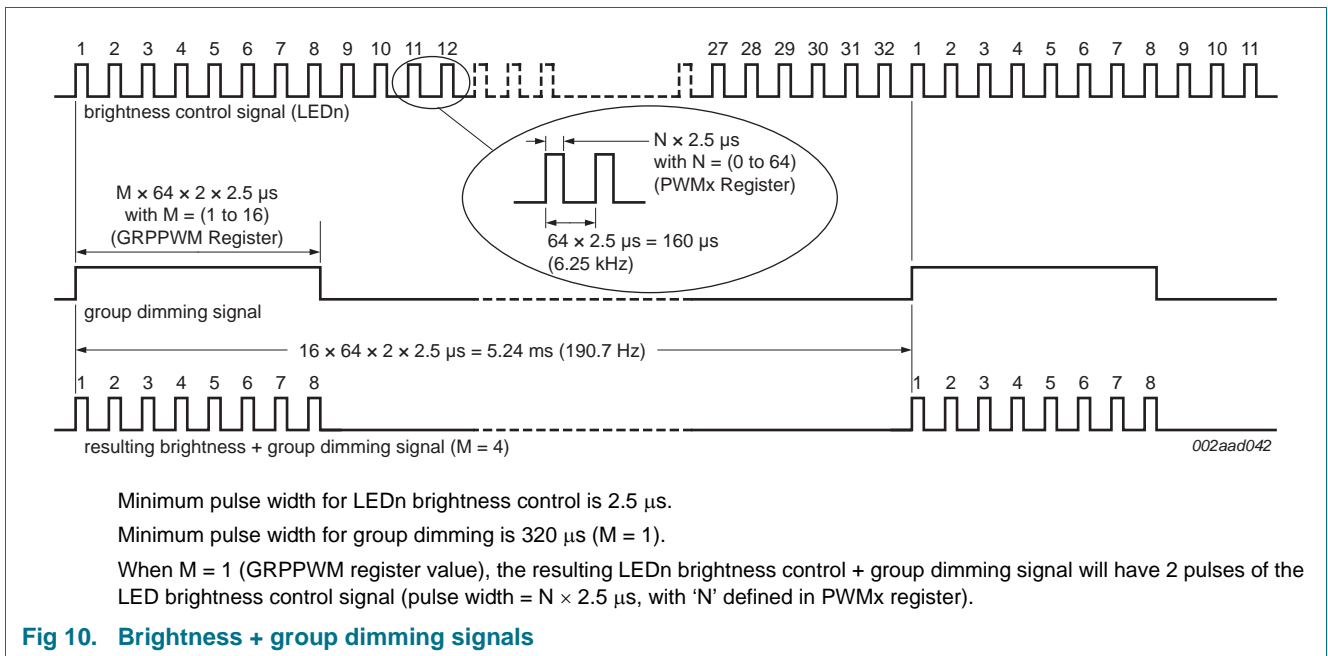
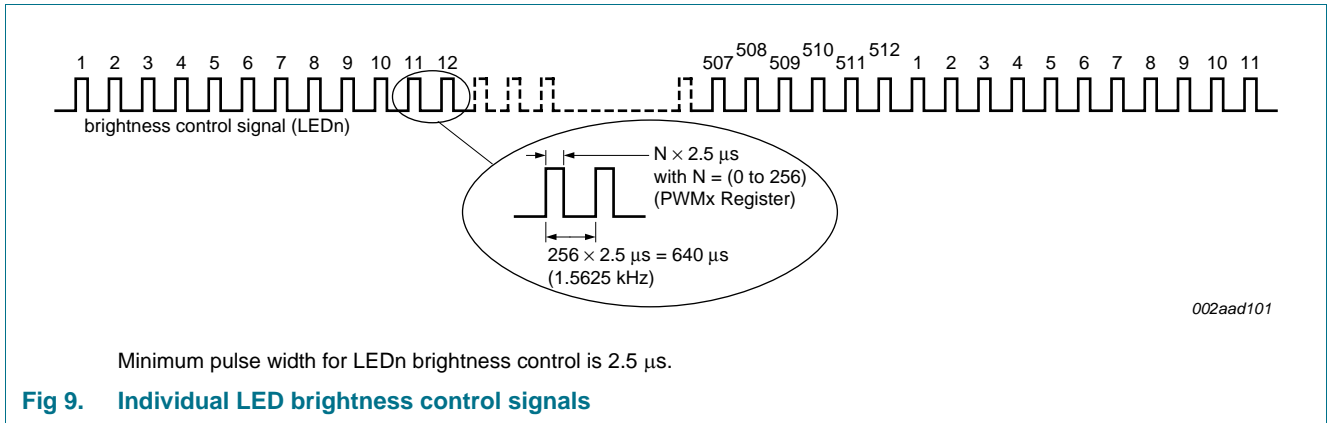
[1] External pull-up or LED current limiting resistor connects LEDn to V<sub>DD</sub>.

## 7.7 Individual brightness control with group dimming/blinking

A 1.5625 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (4 bits, 16 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 Hz (8 bits, 256 steps) with programmable duty cycle (6 bits, 64 steps) is used to provide a global blinking control for (24 Hz to 6 Hz) and (8 bits, 256 steps) for (6 Hz to 1/10.73 Hz).



**Table 16. Dimming and blinking resolution**

| Type of control                               | LDRx | DMBLNK | GRPPWM    | GRPFREQ   | Frequency  | PWMx      |
|---|------|--------|-----------|-----------|--|-----------|
| Individual LED brightness without dimming     | 10   | X      | X         | X         | 1.5625 kHz   | 256 steps |
| Individual LED brightness with global dimming | 11   | 0      | 16 steps  | X         | 190 Hz with 6.25 kHz modulation                                  | 64 steps  |
| Blinking (fast)                               | 11   | 1      | 64 steps  | 256 steps | blink frequency = 6 Hz to 24 Hz<br>PWMx frequency = 1.5625 kHz   | 256 steps |
| Blinking (slow)                               | 11   | 1      | 256 steps | 256 steps | blink frequency = 0.09 Hz to 6 Hz<br>PWMx frequency = 1.5625 kHz | 256 steps |

## 8. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 11](#)).

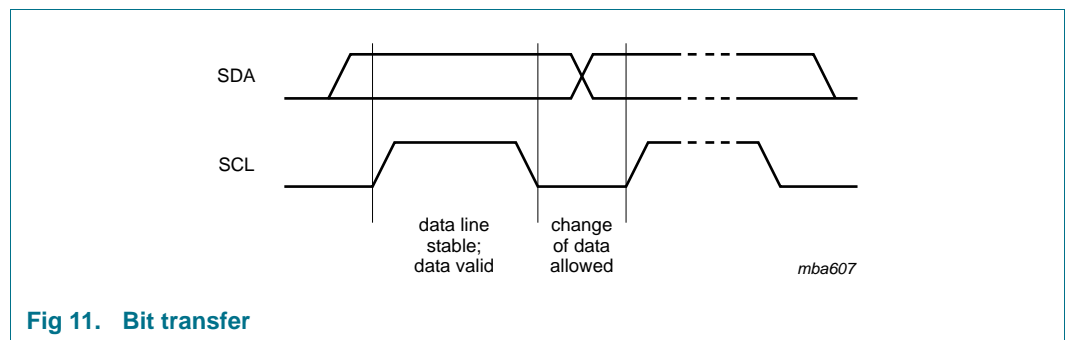


Fig 11. Bit transfer

#### 8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 12](#)).

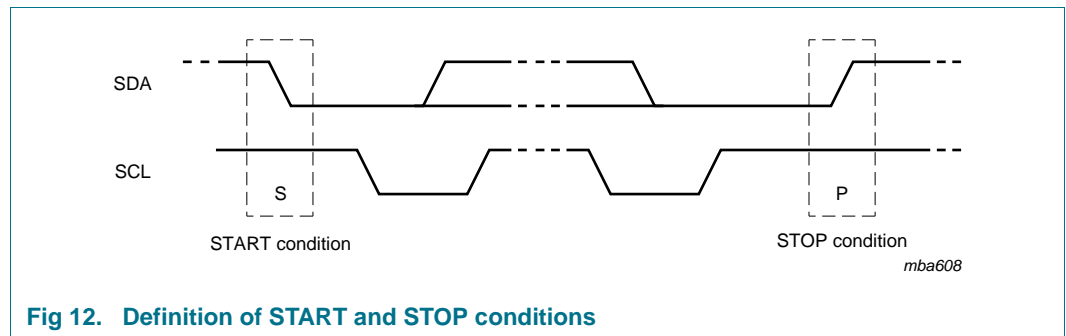


Fig 12. Definition of START and STOP conditions

### 8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 13](#)).

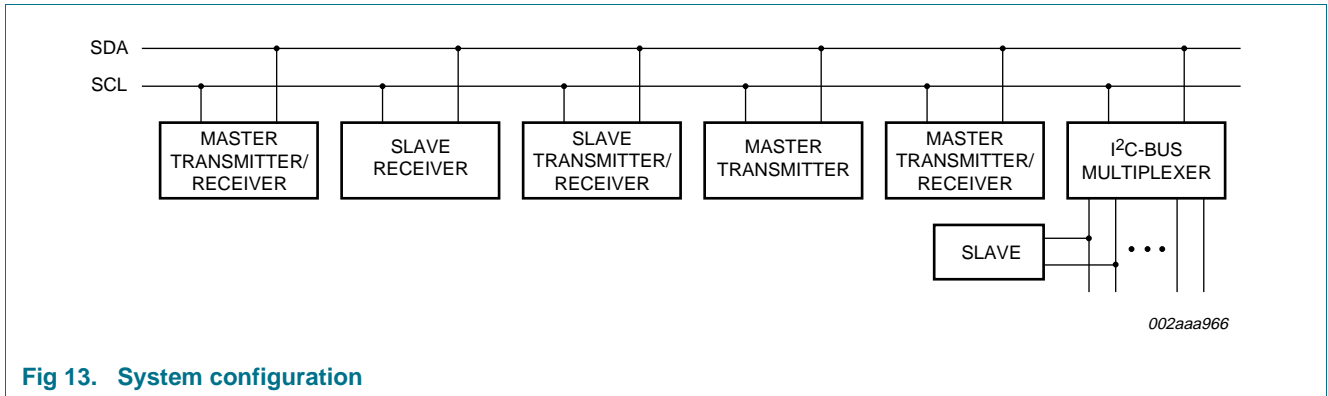


Fig 13. System configuration

### 8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

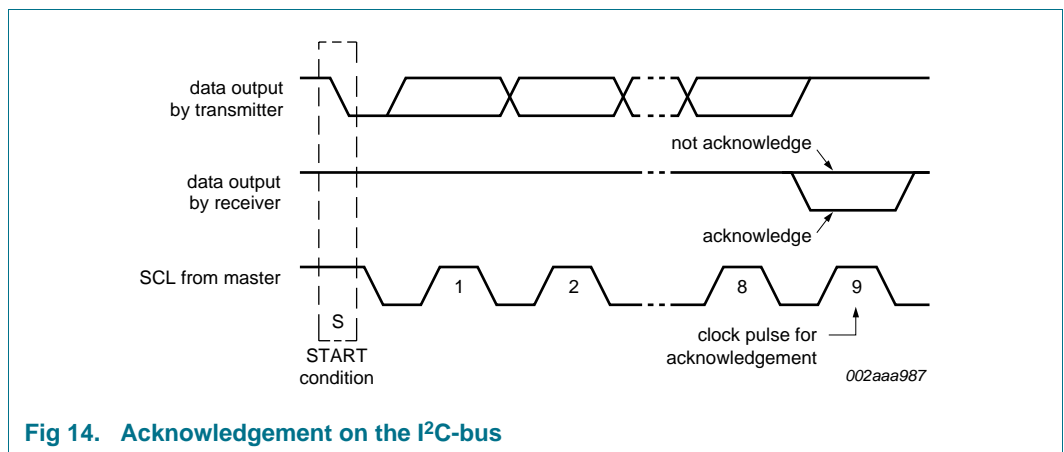
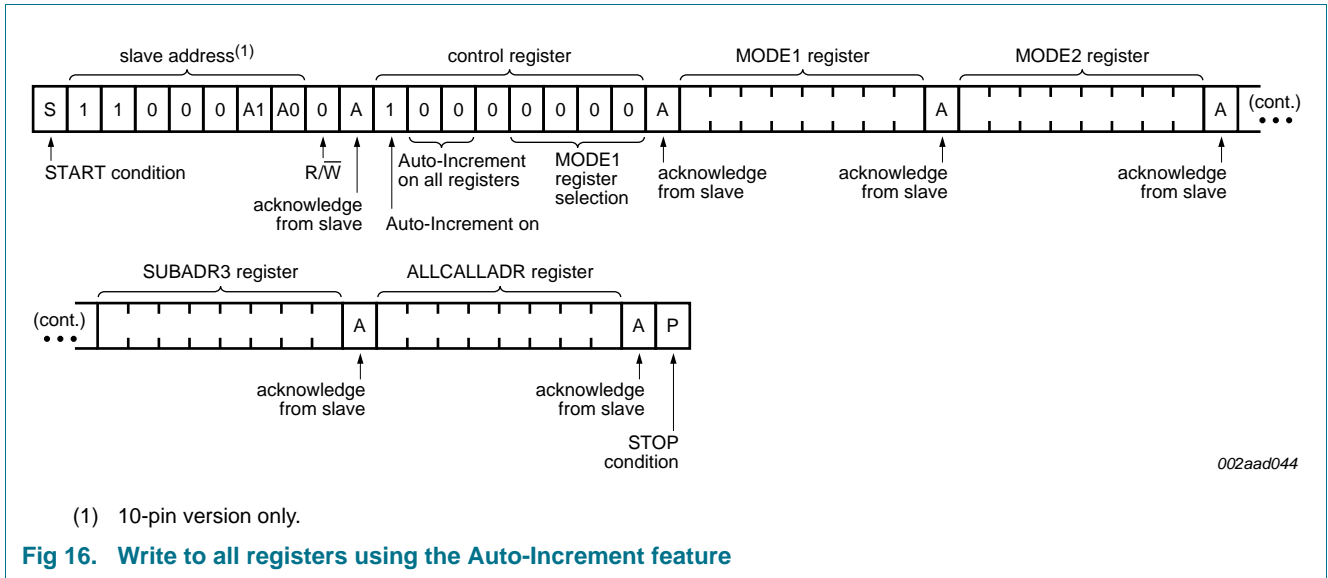
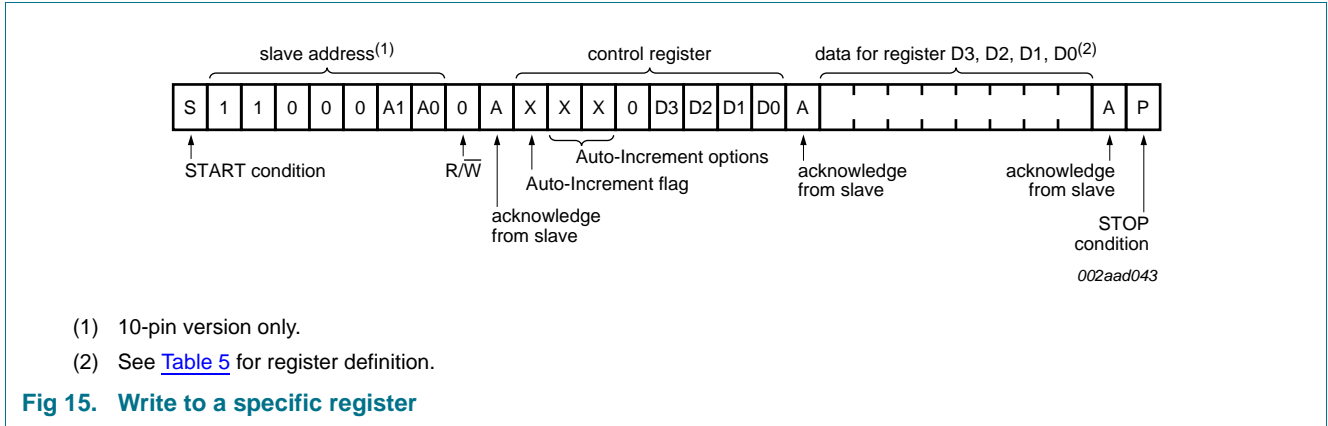
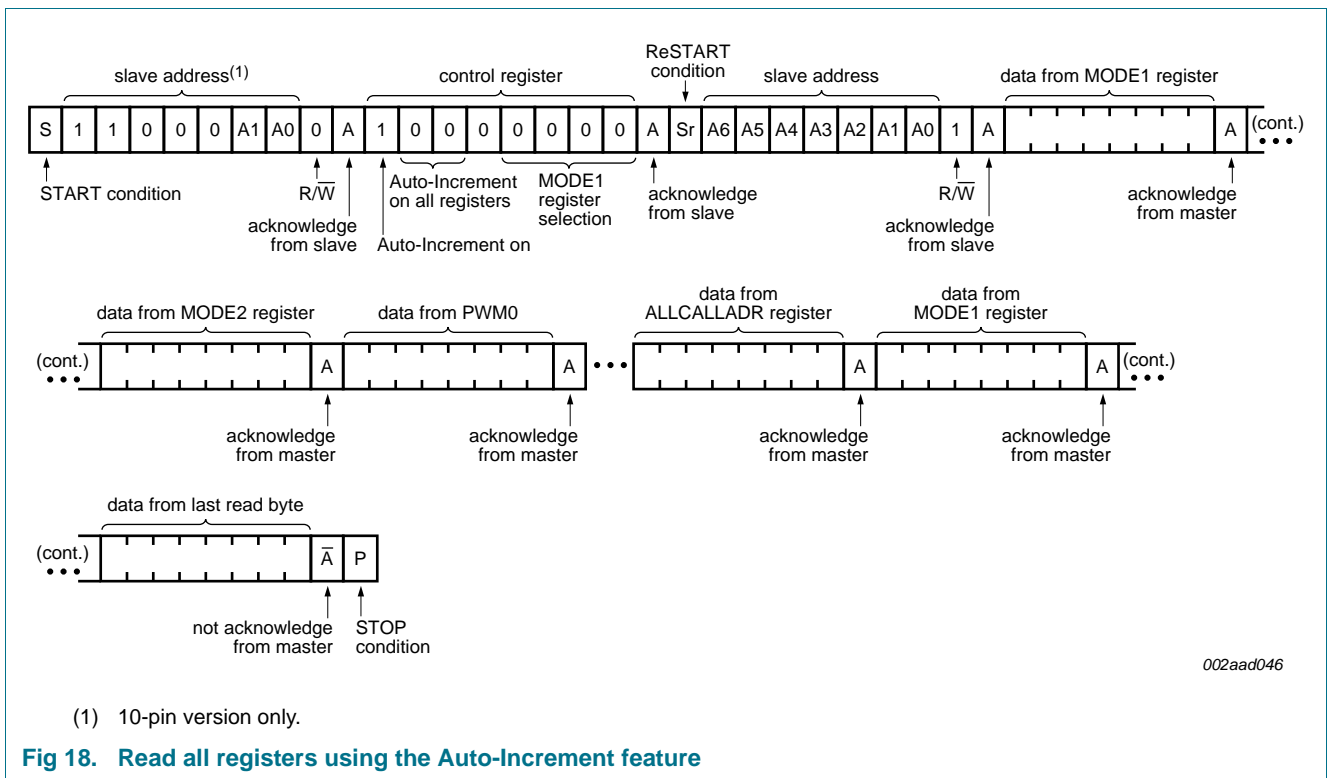
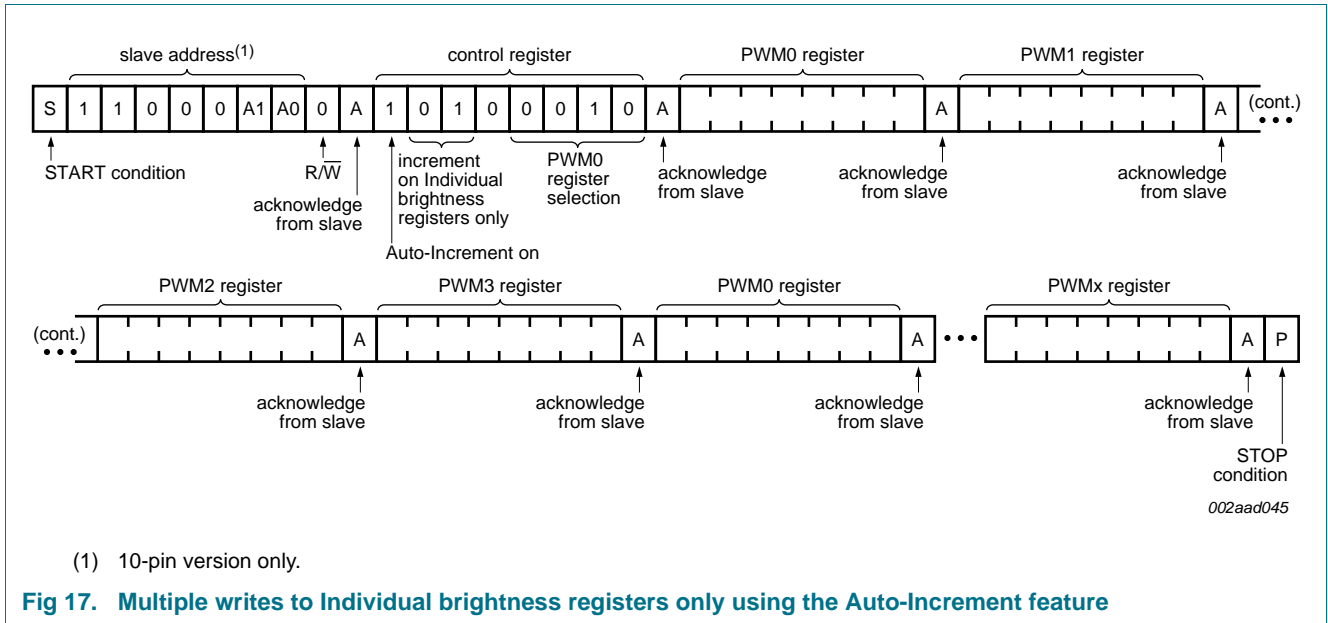
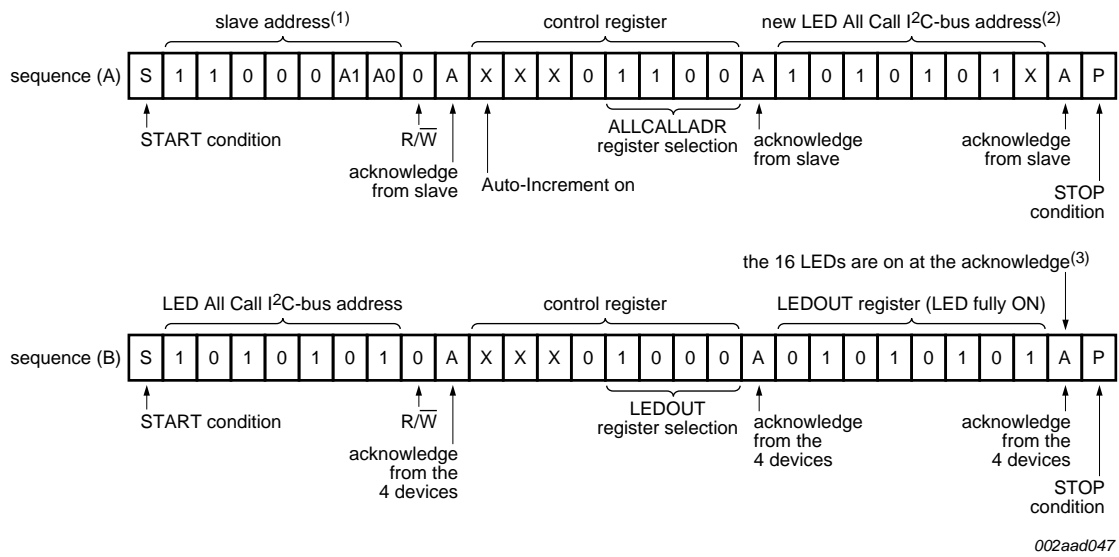


Fig 14. Acknowledgement on the I<sup>2</sup>C-bus

### 9. Bus transactions







- (1) 10-pin version is used for this figure. Four PCA9632DP2 or PCA9632TK2 and same sequence (A) (above) is sent to each of them. A[1:0] = 00 to 11.
- (2) ALLCALL bit in MODE1 register is equal to logic 1 for this example.
- (3) OCH bit in MODE2 register is equal to logic 1 for this example.

Fig 19. LED All Call I<sup>2</sup>C-bus address programming and LED All Call sequence example

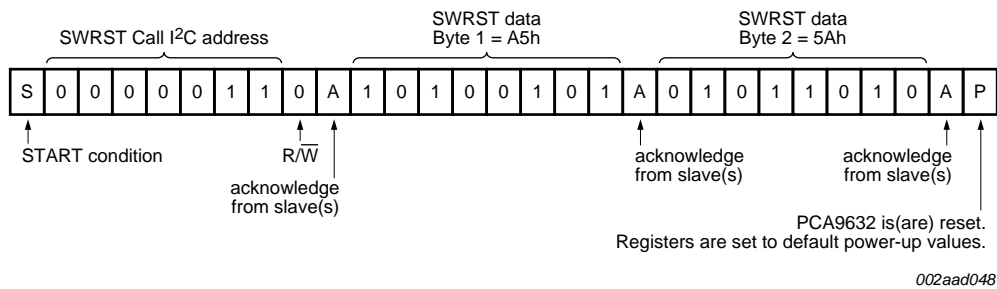
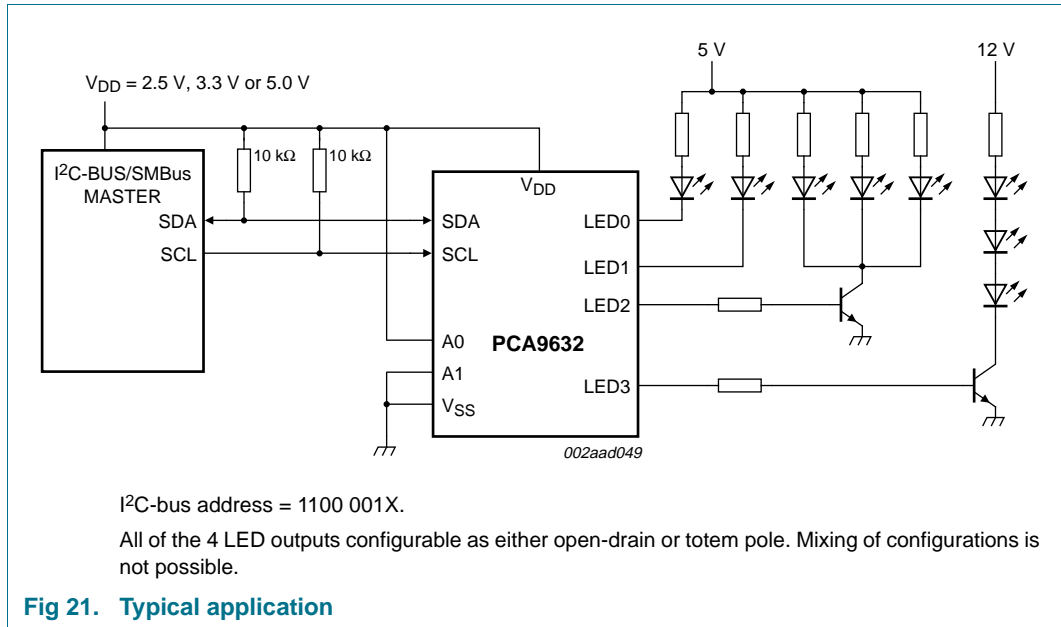


Fig 20. Software Reset (SWRST) Call sequence

10. Application design-in information



**Question 1:** What kind of edge rate control is there on the outputs?

- The typical edge rates depend on the output configuration, supply voltage, and the applied load. The outputs can be configured as either open-drain NMOS or totem pole outputs. If the customer is using the part to directly drive LEDs, they should be using it in an open-drain NMOS, if they are concerned about the maximum I<sub>SS</sub> and ground bounce. The edge rate control was designed primarily to slow down the turn-on of the output device; it turns off rather quickly (~ 1.5 ns). In simulation, the typical turn-on time for the open-drain NMOS was ~ 14 ns (V<sub>DD</sub> = 3.6 V; C<sub>L</sub> = 50 pF; R<sub>PU</sub> = 500 Ω).

**Question 2:** Is ground bounce possible?

- Ground bounce is a possibility, especially if all 16 outputs transition at full current (25 mA each). There is a fair amount of decoupling capacitance on chip (~ 50 pF), which is intended to suppress some of the ground bounce. The customer will need to determine if additional decoupling capacitance externally placed as close as physically possible to the device is required.

**Question 3:** Can I really sink 400 mA through the single ground pin on the package and will this cause any ground bounce problem due to the PWM of the LEDs?

- Yes, you can sink 400 mA through a single ground pin on the **package**. Although the package only has one ground pin, there are two ground pads on the die itself connected to this one pin. Although some ground bounce is likely, it will not disrupt the operation of the part and would be reduced by the external decoupling capacitance.

**Question 4:** I can't turn the LEDs on or off, but their registers are set properly. Why?

- Check the Mode register 1 bit 4 (MODE1[4]) SLEEP setting. The value needs to be a logic 0 so that the OSC is turned on. If the OSC is turned off, the LEDs cannot be turned on or off and also can't be dimmed or blinked.



**Question 5:** I'm using LEDs with integrated Zener diodes and the IC is getting very hot. Why?

- The IC outputs can be set to either open-drain or push-pull and default to push-pull outputs. In this application with the Zener diodes, they need to be set to open-drain since in the push-pull architecture there is a low resistance path to ground through the Zener and this is causing the IC to overheat. The PCA9632/33/34/35 ICs all power-up in the push-pull output mode and with the logic state HIGH, so one of the first things that need to be done is to set the outputs to open-drain.

## 11. Limiting values

**Table 17. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol               | Parameter                      | Conditions | Min                   | Max  | Unit |
|----------------------|--------------------------------|------------|-----------------------|------|------|
| V <sub>DD</sub>      | supply voltage                 |            | -0.5                  | +6.0 | V    |
| V <sub>I/O</sub>     | voltage on an input/output pin |            | V <sub>SS</sub> - 0.5 | 5.5  | V    |
| I <sub>O(LEDn)</sub> | output current on pin LEDn     |            | -                     | 25   | mA   |
| I <sub>SS</sub>      | ground supply current          |            | -                     | 100  | mA   |
| P <sub>tot</sub>     | total power dissipation        |            | -                     | 400  | mW   |
| T <sub>stg</sub>     | storage temperature            |            | -65                   | +150 | °C   |
| T <sub>amb</sub>     | ambient temperature            | operating  | -40                   | +85  | °C   |

## 12. Static characteristics

**Table 18. Static characteristics**

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

| Symbol                             | Parameter                      | Conditions  | Min          | Typ   | Max           | Unit          |             |
|------------------------------------|--------------------------------|---|--------------|-------|---------------|---------------|-------------|
| <b>Supply</b>                      |                                |   |              |       |               |               |             |
| $V_{DD}$                           | supply voltage                 |   | 2.3          | -     | 5.5           | V             |             |
| $I_{DD}$                           | supply current                 | operating mode; no load; $f_{SCL} = 1\text{ MHz}$               |              |       |               |               |             |
|                                    |                                | $V_{DD} = 2.3\text{ V}$   | -            | 38    | 150           | $\mu\text{A}$ |             |
|                                    |                                | $V_{DD} = 3.3\text{ V}$   | -            | 53    | 150           | $\mu\text{A}$ |             |
|                                    |                                | $V_{DD} = 5.5\text{ V}$   | -            | 108   | 150           | $\mu\text{A}$ |             |
| $I_{stb}$                          | standby current                | no load; $f_{SCL} = 0\text{ Hz}$ ; I/O = inputs; $V_I = V_{DD}$ |              |       |               |               |             |
|                                    |                                | $V_{DD} = 5.5\text{ V}$ , MODE1[4] = 1 (Sleep mode)             | -            | 0.005 | 1             | $\mu\text{A}$ |             |
| $V_{POR}$                          | power-on reset voltage         | no load; $V_I = V_{DD}$ or $V_{SS}$                             | [1]          | -     | 1.70          | 2.0           | V           |
| <b>Input SCL; input/output SDA</b> |                                |   |              |       |               |               |             |
| $V_{IL}$                           | LOW-level input voltage        |   | -0.5         | -     | +0.3 $V_{DD}$ | V             |             |
| $V_{IH}$                           | HIGH-level input voltage       |   | 0.7 $V_{DD}$ | -     | 5.5           | V             |             |
| $I_{OL}$                           | LOW-level output current       | $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 2.3\text{ V}$               | 20           | -     | -             | $\text{mA}$   |             |
|                                    |                                | $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 5.0\text{ V}$               | 30           | -     | -             | $\text{mA}$   |             |
| $I_L$                              | leakage current                | $V_I = V_{DD}$ or $V_{SS}$                                      | -1           | -     | +1            | $\mu\text{A}$ |             |
| $C_i$                              | input capacitance              | $V_I = V_{SS}$  | -            | 6     | 10            | $\text{pF}$   |             |
| <b>LED driver outputs</b>          |                                |   |              |       |               |               |             |
| $I_{OL}$                           | LOW-level output current       | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 2.3\text{ V}$               | [2]          | 12    | -             | -             | $\text{mA}$ |
|                                    |                                | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 3.0\text{ V}$               | [2]          | 17    | -             | -             | $\text{mA}$ |
|                                    |                                | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 4.5\text{ V}$               | [2]          | 25    | -             | -             | $\text{mA}$ |
| $I_{OL(tot)}$                      | total LOW-level output current | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 4.5\text{ V}$               | [2]          | -     | -             | 100           | $\text{mA}$ |
| $V_{OH}$                           | HIGH-level output voltage      | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 2.3\text{ V}$              | 1.6          | -     | -             | V             |             |
|                                    |                                | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 3.0\text{ V}$              | 2.3          | -     | -             | V             |             |
|                                    |                                | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 4.5\text{ V}$              | 4.0          | -     | -             | V             |             |
| $C_o$                              | output capacitance             |   | -            | 2.5   | 5             | $\text{pF}$   |             |

[1]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 100 mA due to internal busing limits.

### 13. Dynamic characteristics

Table 19. Dynamic characteristics

| Symbol              | Parameter   | Conditions | Standard- mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus |     | Fast-mode Plus I <sup>2</sup> C-bus |      | Unit |
|---------------------|---|------------|-------------------------------------|------|--------------------------------|-----|-------------------------------------|------|------|
|                     |   |            | Min                                 | Max  | Min                            | Max | Min                                 | Max  |      |
| f <sub>SCL</sub>    | SCL clock frequency   | [1]        | 0                                   | 100  | 0                              | 400 | 0                                   | 1000 | kHz  |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition                  |            | 4.7                                 | -    | 1.3                            | -   | 0.5                                 | -    | μs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition                              |            | 4.0                                 | -    | 0.6                            | -   | 0.26                                | -    | μs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition                        |            | 4.7                                 | -    | 0.6                            | -   | 0.26                                | -    | μs   |
| t <sub>SU;STO</sub> | set-up time for STOP condition                                    |            | 4.0                                 | -    | 0.6                            | -   | 0.26                                | -    | μs   |
| t <sub>HD;DAT</sub> | data hold time  |            | 0                                   | -    | 0                              | -   | 0                                   | -    | ns   |
| t <sub>VD;ACK</sub> | data valid acknowledge time                                       | [2]        | 0.3                                 | 3.45 | 0.1                            | 0.9 | 0.05                                | 0.45 | μs   |
| t <sub>VD;DAT</sub> | data valid time   | [3]        | 0.3                                 | 3.45 | 0.1                            | 0.9 | 0.05                                | 0.45 | μs   |
| t <sub>SU;DAT</sub> | data set-up time  |            | 250                                 | -    | 100                            | -   | 50                                  | -    | ns   |
| t <sub>LOW</sub>    | LOW period of the SCL clock                                       |            | 4.7                                 | -    | 1.3                            | -   | 0.5                                 | -    | μs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock                                      |            | 4.0                                 | -    | 0.6                            | -   | 0.26                                | -    | μs   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals                             | [4][5]     | -                                   | 300  | 20 + 0.1C <sub>b</sub> [6]     | 300 | -                                   | 120  | ns   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals                             |            | -                                   | 1000 | 20 + 0.1C <sub>b</sub> [6]     | 300 | -                                   | 120  | ns   |
| t <sub>SP</sub>     | pulse width of spikes that must be suppressed by the input filter | [7]        | -                                   | 50   | -                              | 50  | -                                   | 50   | ns   |

- [1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.
- [2] t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
- [3] t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.
- [4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to [Table 18](#), V<sub>IL</sub> of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
- [5] The maximum t<sub>f</sub> for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t<sub>f</sub>) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t<sub>f</sub>.
- [6] C<sub>b</sub> = total capacitance of one bus line in pF.
- [7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

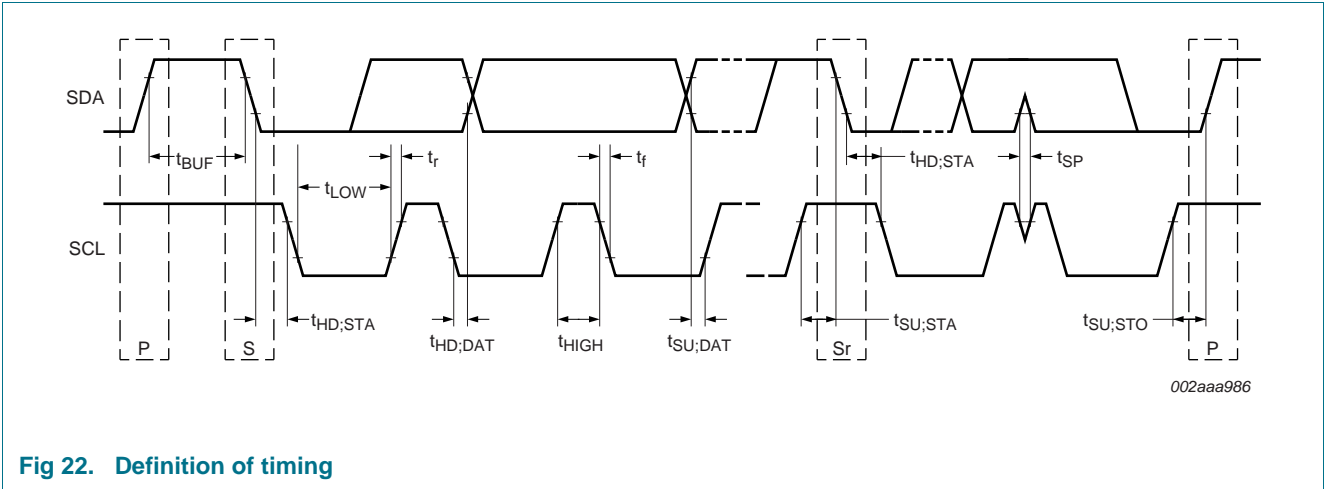
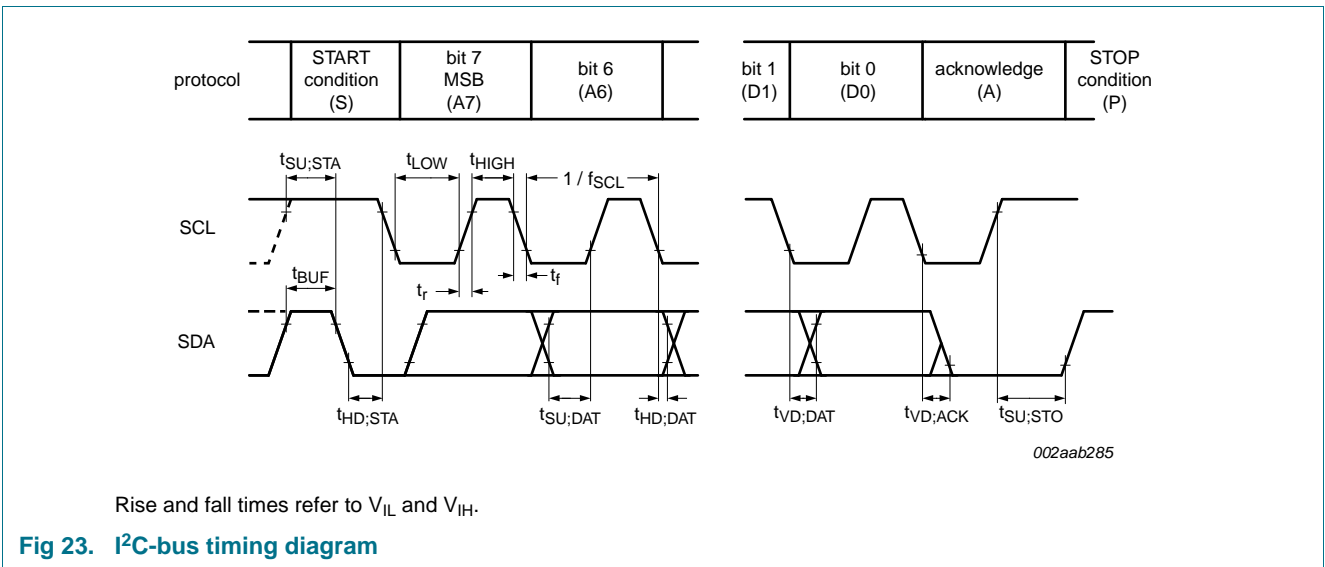


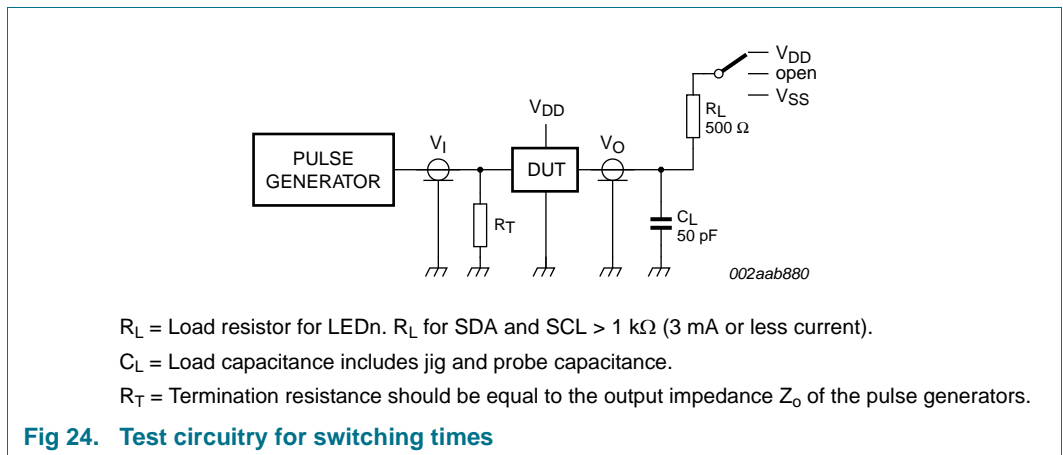
Fig 22. Definition of timing



Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .

Fig 23. I<sup>2</sup>C-bus timing diagram

## 14. Test information



$R_L$  = Load resistor for LEDn.  $R_L$  for SDA and SCL > 1 k $\Omega$  (3 mA or less current).

$C_L$  = Load capacitance includes jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generators.

Fig 24. Test circuitry for switching times

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

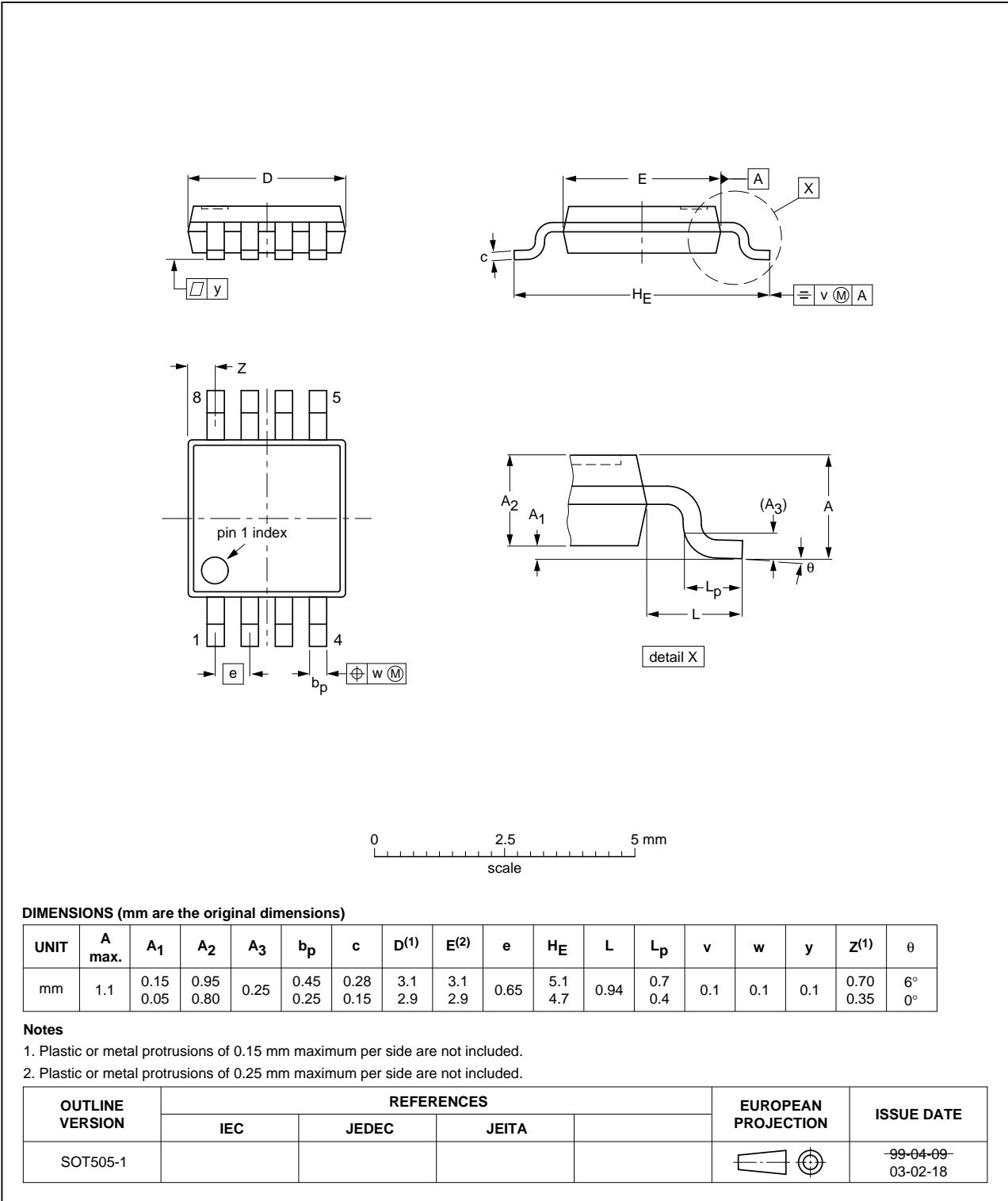


Fig 25. Package outline SOT505-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads;  
8 terminals; body 3 x 3 x 0.85 mm

SOT908-1

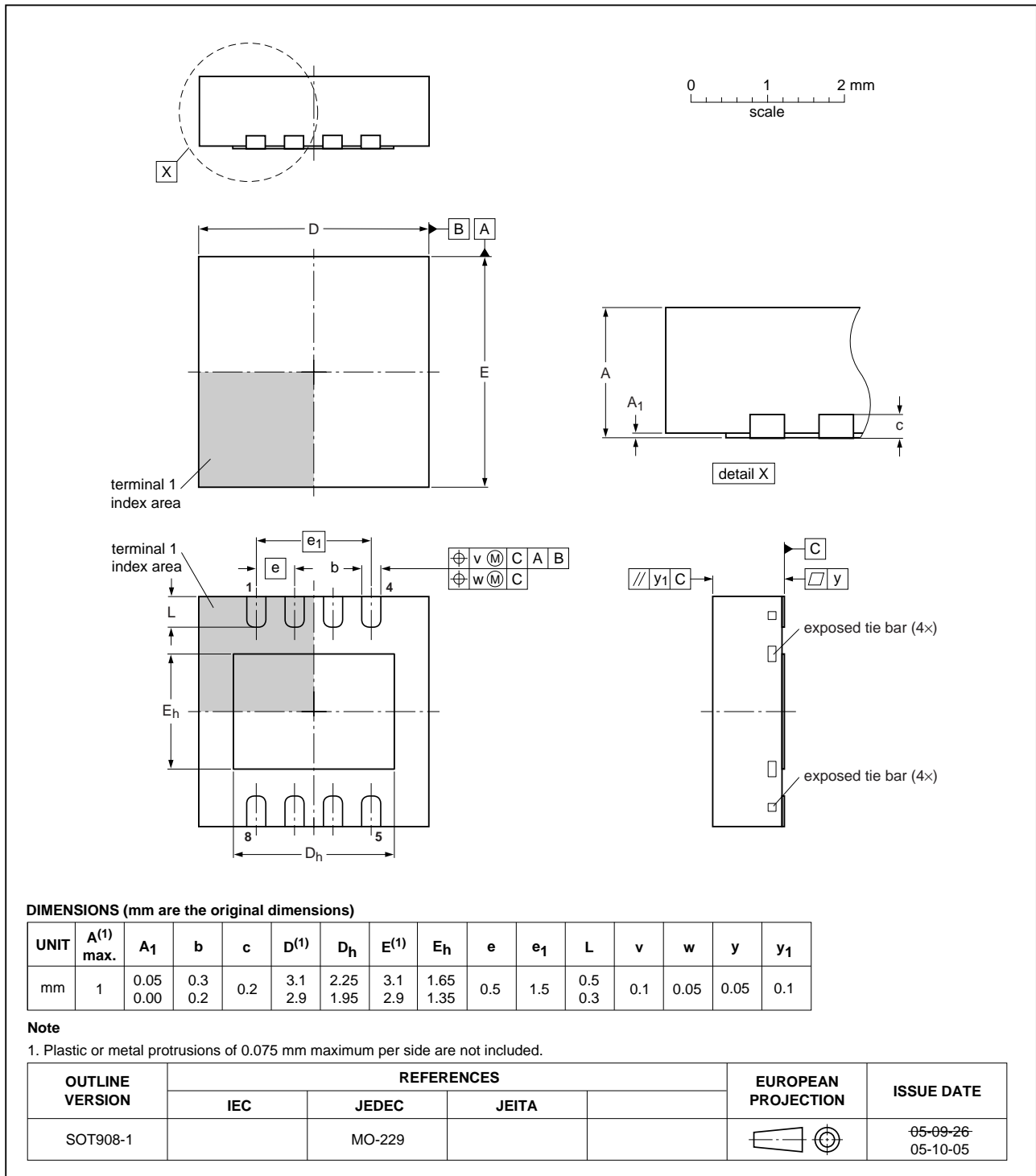


Fig 26. Package outline SOT908-1 (HVSON8)

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1

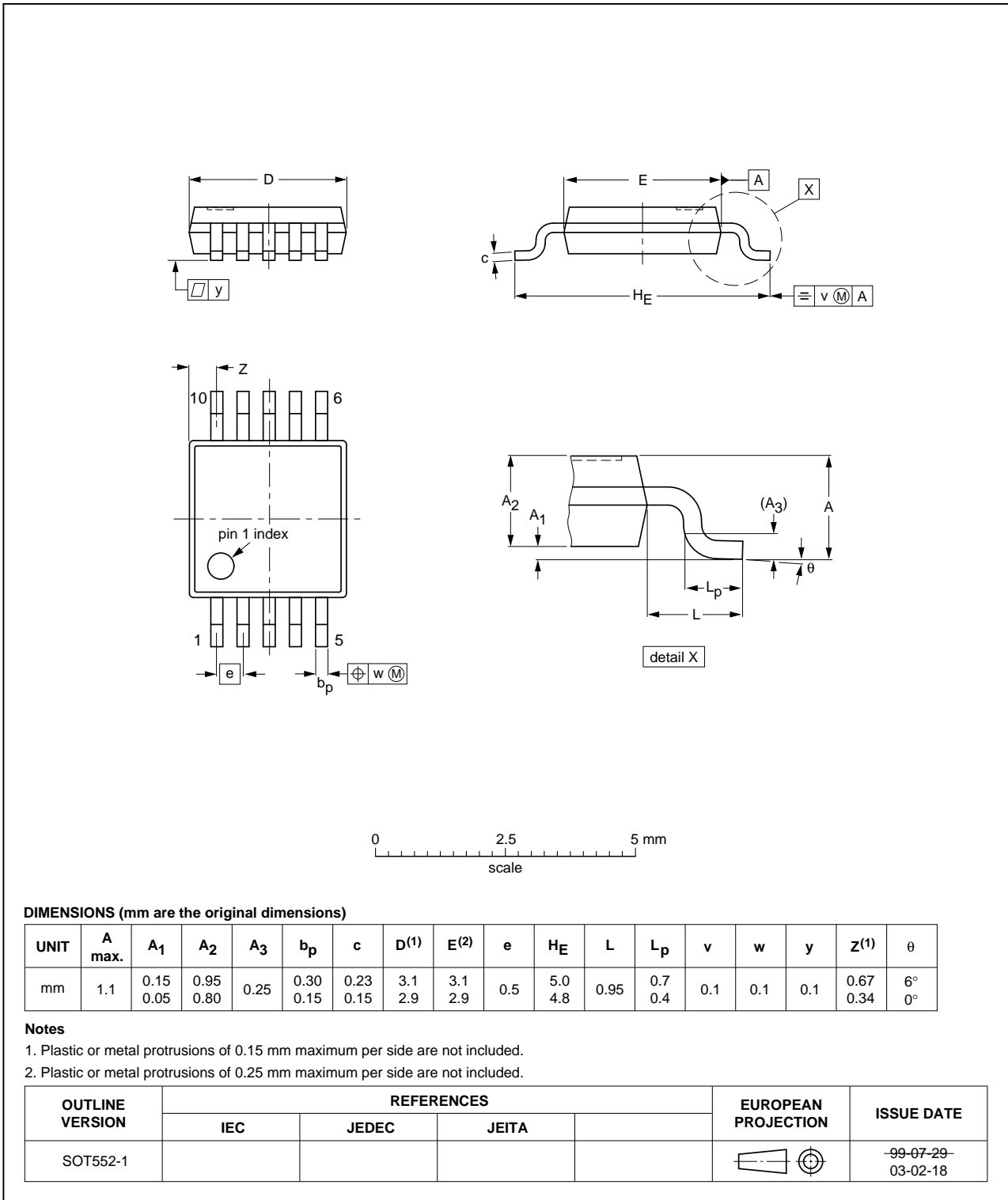
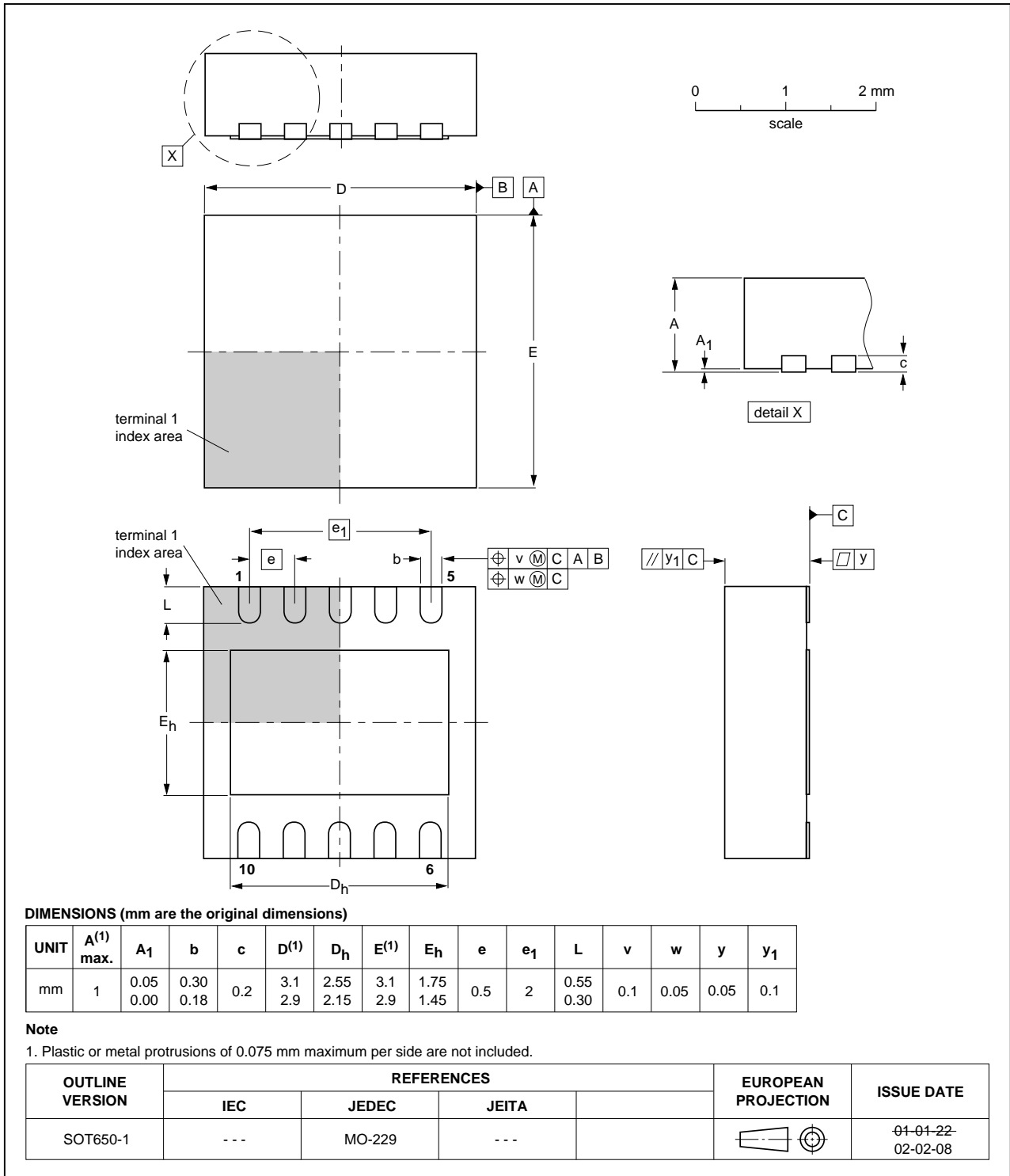


Fig 27. Package outline SOT552-1 (TSSOP10)

**HVSON10: plastic thermal enhanced very thin small outline package; no leads;  
10 terminals; body 3 x 3 x 0.85 mm**

**SOT650-1**



**Fig 28. Package outline SOT650-1 (HVSON10)**



## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 29](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 20](#) and [21](#)

**Table 20. SnPb eutectic process (from J-STD-020C)**

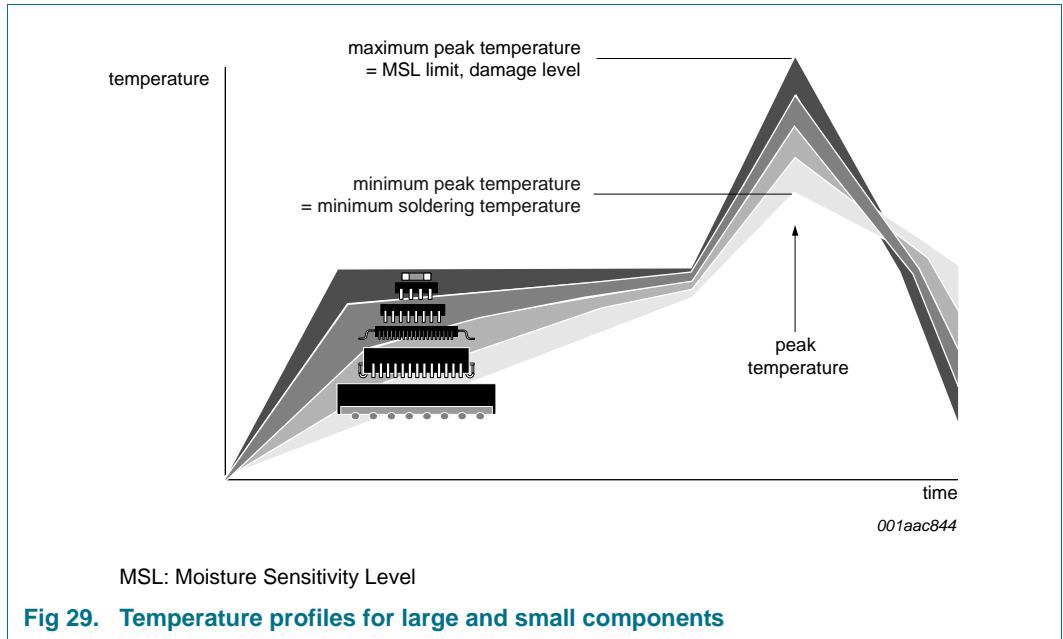
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 21. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 29](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 18. Abbreviations

**Table 22. Abbreviations**

| Acronym              | Description                                |
|----------------------|--|
| CDM                  | Charged-Device Model                       |
| DUT                  | Device Under Test                          |
| ESD                  | ElectroStatic Discharge                    |
| HBM                  | Human Body Model                           |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus               |
| LCD                  | Liquid Crystal Display                     |
| LED                  | Light Emitting Diode                       |
| LSB                  | Least Significant Bit                      |
| MSB                  | Most Significant Bit                       |
| NMOS                 | Negative-channel Metal-Oxide Semiconductor |
| PCB                  | Printed-Circuit Board                      |
| PMOS                 | Positive-channel Metal-Oxide Semiconductor |
| PWM                  | Pulse Width Modulation                     |
| RGB                  | Red/Green/Blue                             |
| RGBA                 | Red/Green/Blue/Amber                       |
| SMBus                | System Management Bus                      |

## 19. Revision history

Table 23. Revision history

| Document ID    | Release date   | Data sheet status    | Change notice | Supersedes  |
|----------------|--|----------------------|---------------|-------------|
| PCA9632 v.5    | 20110727   | Product data sheet   | -             | PCA9632 v.4 |
| Modifications: | <ul style="list-style-type: none"> <li>• <a href="#">Figure 10 "Brightness + group dimming signals"</a> modified</li> </ul>  |                      |               |             |
| PCA9632 v.4    | 20110701   | Product data sheet   | -             | PCA9632 v.3 |
| Modifications: | <ul style="list-style-type: none"> <li>• <a href="#">Section 2 "Features and benefits"</a>, 24th bullet item: deleted phrase "200 V MM per JESD22-A115"</li> <li>• <a href="#">Table 18 "Static characteristics"</a>, sub-section "Supply": <ul style="list-style-type: none"> <li>– Condition for I<sub>DD</sub>: changed from "f<sub>SCL</sub> = 0 MHz" to "f<sub>SCL</sub> = 1 MHz"</li> <li>– Condition for I<sub>stb</sub>: appended ", MODE1[4] = 1 (Sleep mode)"</li> </ul> </li> </ul> |                      |               |             |
| PCA9632 v.3    | 20080715   | Product data sheet   | -             | PCA9632 v.2 |
| PCA9632 v.2    | 20080401   | Product data sheet   | -             | PCA9632 v.1 |
| PCA9632 v.1    | 20070928   | Objective data sheet | -             | -           |

## 20. Legal information

### 20.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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