

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74		SERIES 54H SERIES 74H		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
		'00, '04, '10, '20, '30	MIN NOM MAX	'400, '404, '410, '420, '430	MIN NOM MAX	'L00, 'L04, 'L10, 'L20, 'L30	MIN NOM MAX	'L804, 'L810, 'L820, 'L830	MIN NOM MAX	'800, '804, '810, '820, '830, '8133		
Supply voltage, V _{CC}	54 Family	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	V	
	74 Family	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25		
	54 Family	-400	-600	-500	-100	-400	-1000	-400	-1000	-1000	μA	
	74 Family	-400	-500	-200	-200	-400	-1000	-400	-1000	-1000		
High-level output current, I _{OH}	54 Family	16	20	20	2	4	20	20	20	20	mA	
	74 Family	16	20	20	3.6	8	20	20	20	20		
Low-level output current, I _{OL}	54 Family	-55	125	-55	125	-55	125	-55	125	-55	125	°C
	74 Family	0	70	0	70	0	70	0	70	0	70	
Operating free-air temperature, T _A												

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	TEST CONDITIONS†										UNIT	
			SERIES 54 SERIES 74		SERIES 54H SERIES 74H		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
V _{IH} High-level input voltage	1, 2		2		2		2		2		2		V	
V _{IL} Low-level input voltage	1, 2	54 Family 74 Family	0.8 0.8		0.8 0.8		0.7 0.7		0.7 0.8		0.8 0.8		V	
V _{IK} Input clamp voltage	3		-1.5		-1.5								V	
V _{OH} High-level output voltage	1	54 Family 74 Family	2.4 2.4	3.4 3.5	2.4 2.4	3.3 3.5	2.5 2.5	3.4 3.4	2.5 2.7	3.4 3.4	2.5 2.7	3.4 3.4	V	
V _{OL} Low-level output voltage	2	54 Family 74 Family	0.2 0.2	0.4 0.4	0.2 0.2	0.4 0.4	0.15 0.2	0.3 0.4	0.25 0.25	0.4 0.5	0.5 0.5	0.5 0.5	V	
I _I Input current at maximum input voltage	4	Series 74LS V _I = 5.5 V V _I = 7 V	1		1		0.1				1		mA	
I _{IH} High-level input current	4	V _{IH} = 2.4 V V _{IH} = 2.7 V	40		50		10						μA	
I _{IL} Low-level input current	5	V _{IL} = 0.3 V V _{IL} = 0.4 V	-1.6		-2		-0.18						mA	
I _{OS} Short-circuit output current†	6	V _{IL} = 0.5 V 54 Family 74 Family	-20 -20	55 55	-40 -40	-100 -100	-3 -3	-15 -15	-20 -20	-40 -40	-100 -100	-100 -100	mA	
I _{CC} Supply current	7	V _{CC} = MAX	-18	-56	-40	-100	-3	-15	-20	-40	-100	-100	mA	

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

³ $I_{IH} = -12 \text{ mA}$ for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN64LS/SN74LS, and SN64S/SN74S.

⁴ Not more than one output should be shorted at a time, and for SN54H/SN74H, SN64LS/SN74LS, and SN64S/SN74S, duration of short-circuit should not exceed 1 second.

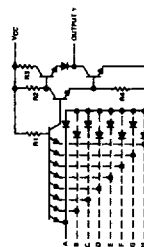
POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

supply current†

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'00	4	8	12	22	2	2
'04	6	12	18	33	2	2
'10	3	6	9	16.5	2	2
'20	2	4	6	11	2	2
'30	1	2	3	6	2	2
'H00	10	16.8	26	40	4.5	4.5
'H04	16	26	40	58	4.5	4.5
'H10	7.5	12.6	19.5	30	4.5	4.5
'H20	5	8.4	13	20	4.5	4.5
'H30	2.5	4.2	6.5	10	4.5	4.5
'L00	0.44	0.8	1.16	2.04	0.20	0.20
'L04	0.66	1.2	1.74	3.06	0.20	0.20
'L10	0.33	0.6	0.87	1.53	0.20	0.20
'L20	0.22	0.4	0.56	1.02	0.20	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20	0.20
'LS00	0.8	1.6	2.4	4.4	0.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4	0.4
'LS10	0.6	1.2	1.8	3.3	0.4	0.4
'LS20	0.4	0.8	1.2	2.2	0.4	0.4
'LS30	0.35	0.6	0.6	1.1	0.48	0.48
'S00	10	16	20	36	3.75	3.75
'S04	15	24	30	54	3.75	3.75
'S10	7.5	12	15	27	3.75	3.75
'S20	5	8	10	18	3.75	3.75
'S30	3	6	5.5	10	4.25	4.25
'S133	3	5	5.5	10	4.25	4.25

† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

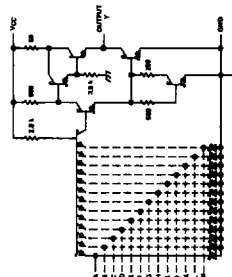
'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS

Input clamp diodes not on SN54L/SN74L circuits.

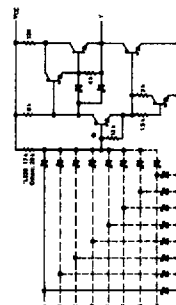
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C _L = 15 pF, R _L = 400 Ω	11	22		7	15	
'04, '20		12	22		8	15	
'30		13	22		8	15	
'H00	C _L = 25 pF, R _L = 280 Ω	5.9	10		6.2	10	
'H04		6	10		6.5	10	
'H10		5.9	10		6.3	10	
'H20	C _L = 50 pF, R _L = 4 kΩ	6	10		7	10	
'H30		6.8	10		8.9	12	
'L00, 'L04		35	60		31	60	
'L10, 'L20	C _L = 15 pF, R _L = 2 kΩ	35	60		70	100	
'L30		35	60		70	100	
'LS00, 'LS04	C _L = 15 pF, R _L = 2 kΩ	9	15		10	15	
'LS10, 'LS20		8	15		13	20	
'LS30		3	4.5		3	5	
'S00, 'S04	C _L = 15 pF, R _L = 280 Ω	4.5			5		
'S10, 'S20		3	4.5		4.5		
'S30, 'S133		4	6		4.5	7	
	C _L = 50 pF, R _L = 280 Ω	5.5			6.5		

Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.



'S00, 'S04, 'S10, 'S20,
'S30, 'S133 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20,
'LS30 CIRCUITS

* The 12-kΩ resistor is not on 'LS30.

Resistor values shown are nominal and in ohms.

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74		SERIES 54H SERIES 74H		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT	
		'01, '02, '05, '12, '22		'100, '122		'L01, 'L03		'L501, 'L502, 'L506, 'L512, 'L522		'900, '922			
Supply voltage, V_{CC}	54 Family	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
	74 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5
High-level output voltage, V_{OH}	54 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
	74 Family		5.5			5.5			5.5			5.5	
Low-level output current, I_{OL}	54 Family	16			20			2			4		
	74 Family		16			20			3.6		8		
Operating free-air temperature, T_A	54 Family	-55		125	-55		125	-55		125	-55		125
	74 Family	0		70	0		70	0		70	0		70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]		SERIES 84		SERIES 84H		SERIES 84L		SERIES 84LS		SERIES 84S		UNIT
				SERIES 74		SERIES 74H		SERIES 74L		SERIES 74LS		SERIES 74S		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		'01, '02, '06, '12, '22		'101, '106, '122		'L01, 'L03		'L501, 'L503, 'L506, 'L512, 'L522		'901, '922				
V_{IH} High-level input voltage	1, 2	2		2		2		2		2		2		V
V_{IL} Low-level input voltage	1, 2	0.8		0.8		0.8		0.8		0.7		0.8		V
V_{IK} Input clamp voltage	3	-1.5		-1.5		-1.5		-1.5		-1.5		-1.2		V
I_{OH} High-level output current	1	250		250		50		100		250		250		μA
V_{OL} Low-level output voltage	2	0.2		0.4		0.15		0.3		0.25		0.4		V
		0.2		0.4		0.2		0.4		0.35		0.5		V
		Series 74LS		Series 74LS		Series 74LS		Series 74LS		Series 74LS		Series 74LS		V
I_{II} Input current at maximum input voltage	4	$V_I = 5.5 \text{ V}$		1		1		0.1		0.25		0.4		1
I_{IH} High-level input current	4	$V_{IH} = 2.4 \text{ V}$		40		50		10		20		50		μA
I_{IL} Low-level input current	5	$V_{IL} = 0.3 \text{ V}$		-1.8		-2		-0.18		-0.4		-2		μA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$		See table on next page		See table on next page		See table on next page		See table on next page		See table on next page		μA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

$\S_1 = -12 \text{ mA}$ for SN54/SN74[†], -8 mA for SN54H/SN74H[†], and -18 mA for SN54LS/SN74LS[†] and SN54S/SN74S[†].

See table on next page

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

supply current†

TYPE	ICCH (mA)		ICCL (mA)		ICC (mA)	
	Total with outputs high		Total with outputs low		Average per Gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'01	4	8	12	22	2	
'03	4	8	12	22	2	
'05	6	12	18	33	2	
'12	3	6	9	16.5	2	
'22	2	4	6	11	2	
'H01	6.8	10	26	40	4.1	
'H05	16	26	40	58	4.87	
'H22	3.4	5	13	20	4.1	
'L01	0.44	0.8	1.16	2.04	0.20	
'L03	0.44	0.8	1.16	2.04	0.20	
'LS01	0.8	1.6	2.4	4.4	0.4	
'LS03	0.8	1.6	2.4	4.4	0.4	
'LS05	1.2	2.4	3.6	6.8	0.4	
'LS12	0.7	1.4	1.8	3.3	0.42	
'LS22	0.4	0.8	1.2	2.2	0.4	
'S03	6	13.2	20	36	3.25	
'S05	9	19.8	30	54	3.25	
'S22	3	6.6	10	18	3.25	

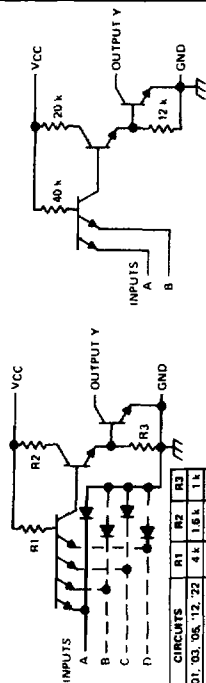
† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A . Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	φ_{LH} (ns)			φ_{PHL} (ns)		
		Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'01, '03	$C_L = 15\text{ pF}$, $R_L = 4\text{ k}\Omega$ for φ_{LH} , 400 Ω for φ_{PHL}		35	45		8	15
'05			40	55		8	15
'12, '22			35	45		8	15
'H01, 'H05, 'H22	$C_L = 25\text{ pF}$, $R_L = 280\text{ }\Omega$		10	15		7.5	12
'L01, 'L03	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$		60	90		33	60
'LS01, 'LS03, 'LS05, 'LS12, 'LS22	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$		17	32		15	28
'S03, 'S05, 'S22	$C_L = 15\text{ pF}$, $R_L = 280\text{ }\Omega$	2	5	7.5	2	4.5	7
	$C_L = 50\text{ pF}$, $R_L = 280\text{ }\Omega$		7.5				7

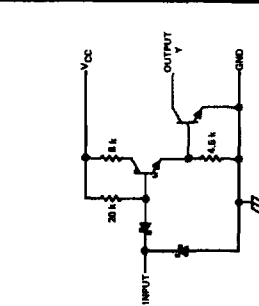
Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

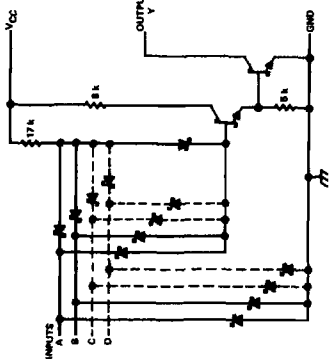


CIRCUITS	R1	R2	R3
'01, '03, '05, '12, '22	4 k	1.6 k	1 k
'H01, 'H05, 'H22	2.8 k	760	470

'L01, 'L03 CIRCUITS

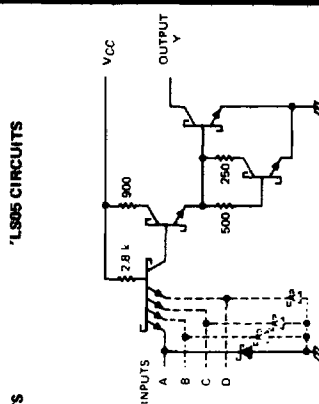


'01, '03, '05, '12, '22, 'H01, 'H05, 'H22 CIRCUITS



'LS05 CIRCUITS

'LS01, 'LS03, 'LS12, 'LS22 CIRCUITS



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH \text{ min}}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(\text{max})} = \frac{V_{CC} - V_{OH \text{ min}}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.

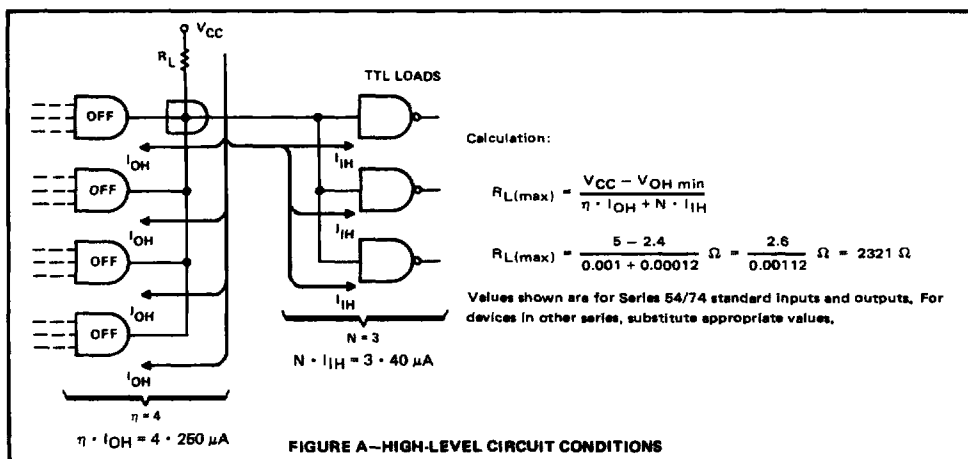


FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

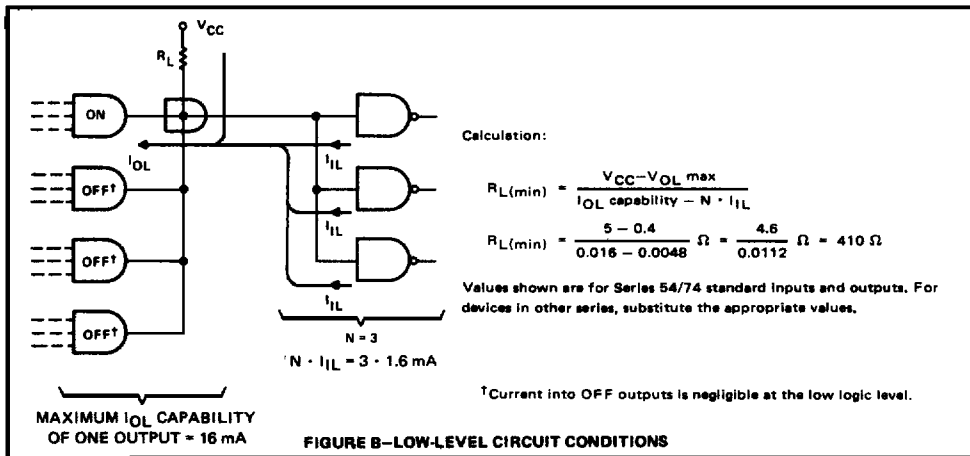
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL} , the maximum current which will ensure that the low-level output voltage, V_{OL} , will be below $V_{OL\ max}$.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L .

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}			4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I _{OH}			4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	mA
Low-level output current, I _{OL}			-400	-400	-800	-400	-400	-800	-400	-400	-800	mA
Operating free-air temperature, T _A			-55	0	70	-55	0	70	-55	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage	1, 2	54 Family 74 Family	0.8		0.7	0.7		0.7	0.7		0.8	V
V _{IL} Low-level input voltage	1, 2	54 Family 74 Family	0.8		0.7	0.7		0.8	0.8		0.7	V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 3	-1.5			-1.5			-1.5			V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4	2.4	3.3	2.5	3.4	2.5	3.4	2.7	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX, V _{IH} = 2 V	0.2	0.4	0.2	0.4	0.15	0.3	0.25	0.4	0.25	V
I _I Input current at maximum input voltage	4	V _I = 5.5 V, V _I = 7 V	1		0.1	0.1		0.1			0.1	mA
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V	40		10	10		10			10	μA
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.3 V	180		20	20		20			20	μA
I _{OS} Short-circuit output current	6	V _{CC} = MAX, V _{IH} = 2.7 V, V _{IL} = 0.4 V	-1.8		-0.4	-0.4		-0.4			-0.4	mA
I _{CC} Supply current	7	V _{CC} = MAX, V _{IH} = 0.5 V	-55		-3	-15		-20			-40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = -12 mA for SN54/SN74 and -18 mA for SN54LS/SN74LS and SN54S/SN74S.

¶Not more than one output should be shorted at a time, and for SN54LS/SN74LS and SN54S/SN74S, duration of output short-circuit should not exceed one second.

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

supply current†

TYPE	I _{CC} (mA)		I _{CC} (mA)		I _{CC} (mA)	
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'02	8	16	14	27	2.75	
'25	8	16	10	19	2.25	
'27	10	16	16	26	4.34	
'L02	0.8	1.6	1.4	2.6	0.275	
'LS02	1.6	3.2	2.8	5.4	0.55	
'LS27	2.0	4	3.4	6.8	0.9	
'S02	17	29	26	45	5.38	
'S260	17	29	26	45	10.75	

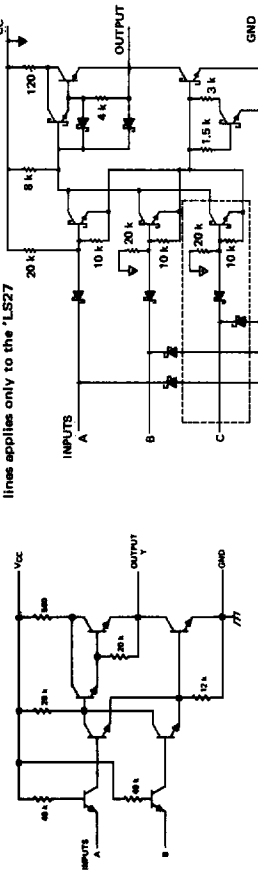
†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

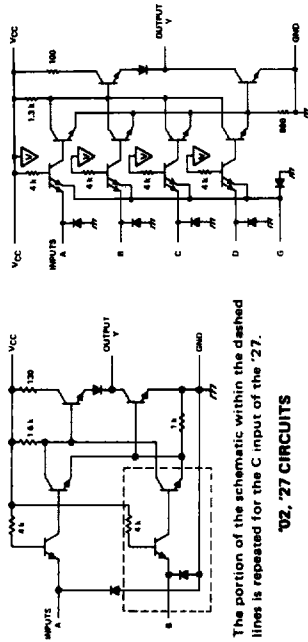
TYPE	TEST CONDITIONS#	t _{PLH} (ns)		t _{PLH} (ns)	
		Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output	
		MIN	TYP	MAX	
'02	C _L = 15 pF, R _L = 400 Ω	12	15	8	15
'25		13	22	8	15
'27		10	15	7	11
'L02	C _L = 50 pF, R _L = 4 kΩ	31	60	35	60
'LS02, 'LS27	C _L = 15 pF, R _L = 2 kΩ	10	15	10	15
'S02	C _L = 15 pF, R _L = 280 Ω	3.5	5.5	3.5	5.5
	C _L = 50 pF, R _L = 280 Ω	5	5	5	5
'S260	C _L = 15 pF, R _L = 280 Ω	4	5.5	4	6

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

The portion of the schematic within the dashed lines applies only to the 'LS27

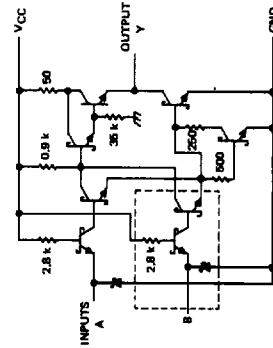


schematics (each gate)



The portion of the schematic within the dashed lines is repeated for the C input of the '27.

Resistor values are nominal and in ohms.



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74	SERIES 54H SERIES 74H	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
Supply Voltage, V_{CC}	54 Family 74 Family	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	V
High-level output current, I_{OH}	54 Family 74 Family	MIN NOM MAX -800	MIN NOM MAX -800	MIN NOM MAX -800	MIN NOM MAX -800	μ A
Low-level output current, I_{OL}	54 Family 74 Family	MIN NOM MAX 16 16	MIN NOM MAX 16 16	MIN NOM MAX 16 16	MIN NOM MAX 16 16	mA
Operating free-air temperature, T_A	54 Family 74 Family	MIN NOM MAX -55 125 175	MIN NOM MAX -55 125 175	MIN NOM MAX -55 125 175	MIN NOM MAX -55 125 175	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54 SERIES 74	SERIES 54H SERIES 74H	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
V_{IH} High-level input voltage	1, 2		MIN TYP [‡] MAX 2 0.8 0.8	MIN TYP [‡] MAX 2 0.8 0.8	MIN TYP [‡] MAX 2 0.7 0.8	MIN TYP [‡] MAX 2 0.8 0.8	V
V_{IL} Low-level input voltage	1, 2		MIN TYP [‡] MAX 0.8 0.8 0.8	MIN TYP [‡] MAX 0.8 0.8 0.8	MIN TYP [‡] MAX 0.8 0.8 0.8	MIN TYP [‡] MAX 0.8 0.8 0.8	V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}$, $I_I = 8$	MIN TYP [‡] MAX -1.5 -1.5 -1.5	MIN TYP [‡] MAX -1.5 -1.5 -1.5	MIN TYP [‡] MAX -1.5 -1.5 -1.5	MIN TYP [‡] MAX -1.5 -1.5 -1.5	V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OH} = \text{MAX}$	MIN TYP [‡] MAX 2.4 3.4 3.4	MIN TYP [‡] MAX 2.4 3.4 3.4	MIN TYP [‡] MAX 2.5 3.4 3.4	MIN TYP [‡] MAX 2.5 3.4 3.4	V
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}$, $I_{OL} = \text{MAX}$	MIN TYP [‡] MAX 0.2 0.4 0.4	MIN TYP [‡] MAX 0.15 0.3 0.3	MIN TYP [‡] MAX 0.25 0.4 0.4	MIN TYP [‡] MAX 0.25 0.4 0.4	V
I_I Input current at maximum input voltage	4	$V_{IH} = 2\text{ V}$, $I_{OL} = 4\text{ mA}$	MIN TYP [‡] MAX 1 1 1	MIN TYP [‡] MAX 1 1 1	MIN TYP [‡] MAX 1 1 1	MIN TYP [‡] MAX 1 1 1	mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$	MIN TYP [‡] MAX 40 40 40	MIN TYP [‡] MAX 50 50 50	MIN TYP [‡] MAX 20 20 20	MIN TYP [‡] MAX 20 20 20	μ A
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$	MIN TYP [‡] MAX -1.6 -1.6 -1.6	MIN TYP [‡] MAX -2 -2 -2	MIN TYP [‡] MAX -0.4 -0.4 -0.4	MIN TYP [‡] MAX -0.4 -0.4 -0.4	mA
I_{QS} Short circuit output current [§]	6	$V_{CC} = \text{MAX}$	MIN TYP [‡] MAX -20 -55 -55	MIN TYP [‡] MAX -40 -100 -100	MIN TYP [‡] MAX -20 -100 -100	MIN TYP [‡] MAX -20 -100 -100	mA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$	MIN TYP [‡] MAX -18 -55 -55	MIN TYP [‡] MAX -40 -100 -100	MIN TYP [‡] MAX -20 -100 -100	MIN TYP [‡] MAX -40 -100 -100	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 2.5\text{ V}$.

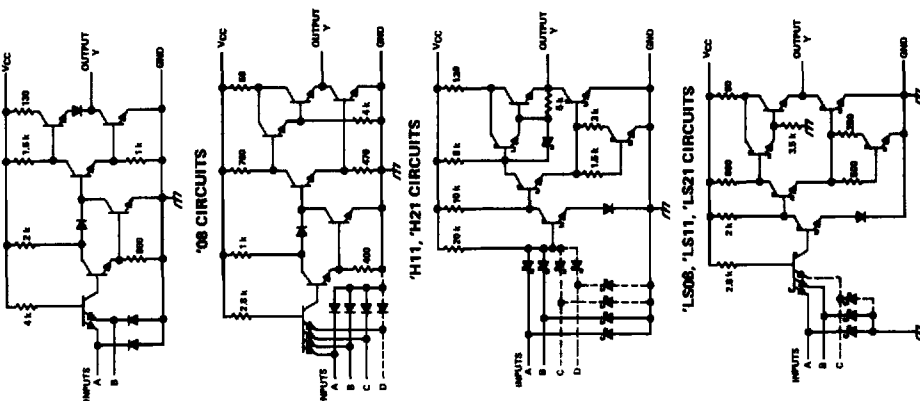
[§] $I_I = -12\text{ mA}$ for SN54/SN74[†], -8 mA for SN54H/SN74H[†], and -18 mA for SN54LS/SN74LS[†] and SN54S/SN74S[†].

[¶] Not more than one output should be shorted at a time, and for SN54H/SN74H[†], SN54LS/SN74LS[†] and SN54S/SN74S[†], duration of output short circuit should not exceed one second.

See table on next page

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

schematics (each gate)



Resistor values shown are nominal and in ohms.

supply current[†]

TYPE	I _{CC} (mA)		I _{QCL} (mA)		I _{CC} (mA)	
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'08	11	21	20	33	3.88	
'H11	18	30	30	48	8	
'H21	12	20	20	32	8	
'LS08	2.4	4.8	4.4	8.8	0.85	
'LS11	1.8	3.6	3.3	6.6	0.85	
'LS21	1.2	2.4	2.2	4.4	0.85	
'S08	18	32	32	57	6.25	
'S11	13.5	24	24	42	6.25	

[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _p LH (ns)			t _p HL (ns)		
		Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C _L = 15 pF, R _L = 400 Ω		17.5	27		12	19
'H11, 'H21	C _L = 25 pF, R _L = 280 Ω		7.6	12		8.8	12
'LS08, 'LS11	C _L = 15 pF, R _L = 2 kΩ		8	15		10	20
'LS21	C _L = 15 pF, R _L = 280 Ω		4.5	7		5	7.5
'S08, 'S11	C _L = 50 pF, R _L = 280 Ω		6			7.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74	SERIES 54H SERIES 74H	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
Supply Voltage, V_{CC}	54 Family 74 Family	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	V
High-level output voltage, V_{OH}	54 Family 74 Family	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	V
Low-level output current, I_{OL}	54 Family 74 Family	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	mA
Operating free-air temperature, T_A	54 Family 74 Family	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	MIN NOM MAX 4.5 5 5.5 4.75 5 5.25	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74	SERIES 54H SERIES 74H	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
V_{IH} High-level input voltage	1, 2		MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.7	MIN TYP‡ MAX 2 0.8 0.8	V
V_{IL} Low-level input voltage	1, 2		MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = 8$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, I_{OL} = 4 \text{ mA}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ $I_I = -12 \text{ mA}$ for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54LS/SN74LS.

See table on next page

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

supply current¹

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'09	11	21	20	33	3.88	
'H15	15	25	30	48	7.5	
'LS09	2.4	4.8	4.4	8.8	0.85	
'LS15	1.8	3.6	3.3	6.6	0.85	
'S09	18	32	32	57	6.25	
'S15	10.5	19.5	24	42	5.75	

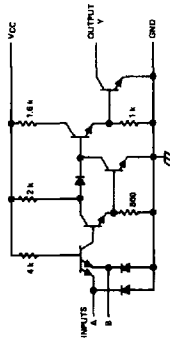
¹Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A . Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

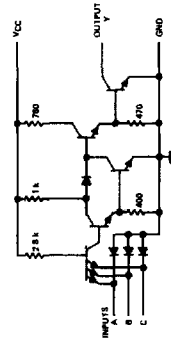
TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output		t _{PHL} (ns) Propagation delay time, high-to-low-level output	
		MIN	MAX	MIN	MAX
'09	C _L = 15 pF, R _L = 400 Ω	21	32	16	24
'H15	C _L = 25 pF, R _L = 280 Ω	12	18	9	13
'LS09, 'LS15	C _L = 15 pF, R _L = 2 kΩ	20	35	17	35
'S09	C _L = 15 pF, R _L = 280 Ω	6.5	10	6.5	10
	C _L = 50 pF, R _L = 280 Ω	9		9	
'S15	C _L = 15 pF, R _L = 280 Ω	5.5	8.5	6	9
	C _L = 50 pF, R _L = 280 Ω	8.5		8	

[#]Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

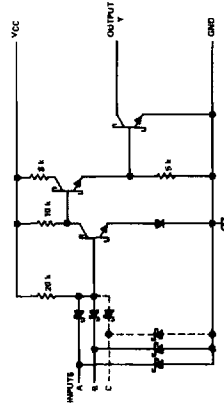
schematics (each gate)



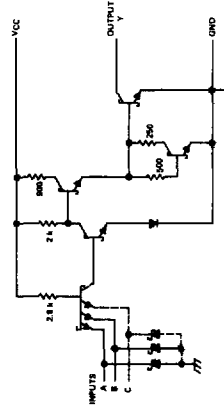
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

[illegible]

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 64 SERIES 74						SERIES 54LS SERIES 74LS						SERIES 64S SERIES 74AS					
			'13			'14, '132			'LS13, 'LS14, 'LS132			'S132								
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{TH}	8	V _{CC} = 5 V	0.6	1.7	2	1.5	1.7	2	1.4	1.6	1.9	1.6	1.7	1.9	V					
V _{T-}	9	V _{CC} = 5 V	0.5	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1	1.1	1.22	1.4	V					
Hysteresis (V _{TH} -V _{T-})	8, 9	V _{CC} = 5 V	0.4	0.8		0.4	0.8		0.4	0.8		0.2	0.85		V					
V _{IK}	3	V _{CC} = MIN, I _I = 8			-1.5			-1.5			1.5			-1.2	V					
V _{OH}	9	V _{CC} = MIN, V _I - V _{T+} min	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V					
		V _{OH} - MAX, 74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		V					
		V _{OL} - MAX, 54 Family		0.2	0.4		0.2	0.4		0.25	0.4		0.5		V					
		V _{OL} - MAX, 74 Family		0.2	0.4		0.2	0.4		0.35	0.5		0.5		V					
		I _{OL} = 4 mA Series 74LS								0.25	0.4									
I _{IT+}	8	V _{CC} = 5 V, V _I = V _{T+}		-0.65			-0.43			-0.14			-0.9		mA					
I _{IT-}	9	V _{CC} = 5 V, V _I = V _{T-}		-0.85			-0.56			-0.18			-1.1		mA					
I _I	4	V _{CC} = MAX Input current at maximum input voltage			1		1						1		mA					
		V _I = 5.5 V V _I = 7 V											0.1							
I _{IH}	4	V _I = 2.4 V High-level input current			40		40						50		µA					
		V _I = 2.7 V											20							
I _{IL}	5	V _I = 0.4 V Low-level input current			-1		-0.8			-0.4			-2		mA					
		V _{I(L)} = 0.5 V											-40							
I _{OS}	6	V _{CC} = MAX Short-circuit output current‡	-18	-35	-85	-18	-55	-20	-100	-40	-100	-40	-100	-100	mA					

† Ent conditions shown as MIN or MAX: use the appropriate value specified under recommended operating conditions.

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§11 = -12 mA for SN54/SN74' and -18 mA for 'LS13, 'LS14, 'LS132, and 'S132.

◆ Not more than one output should be shorted at a time, and for SN54LS/SN74LS' and 'S132, duration of output short-circuit should not exceed one second.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

supply current[†]

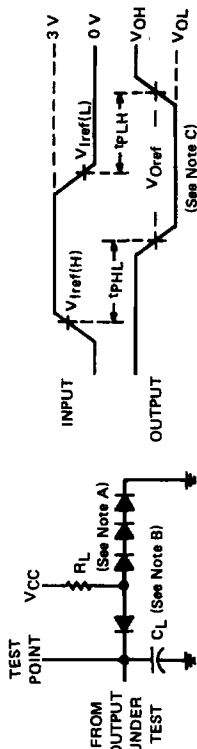
TYPE	I _{CC} (mA)		I _{CC} (mA)		I _{CC} (mA)	
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'13	14	23	20	32	8.5	
'14	22	36	39	60	5.1	
'132	15	24	26	40	5.1	
'LS13	2.9	6	4.1	7	1.75	
'LS14	8.6	16	12	21	1.72	
'LS132	5.9	11	8.2	14	1.76	
'S132	28	44	44	68	9	

[†] Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A: typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t _{PLH} (ns)		t _{PHL} (ns)	
		MIN	TYP	MAX	TYP
'13	C _L = 15 pF, R _L = 400 Ω	18	27	15	22
'14, '132		15	22	15	22
'LS13	C _L = 15 pF, R _L = 2 kΩ	15	22	18	27
'LS14		15	22	15	22
'LS132	C _L = 15 pF, R _L = 280 Ω	15	22	15	22
'S132		7	10.5	8.5	13

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

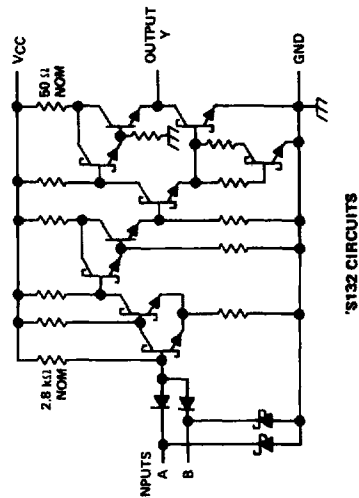
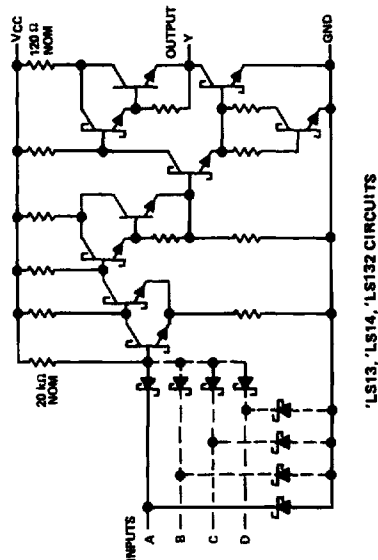
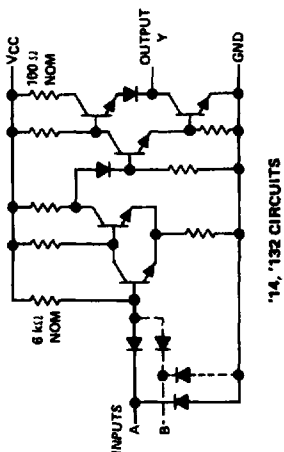
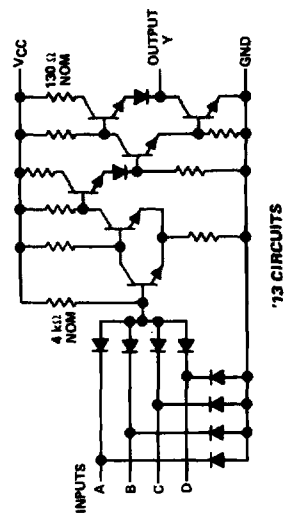
VOLTAGE WAVEFORMS

NOTES: A. All diodes are 1N916 or 1N3064.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltages are:

Generator Characteristics				Reference Voltages		
Z _{out}	PRR	t _r	t _f	V _{I ref(H)}	V _{I ref(L)}	V _{O ref}
50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.8 V	1.5 V
50 Ω	1 MHz	15 ns	6 ns	1.8 V	0.8 V	1.3 V
50 Ω	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL CHARACTERISTICS OF '13, '14, AND '132 CIRCUITS†

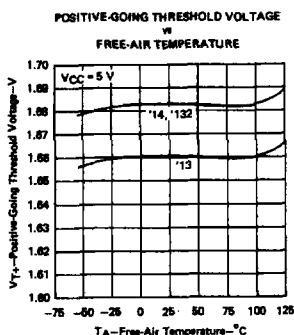


FIGURE 1

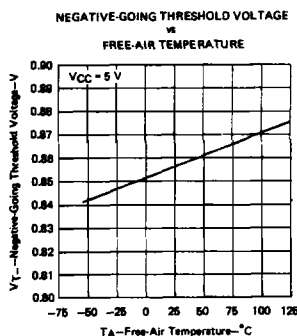


FIGURE 2

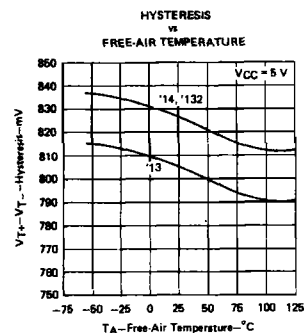


FIGURE 3

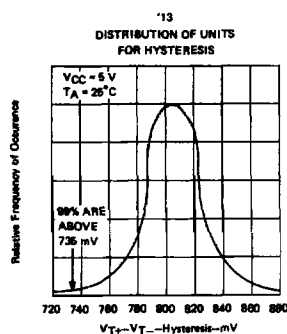


FIGURE 4

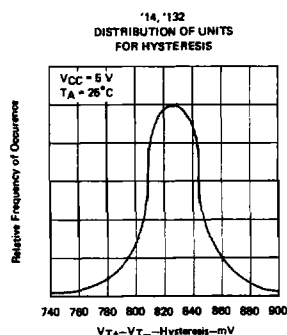


FIGURE 5

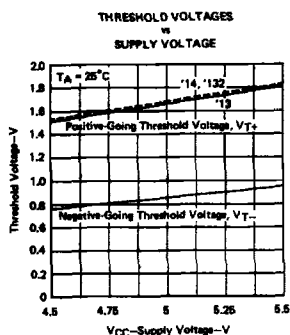


FIGURE 6

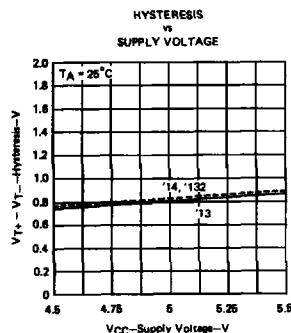


FIGURE 7

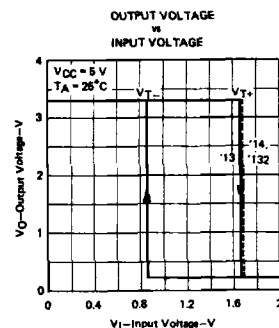
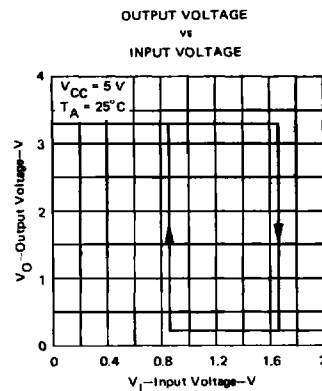
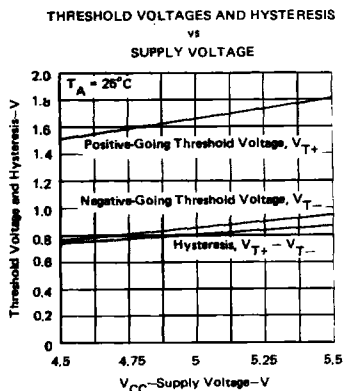
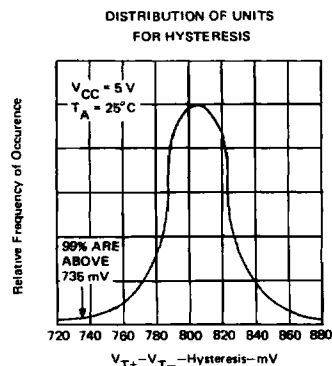
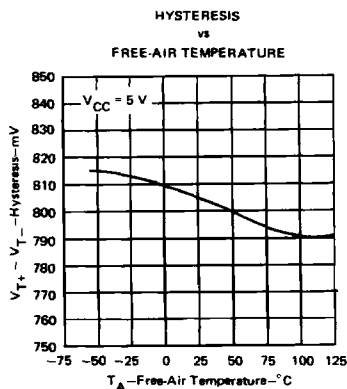
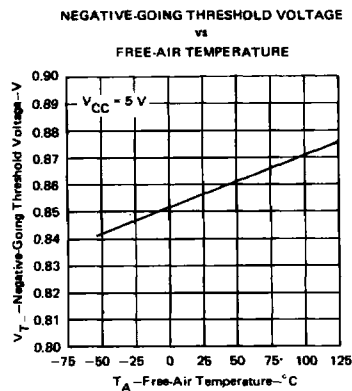
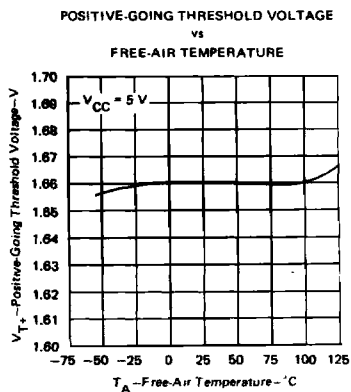


FIGURE 8

†Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5413, SN5414, and SN54132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

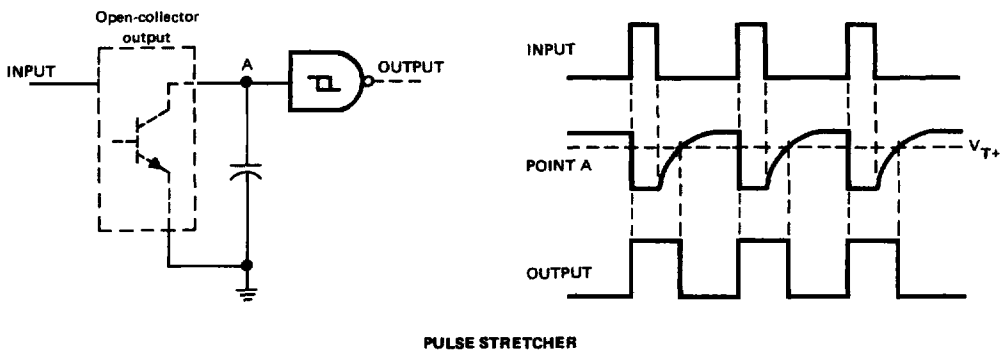
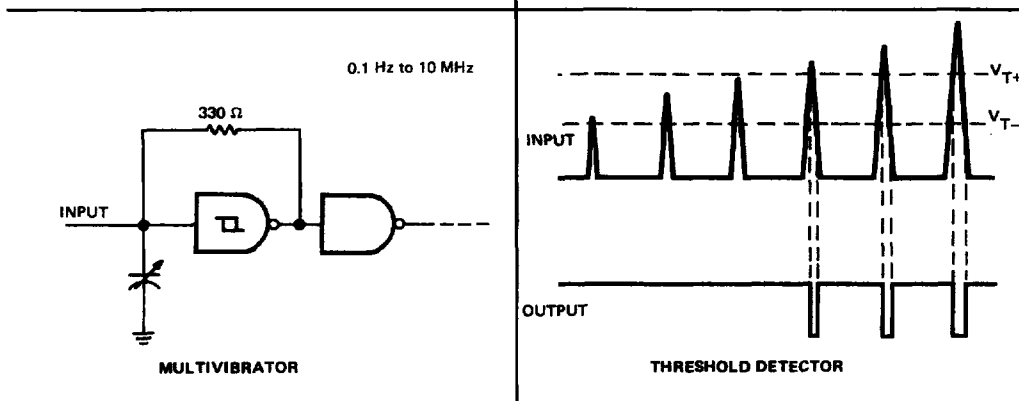
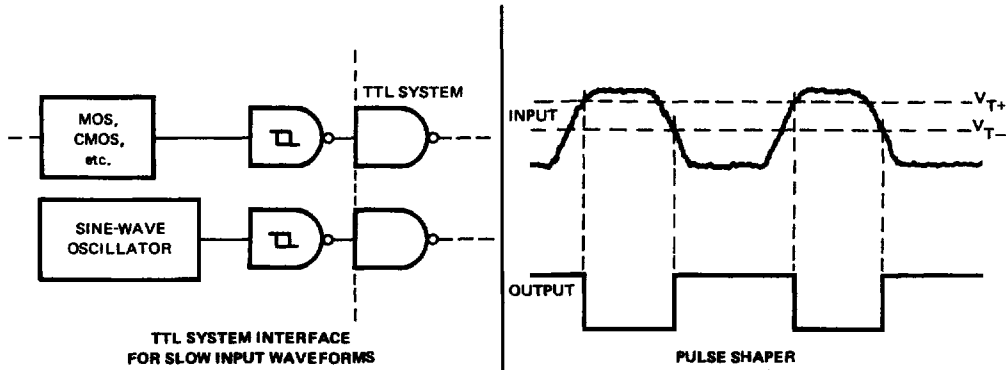
TYPICAL CHARACTERISTICS OF 'LS13, 'LS14, AND 'LS132 CIRCUITS†



† Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL APPLICATION DATA



BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74				SERIES 54H SERIES 74H				SERIES 54LS SERIES 74LS				UNIT
		'28		'37, '40		'1440		'LS28, 'LS37		'LS40		'S37, 'S40		
Supply voltage, V _{CC}	54 Family	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	V
	74 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	
High-level output current, I _{OH}	54 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	mA
	74 Family	-2.4		-1.2			-1.5			-1.2			-3	
Low-level output current, I _{OL}	54 Family	48		48			60			60			60	mA
	74 Family	48		48			60			60			60	
Operating free-air temperature, T _A	54 Family	-55	125	-65	125	-55	125	-55	125	-55	125	-55	125	°C
	74 Family	0	70	0	70	0	70	0	70	0	70	0	70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74				SERIES 54H SERIES 74H				SERIES 54LS SERIES 74LS				UNIT
			'28	MIN	TYP	MAX	'40	MIN	TYP	MAX	'40	MIN	TYP	MAX	
V_{IH} High-level input voltage	1, 2		2		0.8	0.8	0.8	2		0.8	0.8	2		0.8	V
V_{IL} Low-level input voltage	1, 2				0.8	0.8	0.8			0.8	0.8			0.8	V
V_{IK} Input clamp voltage	3				-1.5	-1.5	-1.5			-1.5	-1.5			-1.5	V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}, V_{IL} = V_{IL \text{ max}}$	2.4	3.4	2.4	3.3	2.4	3.4	2.4	3.4	2.5	3.4	2.7	3.4	V
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.25	0.4	0.25	0.4	V
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}$	1		1	1	1	0.1		0.1					mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$	40		40	40	100		100						µA
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$	-1.6		-1.6	-1.6	-4		-4						mA
I_{OS} Short-circuit output current*	6		-70	-180	-70	-70	-125	-40	-125	-40	-130	-50	-130	-50	mA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$	-70	-180	-70	-70	-125	-40	-125	-40	-130	-50	-130	-50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

*Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for all of these circuits except 'S37' and 'S40', or 100 milliseconds for 'S37' and 'S40'.

BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

supply current!

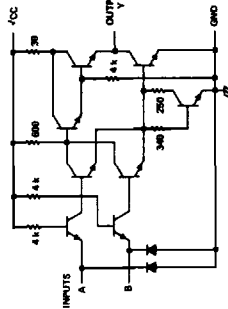
TYPE	I _{QCH} (mA) Total with outputs high		I _{QCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)	
	TYPE	MAX	TYPE	MAX	TYPE	MAX
'28	12	21	33	57		5.63
'37	9	15.5	34	54		5.38
'40	8	14	27	27		5.25
'440	10.4	16	25	40		8.85
'LS28	1.8	3.6	6.9	13.8		1.09
'LS37	0.9	2	6	12		0.86
'LS40	0.45	1	3	6		0.86
'S37	20	36	46	80		8.25
'S40	10	18	25	44		8.75

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low output		
		MIN	TYP	MAX	MIN	TYP	MAX
'26	C _L = 50 pF, R _L = 133 Ω		6	9		8	12
	C _L = 150 pF, R _L = 133 Ω		10	15		12	18
'37	C _L = 45 pF, R _L = 133 Ω		13	22		8	15
'40	C _L = 15 pF, R _L = 133 Ω		13	22		8	15
'440	C _L = 25 pF, R _L = 93 Ω		8.5	12		6.5	12
'LS28			12	24		12	24
'LS37	C _L = 45 pF, R _L = 967 Ω		12	24		12	24
'LS40			12	24		12	24
'337,	C _L = 50 pF, R _L = 93 Ω		4	6.5		4	6.5
'S40	C _L = 150 pF, R _L = 93 Ω		6			6	

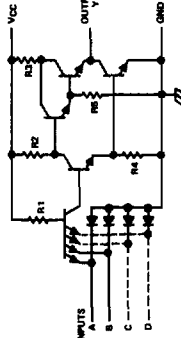
Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

V_{CC} and T_A : typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

schematics (each date)

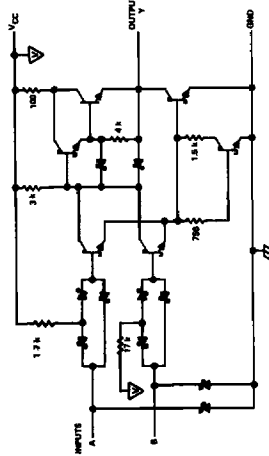


"28 CIRCUITS"



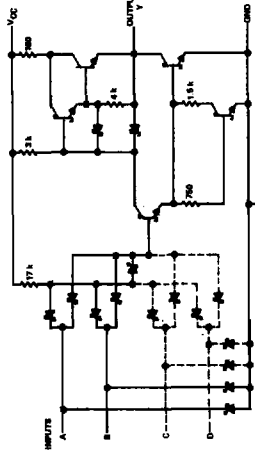
'37, '40, '440 CIRCUITS

	'37	'40	'440
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k

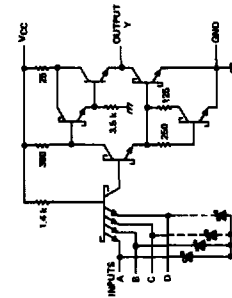


SLURP CIRCUITS

Resistor values shown are nominal and in ohms.



'1537 '1540 CIRCUITS



•\$37. 'S40 CIRCUITS

50-OHM/75-OHM LINE DRIVERS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74		SERIES 54S SERIES 74S		UNIT
		MIN	NOM	MAX	MIN	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5
	74 Family	4.75	5	5.25	4.75	5
High-level output current, I_{OH}	54 Family	-29		-40		mA
	74 Family	-42.4		-40		mA
Low-level output current, I_{OL}					60	mA
Operating free-air temperature, T_A	54 Family	-55	125		-55	125
	74 Family	0	70		0	70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74		SERIES 54S SERIES 74S		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage	1, 2				2			V
V_{IL} Low-level input voltage	1, 2							V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = \S$						V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -2.4 \text{ mA}$		2.4	3.4			V
		$V_{CC} = \text{MIN}, V_{IL} = 0.4 \text{ V}, I_{OH} = -13.2 \text{ mA}$		2.4	3.4			
		$V_{CC} = \text{MIN}, V_{IL} = 0.4 \text{ V}, I_{OH} = \text{MAX}$		2				
		$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$				2.5	3.4	
		$V_{CC} = \text{MIN}, V_{IL} = 0.5 \text{ V}, R_O = 50 \Omega \text{ to GND}$				2.7	3.4	
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = \text{MAX}$		0.26	0.4		0.5	V
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		1	mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$			40			μA
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$			-1.6			mA
I_{OS} Short-circuit output current†	6	$V_{CC} = \text{MAX}$		-70	-180	-50	-225	mA
I_{CC} Supply current	7	Total, outputs high		12	21	10	18	mA
		Average per gate		33	57	25	44	
		$V_{CC} = 5 \text{ V}, 50\% \text{ duty cycle}$		5.63		8.75		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ $I_I = -12 \text{ mA}$ for '128 and -18 mA for 'S140.

¶ Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

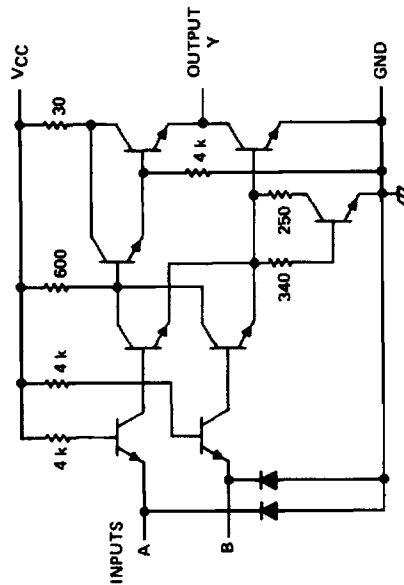
50-OHM/75-OHM LINE DRIVERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		MIN	TYP	MAX	TYP
'128	$C_L = 50\text{ pF}$, $R_L = 133\ \Omega$	6	9	8	12
	$C_L = 150\text{ pF}$, $R_L = 133\ \Omega$	10	15	12	18
'S140	$C_L = 50\text{ pF}$, $R_L = 93\ \Omega$	4	6.5	4	6.5
	$C_L = 150\text{ pF}$, $R_L = 93\ \Omega$	6		6	

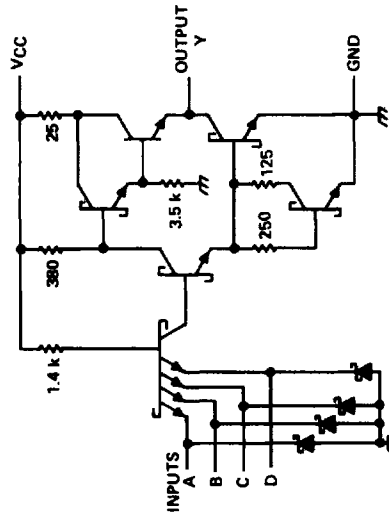
#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each driver)



'128 CIRCUITS

Resistor values shown are nominal and in ohms.



'S140 CIRCUITS

SERIES 54/74

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54' SERIES 74'										UNIT		
		'06, '07		'16, '17		'26		'33, '38						
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX				
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	5	5.5	V	
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}				30			15			15			5.5	V
	54 Family			30			30			16			48	mA
Low-level output current, I_{OL}	74 Family			40			40			18			48	mA
Operating free-air temperature, T_A	54 Family	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	°C
	74 Family	0	70	0	70	0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54' SERIES 74'										UNIT
			'06, '07		'16, '17		'26		'33, '38				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V _{IH} High-level input voltage	1, 2		2			2			2			V	
V _{IL} Low-level input voltage	1, 2											V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = -12 mA			0.8			0.8			0.8	0.8 V	
I _{OH} High-level output current	1	V _{CC} = MIN, V _I = Δ						-1.5			-1.5	V	
		V _{OH} = 12 V									50		
		V _{OH} = MAX			250			250			1000	μA	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = Δ			0.4			0.4			0.4	V	
		I _{OL} = 16 mA											
		I _{OL} = MAX			0.7			0.7			0.4	0.4 V	
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V			1			1			1	mA	
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V			40			40			40	μA	
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.4 V										mA	
I _{CC} Supply current	7	V _{CC} = MAX			-1.8			-1.8			-1.8	mA	

See table on next page

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ The input voltage is $V_{IH} = 2 \text{ V}$ or $V_{IL} = V_{IL} \text{ max}$, as appropriate. See tables with test figures 1 and 2.

See table on next page

SERIES 54/74 **BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t _{PLH} (ns)		t _{PHL} (ns)	
		TYP	MAX	TYP	MAX
'06, '16	$C_L = 15\text{ pF}$, $R_L = 110\ \Omega$	10	15	15	23
'07, '17		6	10	20	30
'26	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$	16	24	11	17
'33	$C_L = 50\text{ pF}$, $R_L = 133\ \Omega$	10	15	12	18
'38	$C_L = 150\text{ pF}$, $R_L = 133\ \Omega$	15	22	16	24
	$C_L = 45\text{ pF}$, $R_L = 133\ \Omega$	14	22	11	18

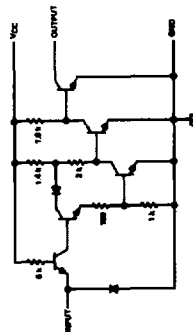
Load circuit and voltage waveforms are shown on page 3-10.

supply current[†]

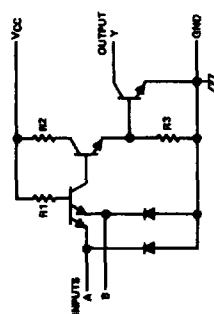
TYPE	I _{CCH} (mA)		I _{CCL} (mA)		I _{CC} (mA)	
	TYP	MAX	TYP	MAX	TYP	MAX
'06, '16	30	48	32	51	5.17	
'07, '17	29	41	21	30	4.17	
'26	4	8	12	22	2.00	
'33	12	21	33	57	5.63	
'38	5	8.5	34	54	4.88	

† Maximum values of I_{CC} shown are over the recommended operating range of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)

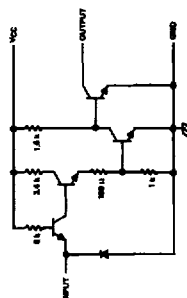


'06, '16 CIRCUITS

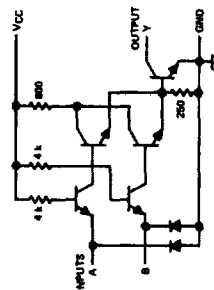


'26, '36 CIRCUITS

CIRCUITS	R1	R2	R3
'26	4 k Ω	1.5 k Ω	1 k Ω
'36	4 k Ω	600 Ω	400 Ω



'07, '17 CIRCUITS



'33 CIRCUITS

SERIES 54LS/74LS AND SERIES 54S/74S BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54LS [†] SERIES 74LS [†]						SERIES 54S [‡] SERIES 74S [‡]			UNIT		
		'LS26		'LS33		'LS38		'S38					
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	5	5.5	
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
High-level output voltage, V _{OH}	54 Family			15			5.5			5.5			5.5
	74 Family			4			12			60			12
Low-level output current, I _{OL}	54 Family			8			24			24			80
	74 Family			8			24			24			80
Operating free-air temperature, T _A	54 Family	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125
	74 Family	0	70	0	70	0	70	0	70	0	70	0	70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54LS [†] SERIES 74LS [†]						SERIES 54S [‡] SERIES 74S [‡]		UNIT
			'LS26		'LS33		'LS38		'S38		
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	
V _{IH} High-level input voltage	1, 2		2		2		2		2		V
V _{IL} Low-level input voltage	1, 2			0.7	0.7			0.7		0.8	V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 8		0.8	0.8			0.8		0.8	V
I _{OH} High-level output current	1	V _{CC} = MIN, V _I = Δ		50	50					-1.2	V
				1000	250			250		250	μA
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = Δ		0.25	0.4			0.25	0.4	0.5	V
		I _{OL} = 4 mA		0.35	0.5			0.35	0.5	0.5	
		I _{OL} = 12 mA		0.25	0.4			0.25	0.4		
I _I Input current at maximum input voltage	4	V _{CC} = MAX								1	mA
I _{IH} High-level input current	4	V _{CC} = MAX		0.1	0.1			0.1			
I _{IL} Low-level input current	5	V _{CC} = MAX		20	20			20		100	μA
I _{CC} Supply current	7	V _{CC} = MAX		-0.4	-0.4			-0.4		-4	mA
											mA

See table on next page

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] I_I = -18 mA for SN54LS/SN74LS and -12 mA for SN54S/SN74S.

[¶] The input voltage is V_{IH} = 2 V or V_{IL} = V_{IH} max, as appropriate. See tables with test figures 1 and 2.

See table on next page

SERIES 54LS/74LS AND SERIES 54S/74S BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		Typ	Max	Typ	Max
'LS26	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	17	32	15	28
'LS33	$C_L = 45\text{ pF}$, $R_L = 687\text{ }\Omega$	20	32	18	28
'LS38	$C_L = 50\text{ pF}$	6.5	10	6.5	10
'S38	$R_L = 93\text{ }\Omega$	9		8.5	

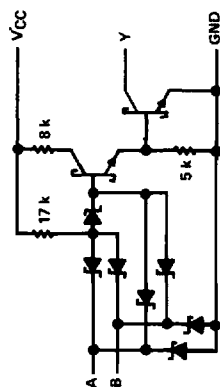
Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

supply current[†]

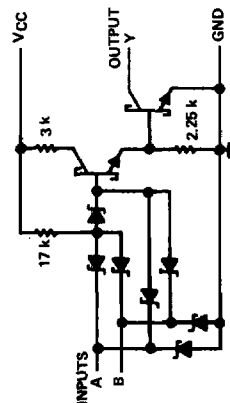
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	Typ	Max	Typ	Max	Typ	Max
'LS26	0.8	1.6	2.4	4.4	0.4	
'LS33	1.8	3.6	6.9	13.8	1.09	
'LS38	0.9	2	6	12	0.88	
'S38	20	36	46	80	8.25	

[†] Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

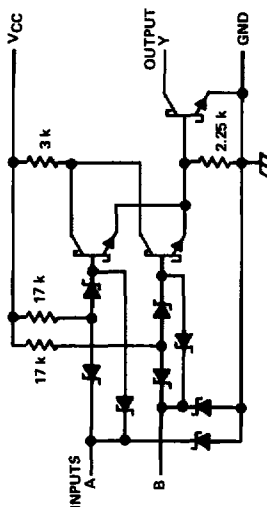
schematics (each gate)



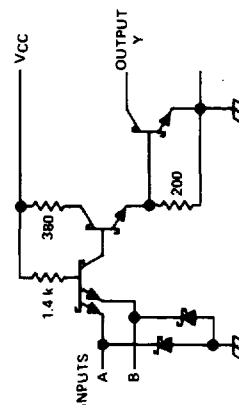
'LS26 CIRCUITS



'LS38 CIRCUITS



'LS33 CIRCUITS



'S38 CIRCUITS

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage, V_{CC}	54 Family 74 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.25	V
High-level output current, I_{OH}	54 Family 74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Low-level output current, I_{OL}	54 Family 74 Family			-800			-400			-1000	μ A
Operating free-air temperature, T_A	54 Family 74 Family	-55	125		-55	125		-55	125		$^{\circ}$ C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH} High-level input voltage	1, 2	54 Family 74 Family	2		0.8	2		0.7	2		0.8	V
V_{IL} Low-level input voltage	1, 2	54 Family 74 Family			0.8			0.8			0.8	V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}$, $I_I = 5$			-1.5			-1.5			-1.2	V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}$, $V_{IH} = 2$ V, $I_{OH} = \text{MAX}$	2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL \text{ max}}$	0.2	0.4		0.25	0.4		0.25	0.4		V
I_I Input current at maximum input voltage	4	$V_I = 5.5$ V, $V_I = 7$ V			1			0.1			1	mA
I_{IH} High-level input current	4	$V_{IH} = 2.4$ V			40			20			50	μ A
I_{IL} Low-level input current	5	$V_{IL} = 0.4$ V			-1.6			-0.4			-2	mA
I_{OS} Short-circuit output current ⁶	6	$V_{CC} = \text{MAX}$	-20	-55		-20	-55		-40	-100		mA
I_{CC} Supply current	7	Total output high	15	22		3.1	6.2		18	32		mA
		Average per gate	23	38		4.9	9.8		38	68		mA
		$V_{CC} = 5$ V, 50% duty cycle	4.75			1.0			7			

¹For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

²All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

³ $I_I = -12$ mA for SN64/SN74⁺ and -18 mA for SN64LS/SN74LS⁺ and SN64S/SN74S⁺.

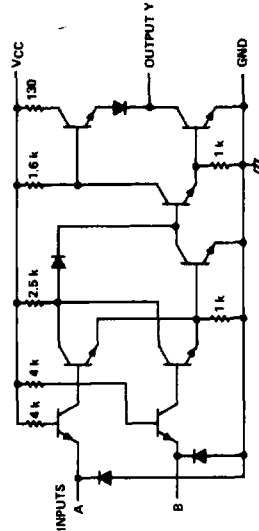
⁶Not more than one output should be shorted at a time, and for SN64LS/SN74LS⁺ and SN64S/SN74S⁺, duration of the short-circuit should be less than one second.

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

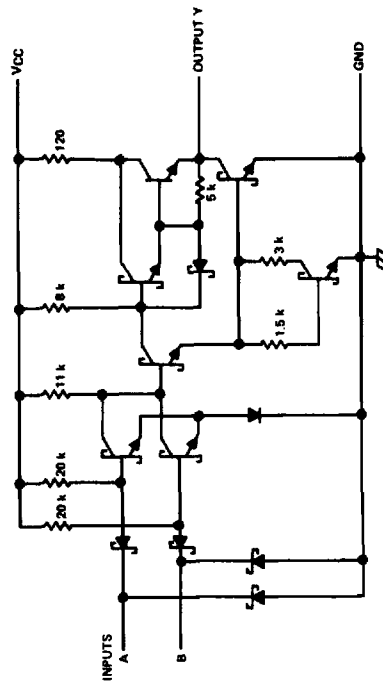
schematics (each gate)

TYPE	TEST CONDITIONS#	t_{pLH} (ns)		t_{pHL} (ns)	
		MIN	TYP	MAX	MIN
'32	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	15	14	22
'LS32	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$	14	22	14	22
'S32	$C_L = 15 \text{ pF}$, $R_L = 280 \Omega$	4	7	4	7
	$C_L = 50 \text{ pF}$, $R_L = 280 \Omega$	5		5	

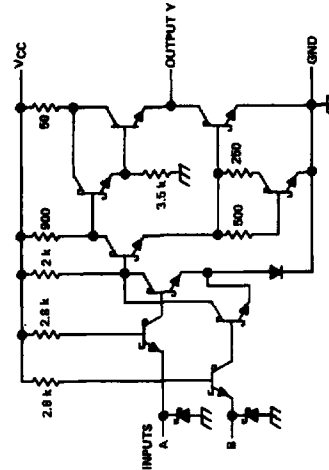
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.



'32 CIRCUITS



'LS32 CIRCUITS



'S32 CIRCUITS

Resistor values shown are nominal and in ohms.

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	74 FAMILY	SERIES 54 SERIES 74	SERIES 54H SERIES 74H	SERIES 54L SERIES 74L	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5
	74 Family	4.75	5	5.25	4.75	5	5.25
High-level output current, I_{OH}	54 Family	-400			-100		
	74 Family	-400			-200		
Low-level output current, I_{OL}	54 Family	16			2		
	74 Family	16			3.6		
Operating free-air temperature, T_A	54 Family	-55	125	-55	125	-55	125
	74 Family	0	70	0	70	0	70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	TEST CONDITIONS ¹												UNIT	
			SERIES 54		SERIES 54H		SERIES 54L		SERIES 54LS		SERIES 54S					
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	MIN	TYP ²	MAX	MIN	TYP ²	MAX		
V _{IH}	High-level input voltage	1, 2	2			0.8			0.8			0.7			0.8	V
V _{IL}	Low-level input voltage	1, 2				0.8			0.8			0.7			0.8	V
V _{IK}	Input clamp voltage	3				-1.5			-1.5			-1.5			-1.2	V
V _{OH}	High-level output voltage	1	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4
			2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4
V _{OL}	Low-level output voltage	2				0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4
						0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5
I _I	Input current at maximum input voltage	4				1			1			0.1			0.1	1
						40			50			10			0.1	1
I _{IH}	High-level input current	4				V _{IH} = 2.4 V			V _{IH} = 2.7 V			10			20	50
						V _{IH} = 2.7 V			V _{IH} = 0.3 V			-0.18			-0.4	50
I _{IL}	Low-level input current	5				V _{IL} = 0.4 V			V _{IL} = 0.5 V			-2			-0.4	50
						V _{IL} = 0.5 V			V _{IL} = 0.3 V			-0.18			-0.4	50
I _{OS}	Short-circuit output current ³	6				-20	-55		-40	-100		-3	-15		-100	-40
						-18	-65		-40	-100		-3	-15		-100	-40
I _{CC}	Supply current	7														mA

See table on next page

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

³ $I_{IH} = -12$ mA for SN54/SN74¹, -8 mA for SN54H/SN74H¹, and -18 mA for SN54LS/SN74LS¹ and SN54S/SN74S¹.

⁴ Not more than one output should be shorted at a time, and for SN54LS/SN74LS¹, SN54H/SN74H¹, and SN54S/SN74S¹, duration of the short-circuit should not exceed one second.

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS*	Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output	
		MIN	TYP	MAX	TYP
'51, '54	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	13	22	8	15
'H51	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$	6.8	11	8.2	11
'H54	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$	7	11	8.2	11
'L51, 'L54, 'L55	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$	50	90	35	60
'LS51, 'LS55	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	12	20	12.5	20
'LS54	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	12	20	12.5	20
'S51, 'S54	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	3.5	5.5	3.5	5.5
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$	5		5.5	

*Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

supply current†

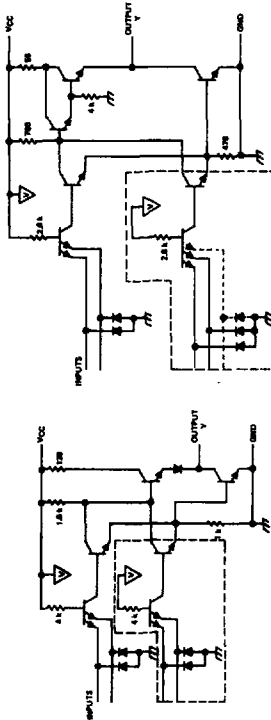
TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per AOI gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'51	4	8	7.4	14	2.85	
'54	4	8	5.1	9.5	4.55	
'H51	8.2	12.8	15.2	24	5.85	
'H54	7.1	11	9.4	14	8.25	
'L51	0.44	0.8	0.76	1.3	0.30	
'L54	0.38	0.8	0.60	0.99	0.50	
'L55	0.22	0.4	0.38	0.65	0.30	
'LS51	0.8	1.6	1.4	2.8	0.55	
'LS54	0.8	1.6	1.0	2	0.9	
'LS55	0.4	0.8	0.7	1.3	0.55	
'S51	8.2	17.8	13.6	22	5.45	
'S54	7	12.5	8.5	16	7.75	

†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

schematics (each gate)

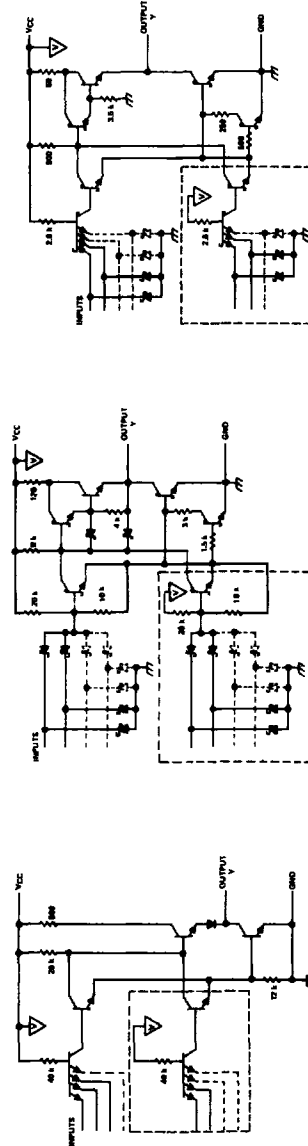
The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

Resistor values shown are nominal and in ohms.



'51, '54 CIRCUITS

'H51, 'H54 CIRCUITS



'L51, 'L54, 'L55 CIRCUITS

'S51, 'S54 CIRCUITS

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN64865			SN74S95			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	'S85			UNIT
			MIN	TYP	MAX	
V_{IH} High-level input voltage	1, 2		2			V
V_{IL} Low-level input voltage	1, 2				0.8	V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_{IH} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250	μA
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IL} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{CCH} Supply current, output high	7	$V_{CC} = \text{MAX}$			6	mA
I_{CCL} Supply current, output low	7	$V_{CC} = \text{MAX}$			8.5	mA

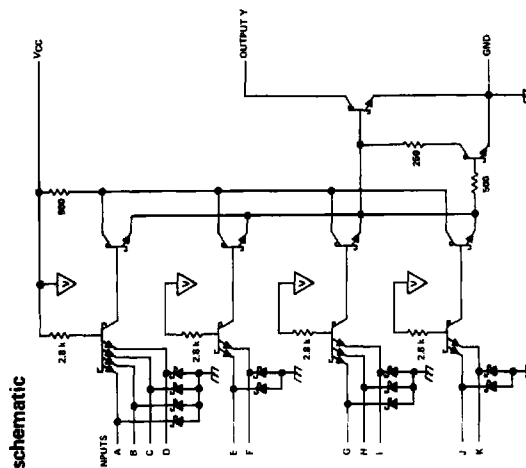
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS#	'S85			UNIT
		MIN	TYP	MAX	
Propagation delay time, t_{PLH} low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5	7.5	ns
Propagation delay time, t_{PHL} high-to-low-level output	$C_L = 50 \text{ pF}, R_L = 280 \Omega$	2	5.5	8.5	ns
	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5.5	8.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$	2	5.5	8.5	ns

Load circuit and voltage waveforms are shown on page 3-10.



Resistor values shown are nominal and in ohms.

GATES WITH 3-STATE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
Supply voltage, V_{CC}		MIN NOM MAX '126, '126, '426, '426	MIN NOM MAX '126A, '126A, '126A	MIN NOM MAX '5134	
High-level output current, I_{OH}	54 Family	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	V
	74 Family	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	V
	54 Family	-2	-2	-2	mA
Low-level output current, I_{OL}	54 Family	-5.2	-2.8	-2.8	mA
	74 Family	-18	-12	-20	mA
	54 Family	-55	-125	-125	mA
Operating free-air temperature, T_A	74 Family	0 70 70	0 70 70	0 70 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74	SERIES 54LS SERIES 74LS	SERIES 54S SERIES 74S	UNIT
V_{IH} High-level input voltage	1, 2		MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
V_{IL} Low-level input voltage	1, 2		MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN.}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
V_{OH} High-level output voltage	1	$V_{IH} = 2 \text{ V, } I_{OH} = \text{MAX}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
V_{OL} Low-level output voltage	2	$V_{IL} = 2 \text{ V, } I_{OL} = \text{MAX}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	V
I_{OZ} Off-state (high-impedance state) output current	19	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	µA
I_I Input current at maximum input voltage	4	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	µA
I_{IH} High-level input current	4	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	µA
I_{IL} Low-level input current	5	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	µA
I_{OS} Short-circuit output current‡	6	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA
I_{CC} Supply current	7	$V_{IH} = 2 \text{ V, } V_{IL} = V_{IL \text{ max}}$	MIN TYP‡ MAX 2 0.8 0.8	MIN TYP‡ MAX 2 0.7 0.8	MIN TYP‡ MAX 2 0.8 0.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V, } T_A = 25^\circ \text{C}$.

§ $I_I = -12 \text{ mA}$ for SN54/SN74 and -18 mA for SN64LS/SN74LS and SN54S/SN74S.

¶Not more than one output should be shorted at a time, and for SN64LS/SN74LS and SN54S/SN74S, duration of the short circuit should not exceed one second.

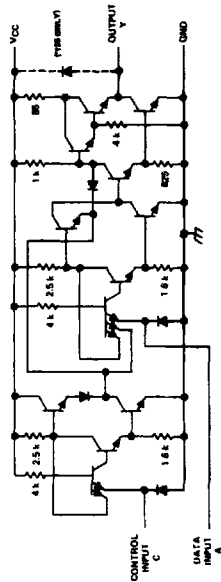
GATES WITH 3-STATE OUTPUTS

supply current[†]

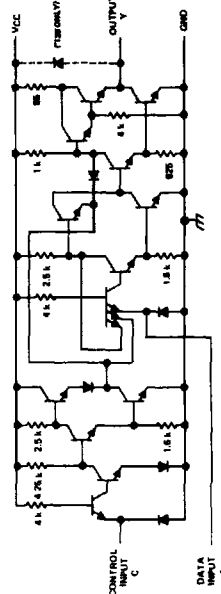
TYPE	TEST CONDITIONS		I _{CC} (mA)	
	DATA INPUTS	OUTPUT CONTROLS	MIN	MAX
'125, '425	0 V	4.5 V	32	54
'126, '426	0 V	0 V	36	62
'LS125A	0 V	4.5 V	11	20
'LS126A	0 V	0 V	12	22
	0 V	0 V	7	13
	5 V	0 V	9	16
'S134	5 V	5 V	14	25

[†]Maximum values of I_{CC} are over the recommended operating range of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



'125A, '425 CIRCUITS



'126A, '426 CIRCUITS

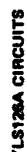
Resistor values shown are nominal and in ohms.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	SERIES 64/74				SERIES 64LS/74LS				SERIES 64S/74S			
	TEST CONDITIONS#	'125, '425		TYP MAX	TEST CONDITIONS#	'LS126A		TYP MAX	TEST CONDITIONS#	'S134		UNIT
		8	13			9	15			4	6	
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 50 pF, R _L = 400 Ω	12	18	18	C _L = 45 pF, R _L = 687 Ω	7	18	18	C _L = 15 pF, R _L = 280 Ω	5	5.5	ns
t _{PHL} Propagation delay time, high-to-low-level output		11	17	11		12	20	16		5	7.5	
t _{PZH} Output enable time to high level	C _L = 5 pF, R _L = 400 Ω	18	26	16	C _L = 5 pF, R _L = 687 Ω	15	25	21	C _L = 50 pF, R _L = 280 Ω	14	21	ns
t _{PZL} Output enable time to low level		5	8	10		20	20	25		5.5	8.5	
t _{PHZ} Output disable time from high level	C _L = 5 pF, R _L = 400 Ω	7	12	12		20	20	25	C _L = 5 pF, R _L = 280 Ω	9	14	ns
t _{PLZ} Output disable time from low level												

#Load circuit and voltage waveforms are shown on page 3-10 and 3-11.

schematics (each gate)



6-35

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

		64 FAMILY 74 FAMILY	SERIES 64 SERIES 74		SERIES 64LS SERIES 74LS		UNIT
			'368A, '368A '367A, '368A	MIN NOM MAX	'LS368A, 'LS368A 'LS367A, 'LS368A	MIN NOM MAX	
Supply voltage, VCC		64 Family 74 Family	4.5 5 5.5 4.75 5 5.25	4.5 5 5.5 4.75 5 5.25	5 5.5 5 5.25	5 5.5 5 5.25	V
High-level output current, I _{OH}		64 Family 74 Family	-2 -2.6	-2 -2.6	-1 -1	-1 -1	mA
Low-level output current, I _{OL}		64 Family 74 Family	32 32	32 32	12 12	12 12	mA
Operating free-air temperature, T _A		64 Family 74 Family	-55 0	-55 0	-55 0	-55 0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 64 SERIES 74		SERIES 64LS SERIES 74LS		UNIT
			'368A, '368A '367A, '368A	MIN TYP ² MAX	'LS368A, 'LS368A 'LS367A, 'LS368A	MIN TYP ² MAX	
V _{IH} High-level input voltage	1, 2			2		2	V
V _{IL} Low-level input voltage	1, 2			0.8		0.7	V
V _{IK} Input clamp voltage	3	VCC = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX		0.8		0.8	V
V _{OH} High-level output voltage	1	VCC = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA	2.4 3.3 2.4 3.3	2.4 3.3 2.4 3.3	2.4 3.3 2.4 3.3	2.4 3.3 2.4 3.3	V
V _{OL} Low-level output voltage	2	VCC = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA		0.4		0.4	V
I _{OZ} Off-state (high-impedance state) output current	19	VCC = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max		40		20	μA
I _I Input current at maximum input voltage	4	VCC = MAX		-40		-20	μA
I _{IH} High-level input current	4	VCC = MAX		40		20	μA
I _{IL} Low-level input current	A inputs	VCC = MAX, V _I = 0.5 V, Either G input at 2 V		-40		-20	μA
I _{IS} Short-circuit output current ³	G inputs	VCC = MAX, V _I = 0.4 V, Both G inputs at 0.4 V		-1.6		-0.4	mA
I _{CC} Supply current		VCC = MAX		-40		-225	mA

¹For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

²All typical values are at VCC = 5 V, T_A = 25°C.

³I_I = -12 mA for SN64/SN74 and -18 mA for SN64LS/SN74LS and SN64/SN74S.

†Not more than one output should be shorted at a time, and for SN64LS/SN74LS and SN64/SN74S, duration of output short-circuit should not exceed one second.

supply current[†]

TYPE	DATA INPUTS	OUTPUT CONTROLS	I _{CC} (mA)
		TYP	MAX
'385A, '387A	0 V	4.5 V	66
'385A, '388A	0 V	4.5 V	66
'LS385A, 'LS387A	0 V	4.5 V	14
'LS385A, 'LS388A	0 V	4.5 V	12

[†] Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

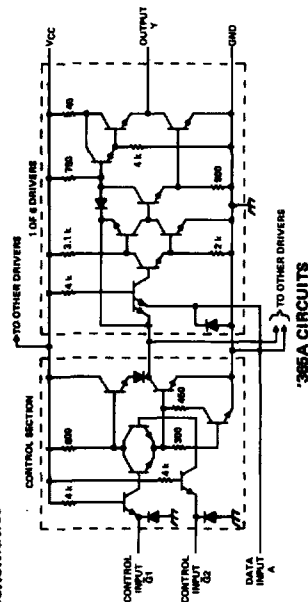
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 1

PARAMETER*	TEST CONDITIONS	SERIES 94L874LS		SERIES 94L874LS	
		'385A, '387A TYP	'385A, '388A MAX	'LS385A, 'LS387A TYP	'LS385A, 'LS388A MAX
t _{PLH}	C _L = 50 pF, R _L = 400 Ω	18	17	10	7
t _{PHL}		22	18	9	12
t _{PZH}		35	35	19	35
t _{PZL}	C _L = 5 pF, R _L = 400 Ω	37	37	24	28
t _{PLZ}		11	11	30	32
t _{PHZ}		27	27	35	35

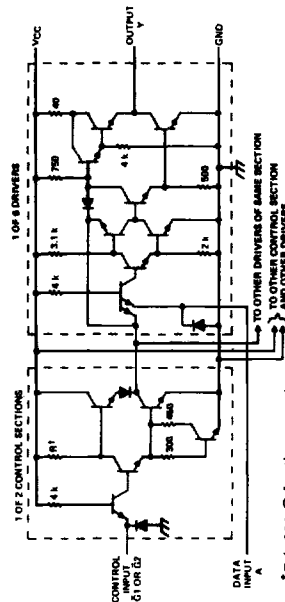
*t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output disable time to low level
t_{PLZ} = Output enable time to low level
t_{PHZ} = Output disable time from high level

NOTE 1: Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics

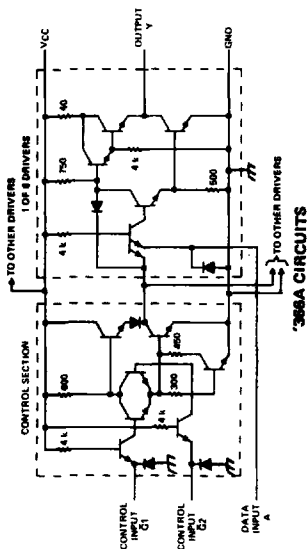


'385A CIRCUITS

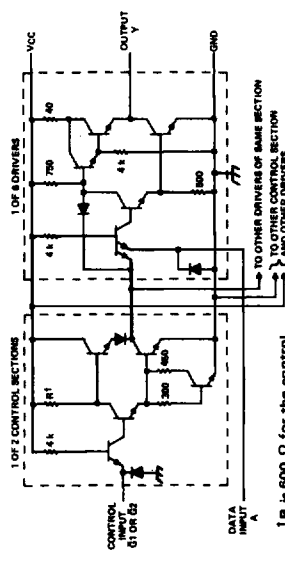


'387A CIRCUITS

[†] R_L is 600 Ω for the control section associated with G₁ and 900 Ω for the control section associated with G₂.



'386A CIRCUITS

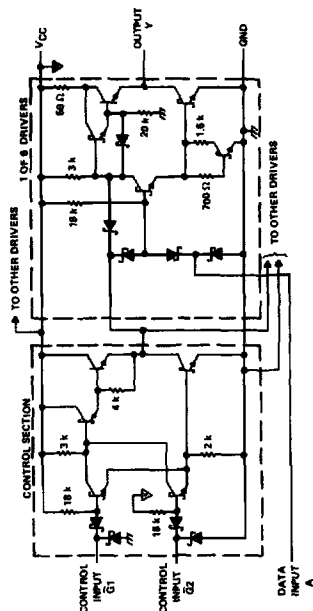


'388A CIRCUITS

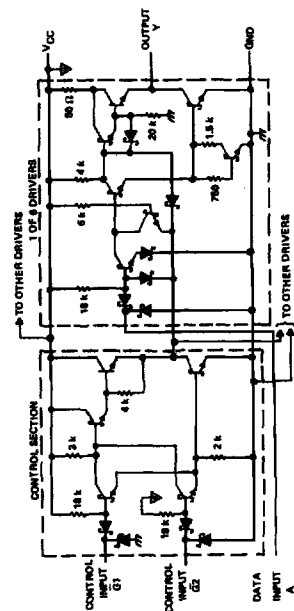
[†] R_L is 600 Ω for the control section associated with G₁ and 900 Ω for the control section associated with G₂.

Resistor values shown are nominal and in ohms.

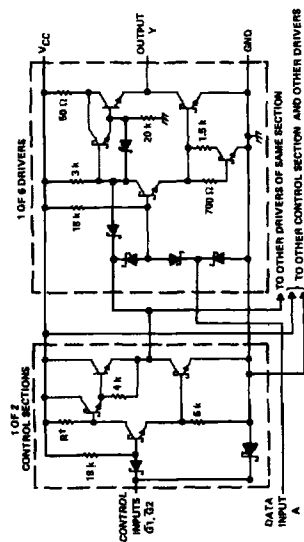
HEX BUS DRIVERS WITH 3-STATE OUTPUTS



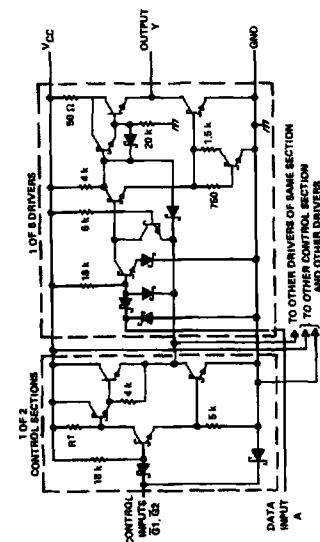
'LS366A CIRCUITS



'LS366A CIRCUITS



'LS368A CIRCUITS



'LS367A CIRCUITS

[†]R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with G2.

Resistor values shown are nominal and in ohms

EXPANDABLE GATES

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H						UNIT
		'23			'50, '53			'H50, 'H52, 'H53, 'H55						
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5		V	
High-level output current, I_{OH}		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25		μ A	
Low-level output current, I_{OL}		54 Family				16		16					mA	
Operating free-air temperature range, T_A		74 Family				16		16					$^{\circ}$ C	
		54 Family	-55		125	-55		125	-55		125		$^{\circ}$ C	
		74 Family	0	0	70	0	0	70	0	0	70		$^{\circ}$ C	

The '23, '50, and '53 are designed for use with up to four '60 expanders.

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74				SERIES 54H SERIES 74H				UNIT
			'23		'50, '53		'H50, 'H52 'H53, 'H55				
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	
V _{IH} High-level input voltage	1, 2		2		0.8		0.8		0.8		V
V _{IL} Low-level input voltage	1, 2				-1.5		-1.5		-1.5		V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 5									V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _I = A, I _{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = A, I _{OL} = MAX	0.2	0.4		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V			1		1		1		mA
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V			40		40		50		μA
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.4 V			-1.6		-1.6		-2		mA
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	-20	-55	-6.4	-20	-55	-40	-100		mA
I _{CC} Supply current	7	V _{CC} = MAX	-18	-55	-6.4	-18	-55	-40	-100		mA
See table on next page											

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] $I_I = -12 \text{ mA}$ for SN54/SN74[†] and -8 mA for SN54H/SN74H[†].

[¶]The input voltage is $V_{IH} = 2 \text{ V}$ or $V_{IL} = V_{IL} \text{ max}$, as appropriate. See tables with test figures 1 and 2.

[¶]Not more than one output should be shorted at a time, and for the SN54H/SN74H[†], duration of short-circuit should not exceed one second.

EXPANDABLE GATES

electrical characteristics using expander inputs, $V_{CC} = \text{MIN}$, $T_A = \text{MIN}$ (unless otherwise noted)

TYPE	I_{IX} (mA) (I_X for 'H62) Expander current		$V_{BE(Q)}$ (V) Base-emitter voltage of output transistor Q		V_{OH} (V) High-level output voltage		V_{OL} (V) Low-level output voltage	
	TEST CONDITIONS	MIN	TYP [†]	MAX	TEST CONDITIONS	MIN	TYP [†]	MAX
SN5423	$V_{IX} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$, See Figure 10	-3.5			$I_X = 160 \mu\text{A}$, $I_{IX} = -150 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	3.4	0.2 0.4
SN5450		-2.9						
SN5453		-2.9						
SN7423	$V_{IX} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$, See Figure 10	-3.8			$I_X = 270 \mu\text{A}$, $I_{IX} = -270 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	3.4	0.2 0.4
SN7450		-3.1						
SN7453		-3.1						
SN54H50	$V_{IX} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10	-5.85			$I_X = 320 \mu\text{A}$, $I_{IX} = -320 \mu\text{A}$, $I_{OH} = -500 \mu\text{A}$, See Figure 12	2.4	3.4	0.2 0.4
SN54H53								
SN54H55								
SN74H50	$V_{IX} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10	-6.3			$I_X = 570 \mu\text{A}$, $I_{IX} = -570 \mu\text{A}$, $I_{OH} = -500 \mu\text{A}$, See Figure 12	2.4	3.4	0.2 0.4
SN74H53								
SN74H55								
SN54H52	$V_X = 1 \text{ V}$, $I_{OH} = -500 \mu\text{A}$, See Figure 13	-2.7	-4.5		$V_X = 1 \text{ V}$, $I_{OH} = -500 \mu\text{A}$, See Figure 13	2.4	3.4	0.2 0.4
SN74H52		-2.9	-5.35					

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] R_{IX} equals 114Ω for SN5423, 138Ω for SN5450 and SN5453, 105Ω for SN7423, and 130Ω for SN7450 and SN7453.

supply current[§]

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	
'23	8	16	10	19	4.5	
'50	4	8	7.4	14	2.85	
'53	4	8	5.1	9.5	4.55	
'H50	8.2	12.8	15.2	24	5.85	
'H52	20	31	15.2	24	17.5	
'H53	7.1	11	9.4	14	8.25	
'H55	4.5	6.4	7.5	12	6.00	

[§]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

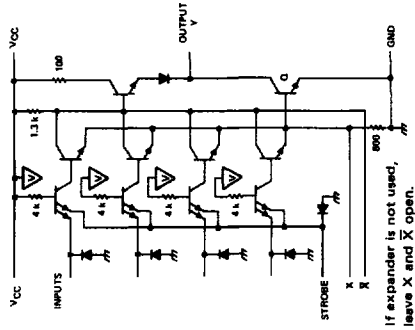
EXPANDABLE GATES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'23, '50, '53	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, Expander pins open	13	22	8	15
'50	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, From input of '50 expander	15	30	10	20
'H50	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, Expander pins open	6.8	11	6.2	11
'H52		10.6	15	9.2	15
'H53		7	11	6.2	11
'H55		7	11	6.5	11
'H50	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, $C = 15\text{ pF}$ (GND to X of	11		7.4	
'H52	'H50, 'H53, or 'H55; or	14.8		9.8	
'H53	to X of 'H52)	11.4		7.4	
'H55		11.4		7.7	

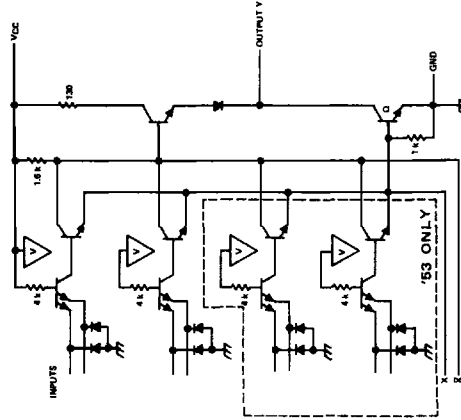
#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each gate)



If expander is not used, leave X and X open.

'23 CIRCUITS

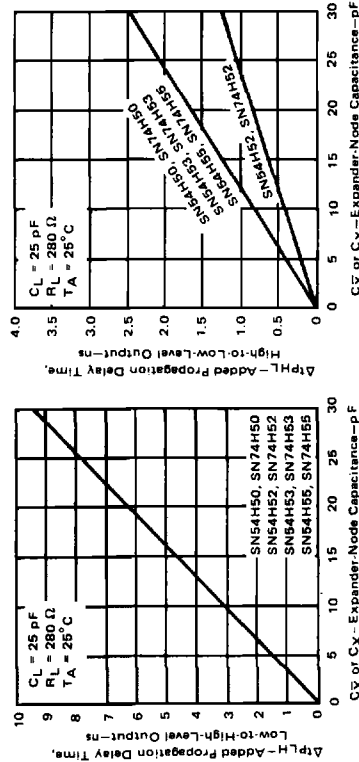


If expander is not used, leave X and X open.

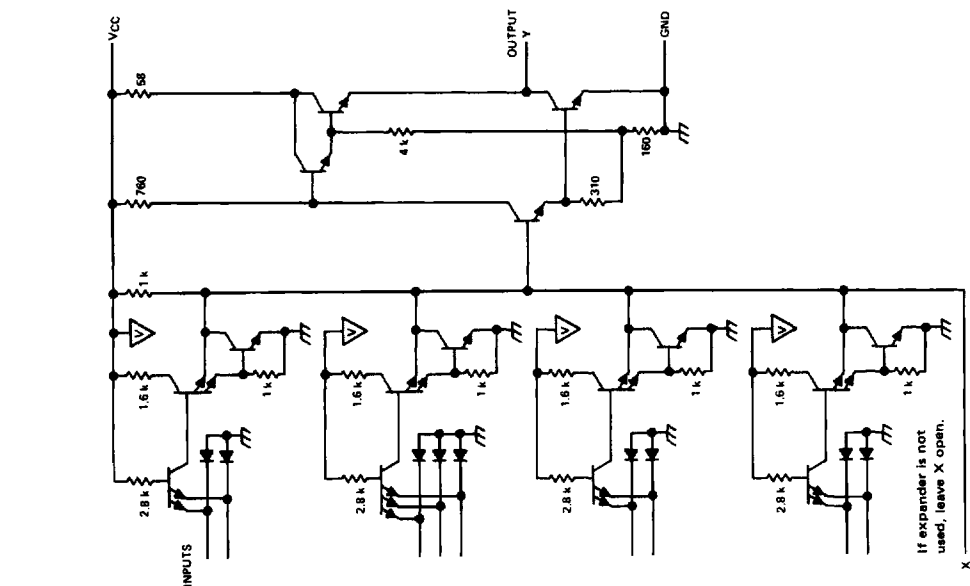
'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.

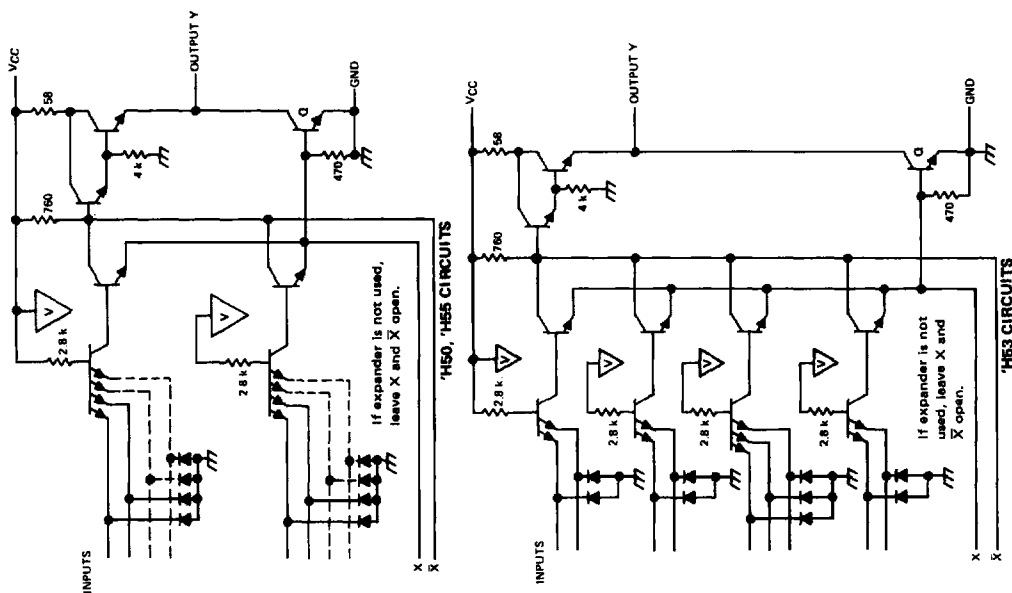
TYPICAL ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE



EXPANDABLE GATES



Resistor values shown are nominal and in ohms.

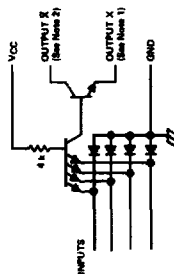


recommended operating conditions

	SN5480			SN7480			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

The '23, '50, and '53 are designed for use with up to four '80 expanders.

schematic (each gate)



'80 CIRCUITS

- NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to X input of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN5480			SN7480			UNIT
		TEST CONDITIONS	MIN	TYP† MAX	TEST CONDITIONS	MIN	TYP† MAX	
V_{IH} High-level input voltage	15							V
V_{IL} Low-level input voltage	16			2		0.8		0.8 V
On-state voltage between $V_{XX}(on)$ expander outputs	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_X = 3.5\text{ mA}$, $T_A = -55^\circ\text{C}$			0.4	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_X = 3.8\text{ mA}$, $T_A = 0^\circ\text{C}$		0.4 V
$I_X(on)$ On-state expander current	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_X = 0$, $T_A = -55^\circ\text{C}$	-0.3			$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_X = 0$, $T_A = 0^\circ\text{C}$	-0.43	mA
$I_X(off)$ Off-state expander current	16	$V_{CC} = 4.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_X = 4.5\text{ V}$, $R_X = 1.2\text{ k}\Omega$, $T_A = -55^\circ\text{C}$			150	$V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_X = 4.5\text{ V}$, $R_X = 1.2\text{ k}\Omega$, $T_A = 0^\circ\text{C}$		μA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$		1		$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$		1 mA
I_{IH} High-level input current	4	$V_{CC} = 5.5\text{ V}$, $V_I = 2.4\text{ V}$		40		$V_{CC} = 5.25\text{ V}$, $V_I = 2.4\text{ V}$		40 μA
I_{IL} Low-level input current	5	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		-1.6		$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$		-1.8 mA
$I_{CC}(on)$ Supply current, expander on	7	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_X = 0$		1.2 2.5		$V_{CC} = 5.25\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_X = 0$	1.2 2.5	mA
$I_{CC}(off)$ Supply current, expander off	7	$V_{CC} = 5.5\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_X = 0$		2 4		$V_{CC} = 5.25\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_X = 0$	2 4	mA

†All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

EXPANDERS

EXPANDERS

recommended operating conditions

	SN54H60 SN54H62		SN74H60 SN74H62		UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55	125	0	0	70	70	°C

See schematics
next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN54H60, SN54H62		SN74H60, SN74H62		UNIT
		TEST CONDITIONS	MIN	TYP [†]	MAX	
V_{IH} High-level input voltage	15		2			V
V_{IL} Low-level input voltage	16			0.8		V
$V_{XX(on)}$ On-state voltage between expander outputs	15	$V_{CC} = 4.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1.1\text{ V}, I_X = 5.85\text{ mA}, T_A = -55^\circ\text{C}$				
		$V_{CC} = 5.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 7.85\text{ mA}, T_A = 125^\circ\text{C}$				
		$V_{CC} = 4.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1.1\text{ V}, I_X = 0, T_A = -55^\circ\text{C}$	-470			μA
		$V_{CC} = 4.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 0, T_A = -55^\circ\text{C}$				
$I_X(on)$ On-state expander current	15					μA
$I_X(off)$ Off-state expander current	16			320		μA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}, V_I = 5.5\text{ V}$		1		mA
I_{IH} High-level input current	4	$V_{CC} = 5.5\text{ V}, V_I = 2.4\text{ V}$		50		μA
I_{IL} Low-level input current	5	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$		-2		mA
$I_{CC(on)}$ Supply current, expander on	'H60	$V_{CC} = 5.5\text{ V}, V_I = 4.5\text{ V}, V_X = 0.85\text{ V}, I_X = 0$		1.9	3.5	mA
	'H62	$V_{CC} = 5.5\text{ V}, V_I = 4.5\text{ V}, V_X = 0.85\text{ V}, I_X = 0$		3.8	7	mA
$I_{CC(off)}$ Supply current, expander off	'H60	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		3	4.5	mA
	'H62	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		6	9	mA
C_X Expander output capacitance	'H60	V_{CC} , inputs, and X open; $f = 1\text{ MHz}$		5.4		pF
	'H62	V_{CC} , inputs, and X open; $f = 1\text{ MHz}$		6.0		pF

[†]All typical values are at $V_{CC} = 5\text{ V}$ (except C_X), $T_A = 25^\circ\text{C}$.

recommended operating conditions

	SN54H61			SN74H61			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

The 'H52 is designed for use with up to six 'H61 expanders.

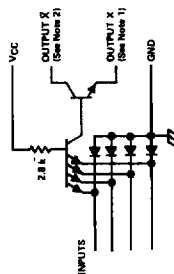
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH} High-level input voltage	17		2			V
V_{IL} Low-level input voltage	18				0.8	V
$V_X(on)$ On-state expander output voltage	17	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_X = 4.5 \text{ mA}$ for SN54H61, 5.35 mA for SN74H61, $T_A = \text{MIN}$			1	V
		$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_X = 2.2 \text{ V}, T_A = \text{MAX}$			50	μA
$I_X(off)$ Off-state expander current	18				1	mA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5 \text{ V}, V_I = 5.5 \text{ V}$			50	μA
I_{IH} High-level input current	4	$V_{CC} = 5.5 \text{ V}, V_I = 2.4 \text{ V}$			-2	mA
I_{IL} Low-level input current	5	$V_{CC} = 5.5 \text{ V}, V_I = 0.4 \text{ V}$			11	mA
$I_{CC(on)}$ Supply current, expander on	7	$V_{CC} = 5.5 \text{ V}, V_I = 4.5 \text{ V}$			5	mA
$I_{CC(off)}$ Supply current, expander off	7	$V_{CC} = 5.5 \text{ V}, V_I = 0$			5.4	pF
C_X Expander output capacitance		V_{CC} and inputs open, $f = 1 \text{ MHz}$				

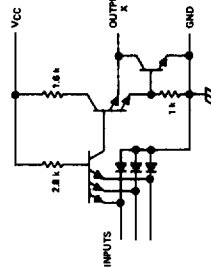
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$ (except C_X). $T_A = 25^\circ\text{C}$.

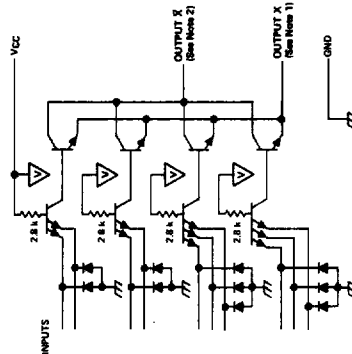
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

NOTES: 1. Connect to X input of 'H50, 'H53, or 'H55 circuit.
2. Connect to X input of 'H50, 'H53, or 'H55 circuit.
Resistor values shown are nominal and in ohms.

SERIES 54/74 FLIP-FLOPS

recommended operating conditions

		SERIES 54/74		'70		'72, '73, '76, '107		'74		'109		'110		'111		UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM		MAX	
Supply voltage, V_{CC}	Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V	
	Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25		
				-400			-400			-400			-900			-800	μ A	
High-level output current, I_{OH}				16			16			16			16			16	mA	
Low-level output current, I_{OL}																		
	Clock high	20		20			30			20			25			25	ns	
	Clock low	30		47			37			20			25			25	ns	
Pulse width, t_w		25		25			30			20			25			25	ns	
	Preset or clear low	20†			0†		20†			10†			20†			0†	ns	
Input setup time, t_{su}		5†		0†			5†			6†			5†			30†	ns	
Input hold time, t_h		-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	°C
Operating free-air temperature, T_A	Series 54	0	70	0	70	0	70	0	70	0	70	0	70	0	70	0	70	°C
	Series 74																	

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'70		'72, '73, '76, '107		'74		'109		'110		'111		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2		0.8	2	0.8	2	0.8	2	0.8	2	0.8	2	V
V _{IL} Low-level input voltage				-1.5		-1.5		-1.5		-1.5		-1.5		V
V _{IK} Input clamp voltage														
V _{OH} High-level output voltage	V _{CC} = MIN, I _L = -12 mA, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1		1	1	1		1		1		1		mA
I _{IH} High-level input current	D, J, K, or $\bar{K}$	40		40	40	40		40		40		40		mA
	Clear	80		80	80	120		160		160		160		mA
	Preset	80		80	80	80		80		80		80		mA
I _{IL} Low-level input current	Clock	-40		-40	-80	-80		-80		-80		-40		mA
	D, J, K, or $\bar{K}$	-1.6		-1.6	-1.6	-1.6		-1.6		-1.6		-1.6		mA
	Clear *	-3.2		-3.2	-3.2	-3.2		-4.8		-3.2		-3.2		mA
I _{IS} Short-circuit output current	Preset *	-3.2		-3.2	-3.2	-3.2		-3.2		-3.2		-3.2		mA
	Clock	-1.6		-3.2	-3.2	-3.2		-3.2		-3.2		-1.6		mA
	Series 54	-20		-20	-57	-57		-30		-20		-20		mA
I _{CC} Supply current (Average per flip-flop)	Series 74	-18		-18	-57	-57		-30		-18		-18		mA
	V _{CC} = MAX, See Note 1	13	26	10	20	8.5	15	9	15	20	34	14	20.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

* Not more than one output should be shorted at a time.

† Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111, and is grounded for all the others.

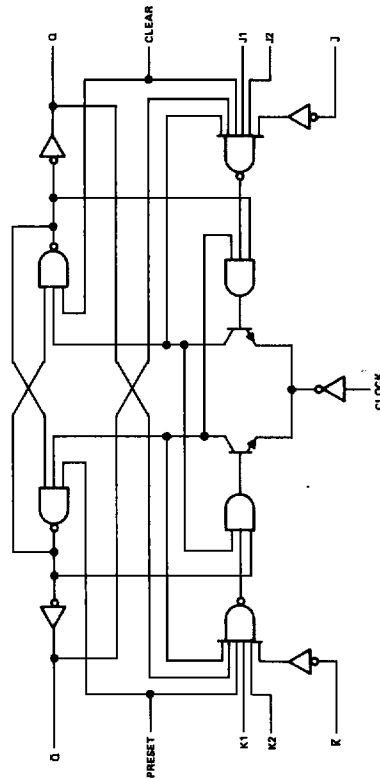
SERIES 54/74 FLIP-FLOPS

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

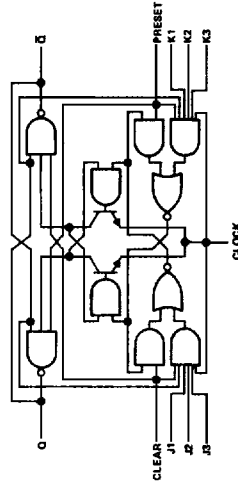
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	70		72, 73 76, 107		74		100		110		111		UNIT
f_{max}				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MHz
t_{PLH}	Preset	Q	$C_L = 15 pF$, $R_L = 400 \Omega$, See Note 2	20	35		15	20	15	25	25	33	20	25	20	ns
t_{PHL}	(as applicable)	$\bar{Q}$		50		16	25	40	23	35	10	15	12	20	12	ns
t_{PLH}	Clear	Q		50		25	40	23	35	10	15	12	20	12	20	ns
t_{PHL}	(as applicable)	$\bar{Q}$		50		25	40	23	35	10	15	12	20	12	20	ns
t_{PLH}	Clock	Q or $\bar{Q}$		27	50	16	25	14	25	10	16	20	30	12	17	ns
t_{PHL}				18	50	25	40	20	40	18	28	13	20	20	30	ns

¹ f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



70—GATED J-K WITH CLEAR AND PRESET



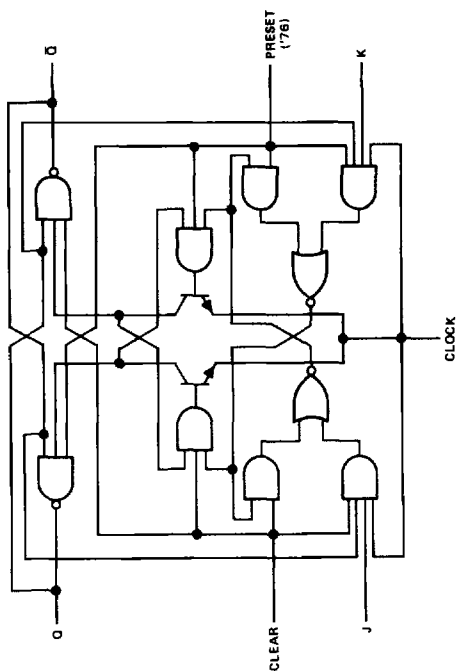
72—GATED J-K WITH CLEAR AND PRESET

See following pages for:
73—DUAL J-K WITH CLEAR
74—DUAL D WITH CLEAR AND PRESET
76—DUAL J-K WITH CLEAR AND PRESET
107—DUAL J-K WITH CLEAR

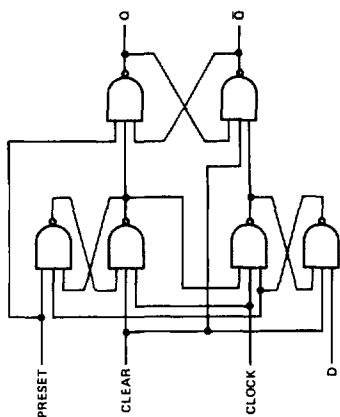
100—DUAL J-K WITH CLEAR AND PRESET
110—GATED J-K WITH CLEAR AND PRESET
111—DUAL J-K WITH CLEAR AND PRESET

SERIES 54/74 FLIP-FLOPS

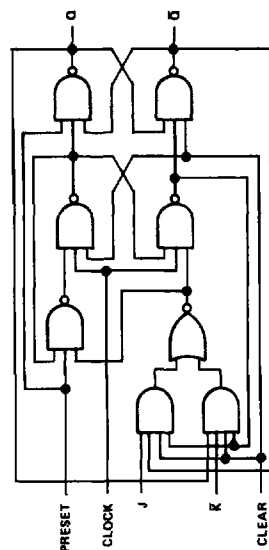
functional block diagrams (continued)



'73-DUAL J-K WITH CLEAR
'76-DUAL J-K WITH CLEAR AND PRESET
'107-DUAL J-K WITH CLEAR

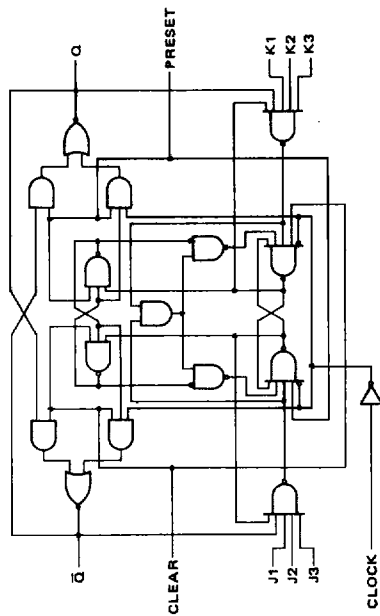


'74-DUAL D WITH CLEAR AND PRESET

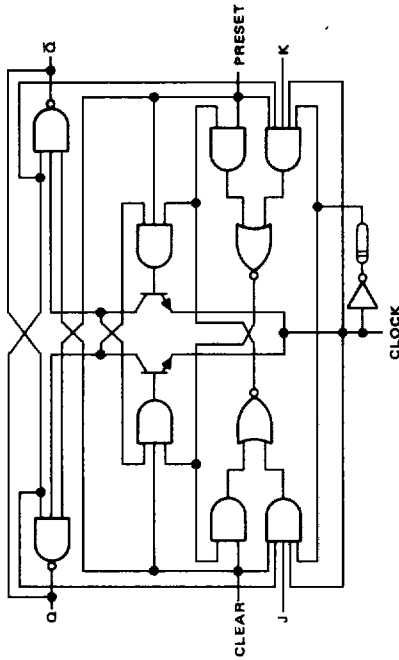


'106-DUAL J-K WITH CLEAR AND PRESET

functional block diagrams (continued)

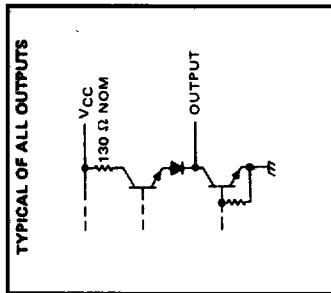
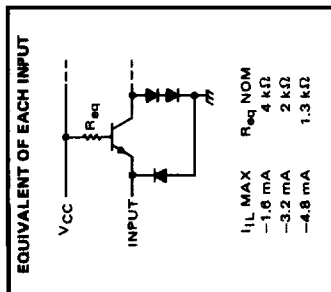


'110-GATED J-K WITH CLEAR AND PRESET



'111-DUAL J-K WITH CLEAR AND PRESET

schematics of inputs and outputs



SERIES 54H/74H PULSE-TRIGGERED J-K AND EDGE-TRIGGERED D-TYPE FLIP-FLOPS

recommended operating conditions

	SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 64H	4.5	6	5.5	4.5	6	5.5	4.5	6	5.5	4.5	6	5.5	V
	Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}				-500			-500			-1000			-500	μ A
Low-level output current, I_{OL}				20			20			20			20	mA
Pulse width, t_w	Clock high			12			12			15			12	
	Clock low			28			28			13.5			28	ns
Clear or preset low				16			16			25			16	
	High-level data			0†			0†			10†			0†	
Setup time, t_{su}				0†			0†			15†			0†	ns
	Low-level data													
Hold time, t_h				0†			0†			5†			0†	ns
Operating free-air temperature, T_A	Series 64H		-55	125		-55	125		-55	125		-55	125	°C
	Series 74H		0	70		0	70		0	70		0	70	

† The arrow indicates the edge of the clock pulse used for reference; † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'H71		'H72, 'H73, 'H76		'H74		'H78		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX
V_{IH} High-level input voltage										
V_{IL} Low-level input voltage										
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$		0.8		0.8		0.8		0.8	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$		-1.5		-1.5		-1.5		-1.5	V
V_{OH} High-level output voltage		2.4	3.4		2.4	3.4		2.4	3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$		0.2	0.4		0.2	0.4		0.2	0.4
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1		1		1	mA
	D, J or K		50		50		50		50	mA
	Clear									
	Preset									
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		150		100		150		100	µA
	Clock		100		50		100		50	µA
	D, J or K		-2		-2		-2		-2	mA
	Clear *		-6		-4		-4		-4	mA
	Preset *		-4		-2		-2		-2	mA
	Clock									
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$	-40	-100	-40	-100	-40	-100	-40	-100	mA
I_{CC} Supply current (Average per flip-flop)	$V_{CC} = \text{MAX},$ See Note 1	19	30	16	25	15	21	16	25	mA
	Series 54H	19	30	16	25	15	21	16	25	mA
	Series 74H	19	30	16	25	15	25	16	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

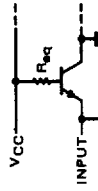
* Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54H/74H PULSE-TRIGGERED J-K AND EDGE-TRIGGERED D-TYPE FLIP-FLOPS

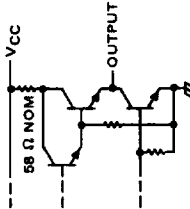
schematics of input and outputs

EQUIVALENT OF EACH INPUT



	I_{IL} MAX	R_{eq} NOM
	-2 mA	2.8 k Ω
	-4 mA	1.4 k Ω
	-6 mA	933 Ω
	-8 mA	700 Ω

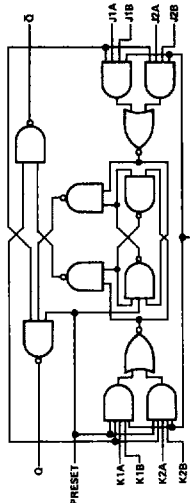
TYPICAL OF ALL OUTPUTS



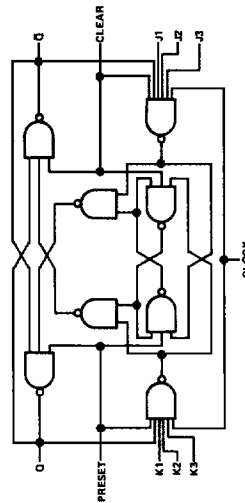
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78		'H74		UNIT
				MIN	TYP	MAX	MIN	
f_{max}	Preset	Q	$C_L = 25$ pF, $R_L = 280$ Ω , See Note 2	25	30	35	43	MHz
t_{PLH}	(as applicable)	$\bar{Q}$		6	13			ns
t_{PHL}	Clear	$\bar{Q}$		12	24			ns
t_{PLH}	(as applicable)	Q		6	13			ns
t_{PHL}	Clock	Q or $\bar{Q}$		12	24			ns
				14	21		8.5	15
				22	27		13	20

¹ f_{max} $\equiv$ maximum clock frequency; tPLH $\equiv$ propagation delay time, low-to-high-level output; tPHL $\equiv$ propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



'H71-GATED J-K WITH PRESET



SERIES 54H/74H EDGE-TRIGGERED J-K FLIP-FLOPS

recommended operating conditions

SERIES 54H/74H		'H101	'H102, 'H106	'H103	'H108	UNIT
		MIN NOM MAX	MIN NOM MAX	MIN NOM MAX	MIN NOM MAX	
Supply voltage, V_{CC}	Series 54H	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	V
	Series 74H	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	V
High-level output current, I_{OH}		-500	-500	-500	-500	μ A
Low-level output current, I_{OL}		20	20	20	20	mA
Pulse width, t_p	Clock high	10	10	10	10	ns
	Clock low	15	15	15	15	ns
	Clear or preset low	16	16	16	16	ns
Setup time, t_{su}	High-level data	10 $\downarrow$	10 $\downarrow$	10 $\downarrow$	10 $\downarrow$	ns
	Low-level data	13 $\downarrow$	13 $\downarrow$	13 $\downarrow$	13 $\downarrow$	ns
Hold time, t_h		0 $\downarrow$	0 $\downarrow$	0 $\downarrow$	0 $\downarrow$	ns
Operating free-air temperature, T_A	Series 54H	-55 125 -55	125 -55 125	-55 125 -55	-55 125 -55	$^{\circ}$ C
	Series 74H	0 70 0	0 70 0	0 70 0	0 70 0	$^{\circ}$ C

$\downarrow$ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'H101	'H102, 'H106	'H103	'H108	UNIT
		MIN TYP‡ MAX	MIN TYP‡ MAX	MIN TYP‡ MAX	MIN TYP‡ MAX	
V_{IH} High-level input voltage		2	0.8	2	0.8	V
V_{IL} Low-level input voltage			-1.5		-1.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$					V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -500 \mu\text{A}$	2.4 3.4	2.4 3.4	2.4 3.4	2.4 3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	0.2 0.4	0.2 0.4	0.2 0.4	0.2 0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1	1	1	1	mA
I_{IH} High-level input current	Any J or K	50	50	50	50	μ A
	Clear					
	Preset	100	100	100	100	μ A
I_{IL} Low-level input current	Any J or K	0	0	0	0	mA
	Clear	-1 -2	-1 -2	-1 -2	-1 -2	mA
	Preset	-1 -2	-1 -2	-1 -2	-1 -2	mA
I_{OS} Short-circuit output current‡		-3 -4.8	-3 -4.8	-3 -4.8	-3 -4.8	mA
I_{CC} Supply current (Average per flip-flop)	$V_{CC} = \text{MAX}$	-40 -100 -40	-100 -40 -100	-40 -100 -40	-40 -100 -40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

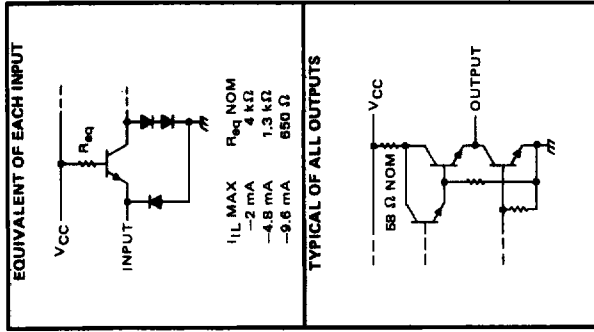
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54H/74H EDGE-TRIGGERED J-K FLIP-FLOPS

schematics of inputs and outputs

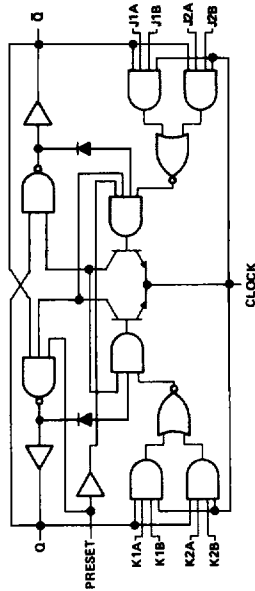


switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ$ C

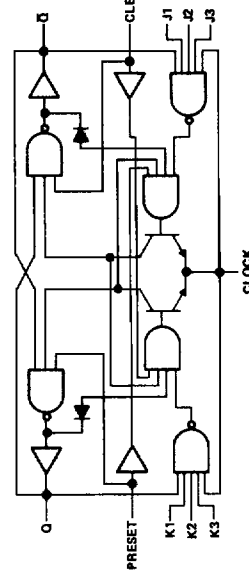
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				40	50		MHz
t_{PLH}	Preset or clear	Q or $\bar{Q}$	$C_L = 25$ pF,		8	12	ns
t_{PHL}	Preset or clear (clock high)	Q or $\bar{Q}$	$R_L = 280 \Omega$,		15	20	ns
t_{PLH}	Preset or clear (clock low)	Q or $\bar{Q}$	See Note 2		23	35	ns
t_{PHL}	Clock	Q or $\bar{Q}$			10	15	ns
t_{PHL}					16	20	ns

¹ f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

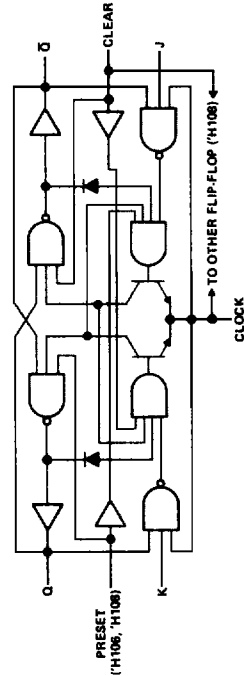
functional block diagrams



'H101-GATED J-K WITH PRESET



'H102-GATED J-K WITH CLEAR AND PRESET



'H103-DUAL J-K WITH CLEAR
 'H106-DUAL J-K WITH CLEAR AND PRESET
 'H108-DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SERIES 54L/74L FLIP-FLOPS

recommended operating conditions

	SERIES 54L/74L	'L71		'L72, 'L73		'L74		'L78		UNIT
		MIN	NOM MAX	MIN	NOM MAX	MIN	NOM MAX	MIN	NOM MAX	
Supply voltage, V_{CC}	Series 54L	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5
	Series 74L	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
	Series 54L									
High-level output current, I_{OH}	Series 54L									
	Series 74L									
	Series 54L									
Low-level output current, I_{OL}	Series 54L									
	Series 74L									
	Series 54L									
Pulse width, t_w	Clock high									
	Clock low									
	Clear or preset low									
Setup time, t_{su}										
Hold time, t_h										
Operating free-air temperature, T_A	Series 54L									
	Series 74L									

† The arrow indicates the edge of the clock pulse used for reference. † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'L71		'L72, 'L73		'L74		'L78		UNIT
		MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V_{IH} High-level input voltage		2		2		2		2		V
V_{IL} Low-level input voltage			0.6		0.6		0.7		0.7	V
V_{OH} High-level output voltage	All other inputs		0.7		0.7		0.7		0.7	V
	Series 54L									
	Series 74L									
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	3.3	2.4	3.3	2.4	3.3	2.4	3.3	V
	Series 54L									
	Series 74L									
Input current at maximum input voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = \text{MAX}$	0.15	0.3	0.15	0.3	0.15	0.3	0.15	0.3	V
	Series 54L									
	Series 74L									
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	100		100		100		100		μA
	Clear									
	Preset									
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	200		200		200		200		μA
	Clear									
	Preset									
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.3 \text{ V}$	200		200		200		200		μA
	Clear									
	Preset									
I_{OS} Short-circuit output current	$V_{CC} = \text{MAX}$									
	Clear									
	Preset									
I_{CC} Supply current (Average per flip-flop)	$V_{CC} = \text{MAX}$									
	Clear									
	Preset									

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

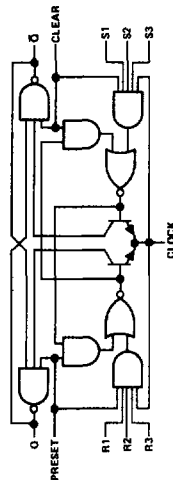
SERIES 54L/74L FLIP-FLOPS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

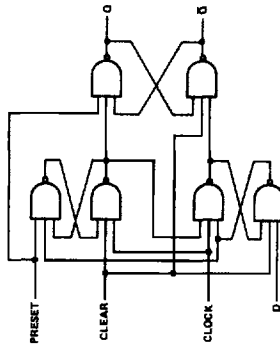
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L71, 'L72, 'L73, 'L78			'L74		UNIT	
				MIN	TYP	MAX	MIN	TYP		MAX
				2.5	3		2.5	3	MHz	
f_{max}										
t_{pLH}	Preset or clear	Q or $\bar{Q}$	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$, See Note 2		35	75	50	75	ns	
t_{pHL}	Preset or clear (clock high)	$\bar{Q}$ or Q			60	150	80	150	ns	
	Preset or clear (clock low)					200	80	150		
t_{pLH}	Clock	Q or $\bar{Q}$		10	35	75	15	65	100	ns
t_{pHL}				10	60	150	15	65	150	

¹ f_{max} $\equiv$ maximum clock frequency
 t_{PLH} $\equiv$ propagation delay time, low-to-high-level output
 t_{PHL} $\equiv$ propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

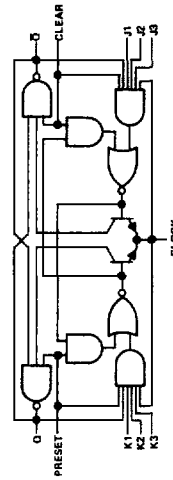
functional block diagrams



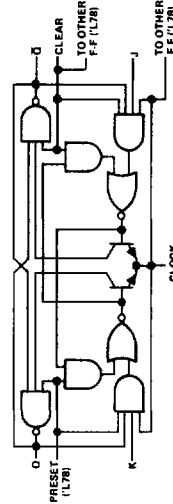
'L71—GATED R-S WITH CLEAR AND PRESET



'L74—DUAL D WITH CLEAR AND PRESET

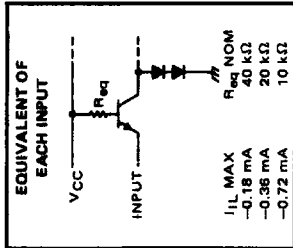


'L72—GATED J-K WITH CLEAR AND PRESET



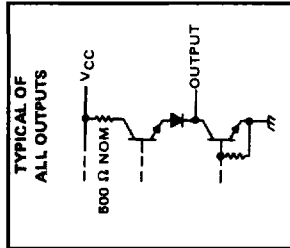
'L73—DUAL J-K WITH CLEAR
 'L78—DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

schematics of inputs and outputs



I_{IL} MAX
 -0.18 mA
 -0.36 mA
 -0.72 mA

R_{eq} NOM
 $40\text{ k}\Omega$
 $20\text{ k}\Omega$
 $10\text{ k}\Omega$



TYPICAL OF
 ALL OUTPUTS

SERIES SELECT		'LST2A, 'LST37A, 'LST150A	'LST4A	'LST6A, 'LST12A	'LST7A, 'LST14A	'LST10A	UNIT
Supply voltage, V_{CC}	Series 54LS	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	V
	Series 74LS	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	V
High-level output current, I_{OH}	Series 54LS	-400	-400	-400	-400	-400	μA
	Series 74LS	4	4	4	4	4	μA
Low-level output current, I_{OL}	Series 54LS	8	8	8	8	8	mA
	Series 74LS	0	0	0	0	0	mA
Clock frequency, f_{clock}	Click high	0	0	0	0	0	MHz
	Pulse width, t_p	20	25	20	20	25	ns
Present or clear low	Present or clear low	25	25	25	25	25	ns
	High-level data	20	25	20	20	20	ns
Setup time, t_{su}	High-level data	20	20	20	20	20	ns
	Low-level data	0	0	0	0	0	ns
Hold time, t_h	High-level data	0	0	0	0	0	ns
	Low-level data	0	0	0	0	0	ns
Operating free-air temperature, T_A	Series 54LS	-55	-55	-55	-55	-55	$^{\circ}C$
	Series 74LS	0	0	0	0	0	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ¹				'LE72A'		'LE72B'		'LE72C'		'LE72D'		'LE72E'		'LE72F'		'LE72G'		'LE72H'		'LE72I'		'LE72J'		'LE72K'		'LE72L'		'LE72M'		'LE72N'		'LE72O'		'LE72P'		'LE72Q'		'LE72R'		'LE72S'		'LE72T'		'LE72U'		'LE72V'		'LE72W'		'LE72X'		'LE72Y'		'LE72Z'		'LE72AA'		'LE72AB'		'LE72AC'		'LE72AD'		'LE72AE'		'LE72AF'		'LE72AG'		'LE72AH'		'LE72AI'		'LE72AJ'		'LE72AK'		'LE72AL'		'LE72AM'		'LE72AN'		'LE72AO'		'LE72AP'		'LE72AQ'		'LE72AR'		'LE72AS'		'LE72AT'		'LE72AU'		'LE72AV'		'LE72AW'		'LE72AX'		'LE72AY'		'LE72AZ'		'LE72BA'		'LE72BB'		'LE72BC'		'LE72BD'		'LE72BE'		'LE72BF'		'LE72BG'		'LE72BH'		'LE72BI'		'LE72BJ'		'LE72BK'		'LE72BL'		'LE72BM'		'LE72BN'		'LE72BO'		'LE72BP'		'LE72BQ'		'LE72BR'		'LE72BS'		'LE72BT'		'LE72BU'		'LE72BV'		'LE72BW'		'LE72BX'		'LE72BY'		'LE72BZ'		'LE72CA'		'LE72CB'		'LE72CC'		'LE72CD'		'LE72CE'		'LE72CF'		'LE72CG'		'LE72CH'		'LE72CI'		'LE72CJ'		'LE72CK'		'LE72CL'		'LE72CM'		'LE72CN'		'LE72CO'		'LE72CP'		'LE72CQ'		'LE72CR'		'LE72CS'		'LE72CT'		'LE72CU'		'LE72CV'		'LE72CW'		'LE72CX'		'LE72CY'		'LE72CZ'		'LE72DA'		'LE72DB'		'LE72DC'		'LE72DD'		'LE72DE'		'LE72DF'		'LE72DG'		'LE72DH'		'LE72DI'		'LE72DJ'		'LE72DK'		'LE72DL'		'LE72DM'		'LE72DN'		'LE72DO'		'LE72DP'		'LE72DQ'		'LE72DR'		'LE72DS'		'LE72DT'		'LE72DU'		'LE72DV'		'LE72DW'		'LE72DX'		'LE72DY'		'LE72DZ'		'LE72EA'		'LE72EB'		'LE72EC'		'LE72ED'		'LE72EE'		'LE72EF'		'LE72EG'		'LE72EH'		'LE72EI'		'LE72EJ'		'LE72EK'		'LE72EL'		'LE72EM'		'LE72EN'		'LE72EO'		'LE72EP'		'LE72EQ'		'LE72ER'		'LE72ES'		'LE72ET'		'LE72EU'		'LE72EV'		'LE72EW'		'LE72EX'		'LE72EY'		'LE72EZ'		'LE72FA'		'LE72FB'		'LE72FC'		'LE72FD'		'LE72FE'		'LE72FF'		'LE72FG'		'LE72FH'		'LE72FI'		'LE72FJ'		'LE72FK'		'LE72FL'		'LE72FM'		'LE72FN'		'LE72FO'		'LE72FP'		'LE72FQ'		'LE72FR'		'LE72FS'		'LE72FT'		'LE72FU'		'LE72FV'		'LE72FW'		'LE72FX'		'LE72FY'		'LE72FZ'		'LE72GA'		'LE72GB'		'LE72GC'		'LE72GD'		'LE72GE'		'LE72GF'		'LE72GG'		'LE72GH'		'LE72GI'		'LE72GJ'		'LE72GK'		'LE72GL'		'LE72GM'		'LE72GN'		'LE72GO'		'LE72GP'		'LE72GQ'		'LE72GR'		'LE72GS'		'LE72GT'		'LE72GU'		'LE72GV'		'LE72GW'		'LE72GX'		'LE72GY'		'LE72GZ'		'LE72HA'		'LE72HB'		'LE72HC'		'LE72HD'		'LE72HE'		'LE72HF'		'LE72HG'		'LE72HH'		'LE72HI'		'LE72HJ'		'LE72HK'		'LE72HL'		'LE72HM'		'LE72HN'		'LE72HO'		'LE72HP'		'LE72HQ'		'LE72HR'		'LE72HS'		'LE72HT'		'LE72HU'		'LE72HV'		'LE72HW'		'LE72HX'		'LE72HY'		'LE72HZ'		'LE72IA'		'LE72IB'		'LE72IC'		'LE72ID'		'LE72IE'		'LE72IF'		'LE72IG'		'LE72IH'		'LE72II'		'LE72IJ'		'LE72IK'		'LE72IL'		'LE72IM'		'LE72IN'		'LE72IO'		'LE72IP'		'LE72IQ'		'LE72IR'		'LE72IS'		'LE72IT'		'LE72IU'		'LE72IV'		'LE72IW'		'LE72IX'		'LE72IY'		'LE72IZ'		'LE72JA'		'LE72JB'		'LE72JC'		'LE72JD'		'LE72JE'		'LE72JF'		'LE72JG'		'LE72JH'		'LE72JI'		'LE72JJ'		'LE72JK'		'LE72JL'		'LE72JM'		'LE72JN'		'LE72JO'		'LE72JP'		'LE72JQ'		'LE72JR'		'LE72JS'		'LE72JT'		'LE72JU'		'LE72JV'		'LE72JW'		'LE72JX'		'LE72JY'		'LE72JZ'		'LE72KA'		'LE72KB'		'LE72KC'		'LE72KD'		'LE72KE'		'LE72KF'		'LE72KG'		'LE72KH'		'LE72KI'		'LE72KJ'		'LE72KK'		'LE72KL'		'LE72KM'		'LE72KN'		'LE72KO'		'LE72KP'		'LE72KQ'		'LE72KR'		'LE72KS'		'LE72KT'		'LE72KU'		'LE72KV'		'LE72KW'		'LE72	
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NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TEST CONDITIONS	'LS74A, 'LS108A		UNIT
f_{max}		$C_L = 15$ pF, $R_L = 2$ k Ω , See Note 2	MIN	TYP	MAX
t_{PLH}	Clear, preset, or clock (as appropriate)	$Q \rightarrow \bar{Q}$	30	45	25
t_{PLH}			15	20	13
			15	20	25
			20	25	40
					ns

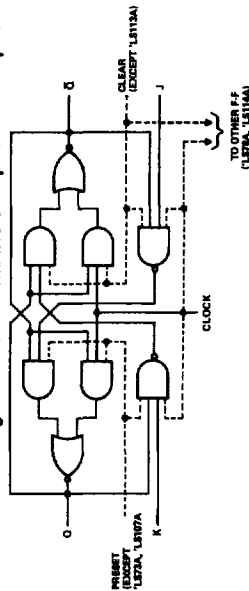
 $\omega_{\text{fmax}} \equiv \text{maximum clock frequency}$

tp_{LH} $\equiv$ propagation delay time, low-to-high-level output

tpHL $\equiv$ propagation delay time, high-to-low-level output

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagrams and schematics of inputs and outputs



'LS73A, 'LS107A--DUAL J-K WITH CLEAR

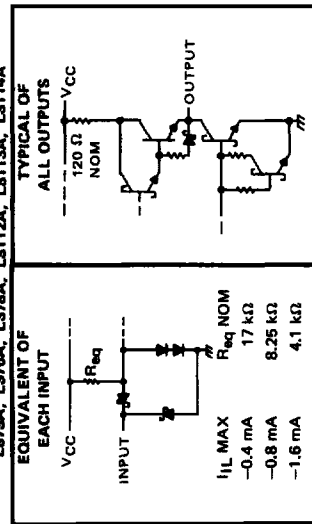
'LS76A,' 'LS112A—DUAL J-K WITH CLEAR AND PRESET

'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR,

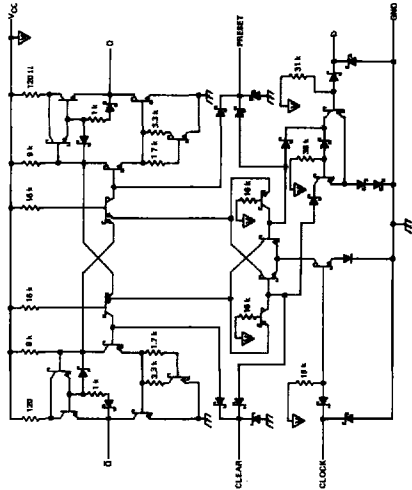
AND COMMON CLOCK

'LS113A—DUAL JK WITH PRESET

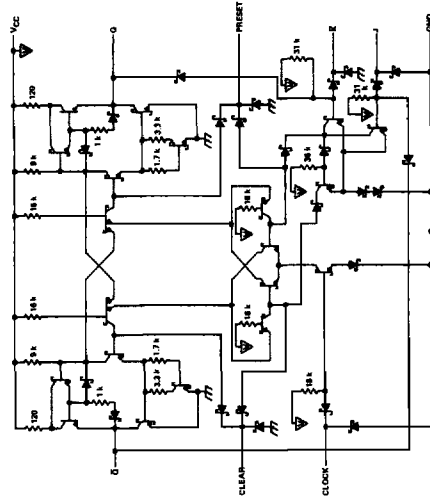
DATE



schematics of 'LS74A and 'LS109A



'LS74A--DUAL D WITH CLEAR AND PRESET



'LS109A—DUAL J-K WITH CLEAR AND PRESET

SERIES 54S/74S FLIP-FLOPS

recommended operating conditions

		SERIES 54S/74S		'S74		'S112		'S113		'S114		UNIT
		MIN	NOM MAX	MIN	NOM MAX	MIN	NOM MAX	MIN	NOM MAX	MIN	NOM MAX	
Supply voltage, V _{CC}		Series 54S		4.5	5 5.5	4.5	5 5.5	4.5	5 5.5	4.5	5 5.5	V
		Series 74S		4.75	5 5.25	4.75	5 5.25	4.75	5 5.25	4.75	5 5.25	V
High-level output current, I _{OH}				-1	-1	-1	-1	-1	-1	-1	-1	mA
Low-level output current, I _{OL}				20	20	20	20	20	20	20	20	mA
Pulse width, t _w		Clock high		6	6	6	6	6	6	6	6	ns
		Clock low		7.3	6.5	6.5	6.5	6.5	6.5	6.5	6.5	ns
Input setup time, t _{su}		Clear or preset low		7	8	8	8	8	8	8	8	ns
		High-level data		31	31	31	31	31	31	31	31	ns
Input hold time, t _h		Low-level data		31	31	31	31	31	31	31	31	ns
				21	01	01	01	01	01	01	01	ns
Operating free-air temperature, T _A		Series 54S		-55	125	-55	125	-55	125	-55	125	°C
		Series 74S		0	70	0	70	0	70	0	70	°C

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'S74		'S112		'S113		'S114		UNIT
			MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IH}	High-level input voltage		2	0.8	2	0.8	2	0.8	2	0.8	V
V _{IL}	Low-level input voltage			-1.2		-1.2		-1.2		-1.2	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA									V
V _{OH}	High-level output voltage	Series 54S	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	V
		Series 74S	2.7	3.4	2.7	3.4	2.7	3.4	2.7	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V,		0.5		0.5		0.5		0.5	V
		V _{IL} = 0.8 V, I _{OL} = 20 mA									
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1	1	1	1	1	1	1	1	mA
I _{IH}	High-level input current	J, K, or D	50	50	50	50	50	50	50	50	µA
		Clear	150	100	100	100	100	100	100	100	µA
		Preset	100	100	100	100	100	100	100	100	µA
I _{IL}	Low-level input current	Clock	100	100	100	100	100	100	100	100	µA
		J, K, or D	-2	-2	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	mA
		Clear *	-6	-6	-7	-7	-7	-7	-7	-7	mA
		Preset *	-4	-4	-7	-7	-7	-7	-7	-7	mA
		Clock	-4	-4	-4	-4	-4	-4	-4	-4	mA
I _{OS}	Short-circuit output current*	V _{CC} = MAX	-40	-100	-40	-100	-40	-100	-40	-100	mA
I _{CC}	Supply current (average per flip-flop)	V _{CC} = MAX, See Note 1	15	25	15	25	15	25	15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

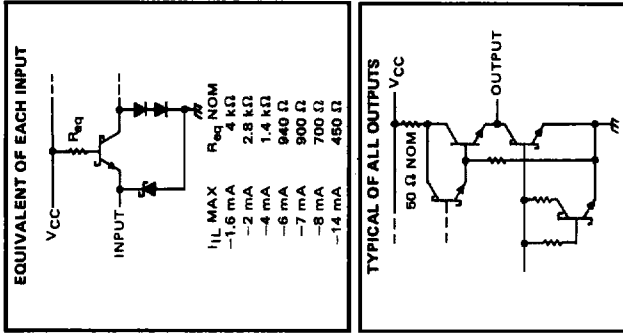
* Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

§ Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54S/74S FLIP-FLOPS

schematics of inputs and outputs

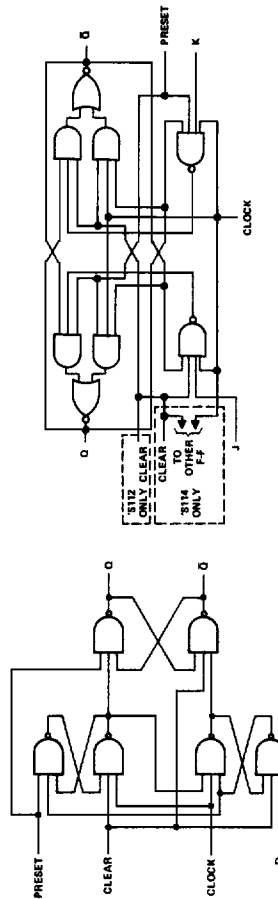


switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74	'S112, 'S113, 'S114	UNIT
f_{max}				MIN TYP MAX	MIN TYP MAX	MHz
t_{PLH}	Preset or clear	Q or $\bar{Q}$	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$, See Note 2	75 110	80 125	ns
t_{PHL}	Preset or clear (clock high)	$\bar{Q}$ or Q		4 6	4 7	ns
t_{PLH}	Preset or clear (clock low)	Q or $\bar{Q}$		9 13.5	5 7	ns
t_{PHL}	Clock	Q or $\bar{Q}$		5 8	5 7	ns
				6 9	4 7	ns
				6 9	5 7	ns

¹ f_{max} $\equiv$ maximum clock frequency
 t_{PLH} $\equiv$ propagation delay time, low-to-high-level output
 t_{PHL} $\equiv$ propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



'S74-DUAL D WITH CLEAR AND PRESET

'S112-DUAL J-K WITH CLEAR AND PRESET

'S113-DUAL J-K WITH PRESET

'S114-DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

3-R LATCHES

recommended operating conditions

	54 FAMILY 74 FAMILY	SN54LS279 SN74LS279			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	V
High-level output current, I_{OH}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	μ A
Low-level output current, I_{OL}	54 Family 74 Family	16 16			mA
Operating free-air temperature, T_A	54 Family 74 Family	-55 0	125 70	-65 0	$^{\circ}$ C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS279 SN74LS279			UNIT
		MIN	TYP‡	MAX	
V_{IH} High-level output voltage		2			V
V_{IL} Low-level output voltage	54 Family 74 Family		0.8	0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MAX}, I_I = \frac{1}{2}$		-1.5	-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	3.4	2.5	3.4
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = V_{IL \text{ max}}, V_{IH} = 2 \text{ V}$	0.2	0.4	0.25	0.4
	$I_{OL} = \text{MAX}$			0.35	0.4
	$I_{OL} = 4 \text{ mA}$			0.35	0.4
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$		1		mA
	$V_I = 5.5 \text{ V}$				
	$V_I = 7 \text{ V}$			0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$		40		μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.8	-0.4	mA
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$	-18	-55	-20	-100
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See note 1	-18	-57	-20	-100
		18	30	3.8	7

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

* $I_I = -12 \text{ mA}$ for SN54/LSN74 and -18 mA for SN54LS/LSN74LS.

†Not more than one output should be shorted at a time, and for SN54LS/LSN74LS, duration of the output short circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all $\bar{R}$ inputs grounded, all $\bar{S}$ inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

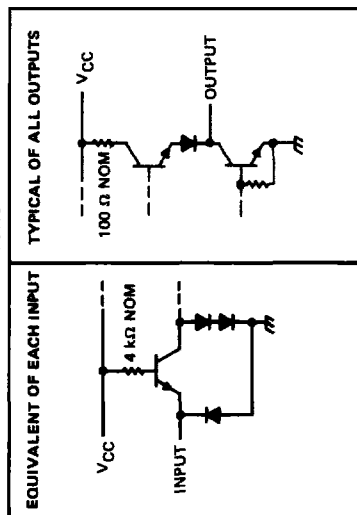
PARAMETER	TEST CONDITIONS		'279		'LS279		UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pLH} Propagation delay time, low-to-high-level output from S input		12	22		12	22	ns
t_{pHL} Propagation delay time, high-to-low-level output from S input		9	15		13	21	
t_{pHL} Propagation delay time, high-to-low-level output from R input		15	27		15	27	

NOTE 2: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

NOTE 3: $R_L = 400\ \Omega$ for '279, $R_L = 2\text{ k}\Omega$ for 'LS279.

schematics of inputs and outputs

'279 CIRCUITS



'LS279 CIRCUITS

