



Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

General Description

The MAX9960 dual-flash-pin electronics/supervoltage switch matrix replaces most of the relays and switches commonly needed to connect system resources to each of two pins in a flash memory or SOC ATE system (Figure 1). The device provides seven switches per channel to select up to four independent sources: the pin electronics (PE), two parametric measurement units (PMUs) or other Kelvin analog resources, and a flash memory programming supervoltage (FV_{HH}_). The force-and-sense PMU switches are independently controlled, enabling their use to connect two non-Kelvin resources in place of each PMU or Kelvin resource. Each MAX9960 contains two complete seven-switch channels with fully independent controls.

The MAX9960 features signal path switches with wide 600MHz bandwidth, low 3Ω series resistance, and low 8pF shunt capacitance over a voltage range compatible with common pin electronics ICs. An on-chip voltage-doubling buffer with selectable 1x or 2x gain generates the flash supervoltage, allowing a 6.5V DAC reference input to generate up to a maximum of 13V for flash-memory programming levels.

When switching from the FV_{HH_} to PE_ or from PE_ to FV_{HH_}, the device-under-test (DUT_) voltage behaves monotonically. Switching transitions between the PE_ and FV_{HH_} inputs are typically less than 350ns.

The MAX9960 operates over a commercial 0°C to +70°C temperature range, and is available in the 48-pin thin QFN package (7mm x 7mm x 0.8mm) with an exposed pad on the bottom for heat removal.

Applications

Flash Memory Automatic Test Equipment

SOC Automatic Test Equipment

Features

- ◆ Dual Supervoltage Switch Arrays
- ◆ 3Ω, 8pF, 600MHz Bandwidth Pin Electronics Paths
- ◆ 13V Flash Programming Paths
- ◆ On-Chip 1x and 2x Selectable Gains
- ◆ 2 Kelvin PMU Paths
- ◆ Fast Switching: 350ns (typ)
- ◆ Monotonic Slew Rate When Switching Between PE₀ and FVHH

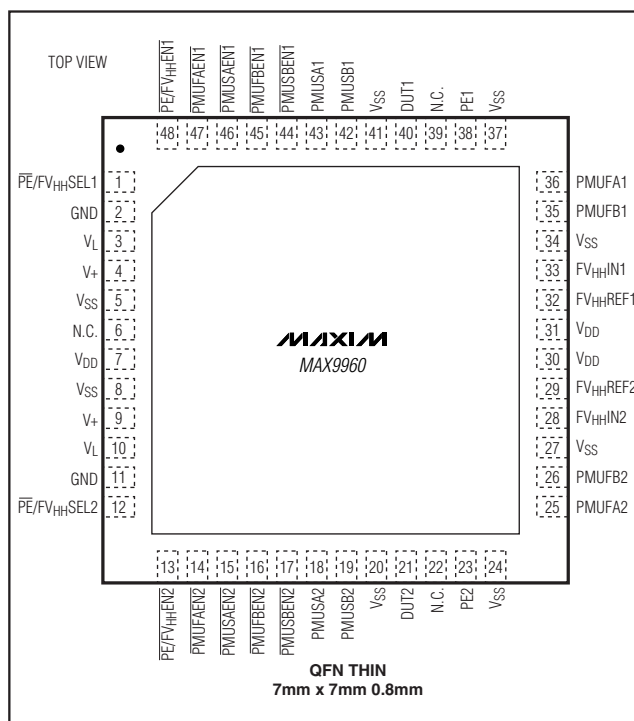
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE* | PKG CODE |
|-------------|--------------|---|----------|
| MAX9960BCTM | 0°C to +70°C | 48 Thin QFN-EP** (7mm x 7mm x 0.8mm) | T4877-6 |

* See full package information at the end of this data sheet.

**EP = Exposed pad.

Pin Configuration



MAX9960



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.



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Part Number Table

Notes:

1. See the [MAX9960 QuickView Data Sheet](#) for further information on this product family or download the [MAX9960 full data sheet](#) (PDF, 632kB).
2. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
3. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [full data sheet](#) or [Part Naming Conventions](#).
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

| Part Number | Free Sample | Buy Direct | Package: TYPE PINS SIZE DRAWING CODE/VAR * | Temp | RoHS/Lead-Free? Materials Analysis |
|----------------|----------------------|----------------------|---|------------|--|
| MAX9960BCTM-TD | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: No |
| MAX9960BCTM+D | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: Yes |
| MAX9960BCTM+TD | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: Yes |
| MAX9960BCTM-D | <input type="text"/> | <input type="text"/> | THIN QFN;48 pin;7x7x0.8mm Dwg: 21-0144F (PDF) Use pkgcode/variation: T4877-6* | 0C to +70C | RoHS/Lead-Free: No Materials Analysis |

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Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

ABSOLUTE MAXIMUM RATINGS

V₊ to GND -0.3V to +26V
V_{DD} to GND -0.3V to +16.5V
V_{SS} to GND -6.5V to +0.3V
V_L to GND -0.3V to +6V
V₊ to V_{SS} +32V
Digital Inputs (GND - 0.3V) to (V_L + 0.3V)
FVHHIN₋ (the higher of -4V and (V_{SS} - 0.3V)) to (the lower of +10V and (V_{DD} + 0.3V))
All Other Pins (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Continuous Current, PE₋ ±120mA
Continuous Current, PMUS₋ ±10mA
Continuous Current, PMUFA₋ + PMUFB₋ + (FVHH₋ Path) ±45mA

Peak Current (100ns), PE₋ ±300mA
Peak Current (100ns), PMUS₋ ±20mA
Peak Current (100ns), PMUFA₋ + PMUFB₋ + (FVHH₋ Path) ±70mA
Package Continuous Power Dissipation (T_A = +70°C)
48-Pin QFN-EP, on Single-Layer Board (derate 27.8mW/°C above +70°C) 2222mW
48-Pin QFN-EP, on Multilayer Board (derate 40.0mW/°C above +70°C) 3200mW
Operating Temperature Range 0°C to +70°C
Junction Temperature +150°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (soldering 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V₊ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|-----------------------|--|-------|-----|-----------------------|-------|
| DC CHARACTERISTICS | | | | | | |
| PE₋ PATH | | | | | | |
| On-Resistance | R _{ON} | V _{DUT₋} = +2.5V, I _{SW} = -40mA to +40mA, T _A = 0°C to +30°C (Note 1) | 2.5 | 3.0 | 3.5 | Ω |
| | | V _{DUT₋} = +2.5V, I _{SW} = -40mA to +40mA, T _A = +30°C to +70°C (Note 1) | 2.5 | | 4.2 | |
| On-Resistance Flatness | R _{FLAT(ON)} | V _{DUT₋} = 0 to +5V (Note 1) | -0.6 | | +0.6 | Ω |
| Ch1 to Ch2 Resistance Match | R _{MATCH} | V _{DUT₋} = +2.5V, I _{SW} = -40mA to +40mA | -0.5 | | +0.5 | Ω |
| Signal Voltage Range | V _{PE} | | -3.5 | | +8.0 | V |
| Operating DC Current Range | I _{SW} | | -40 | | +40 | mA |
| FVHH₋ PATH | | | | | | |
| On-Resistance | R _{ON} | FVHH ₋ = -1.5V to (V _{DD} - 1.5V), I _{HH₋} = -10mA to +10mA (Notes 1, 2) | 32 | | 100 | Ω |
| Operating Voltage Range | FVHH ₋ | | -1.5 | | V _{DD} - 1.5 | V |
| Operating DC Current Range | I _{SW} | | -10 | | +10 | mA |
| FORCE PATHS | | | | | | |
| On-Resistance | R _{ON} | V _{PMUF₋} = -4.25V to +14.5V, I _{PMUF₋} = -25mA to +25mA (Note 1) | | | 70 | Ω |
| Operating Voltage Range | V _{PMUF} | | -4.25 | | +14.5 | V |
| Operating DC Current Range | I _{SW} | | -25 | | +25 | mA |
| SENSE PATHS | | | | | | |
| On-Resistance | R _{ON} | V _{PMUS₋} = -4.25V to +14.5V, I _{PMUS₋} = -1mA to +1mA (Note 1) | | | 1250 | Ω |

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ELECTRICAL CHARACTERISTICS (continued)

(V₊ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------------------|--|-------|------|------------------------|-------|
| Operating Voltage Range | V _{PMUS} | | -4.25 | | +14.5 | V |
| Operating DC Current Range | I _{SW} | | -1 | | +1 | mA |
| FV_{HH}_ BUFFERS | | | | | | |
| DC Output Current | I _{ODC} | FV _{HH} = -1.5V to (V _{DD} - 1.5V) | 10 | | | mA |
| Current Limit | I _{LIM} | DUT_ sourcing current | +15 | | +25 | mA |
| | | DUT_ sinking current | -25 | | -15 | |
| Operating Voltage Range | FV _{HH} | FV _{HH} REF_ = 0 (Note 2) | -1.5 | | V _{DD} - 1.5V | V |
| Linearity Error | LER_FV _{HH} | FV _{HH} REF_ = 0; no load; relative to 2-point line between V _{DUT_} = 0 and +13V; measured at V _{DUT_} = +3.25V, +6.5V, and +9.75V | -2 | | +2 | mV |
| Gain | GFV _{HH} | FV _{HH} REF_ = 0, no load, V _{DUT_} = 0 to +13V (Note 3) | 1.98 | 2.00 | 2.02 | V/V |
| Output Offset | V _{OS_FV_{HH}} | FV _{HH} REF_ = 0, V _{DUT_} = +12V, no load | -50 | | +50 | mV |
| Output Offset Temperature Coefficient | T _{C_VOS} | V _{DUT_} = 0 to +13V, FV _{HH} REF_ = 0, T _{CASE} = +30°C to +50°C | | ±0.2 | | mV/°C |
| Input Bias Current | IFV _{HH} | FV _{HH} IN_ = -1.5V to +7.5V, FV _{HH} REF_ = open | -25 | | +25 | μA |
| Gain Resistor Ground | FV _{HH} REF | (Note 4) | -1.5 | | +0.5 | V |
| Gain Resistor Current | I _{V_{HH}REF} | Measured with FV _{HH} IN_ = +5V, FV _{HH} REF_ = 0 | | 0.4 | | mA |
| LEAKAGE (Notes 5, 6) | | | | | | |
| DUT_ Leakage, Disabled | I _{LEAK_OFF} | Switches S1, S2, S6, S7 open; V _{DUT_} = -4.25V to +14.5V | -1 | | +1 | nA |
| PE_ Leakage | I _{LEAK_PE} | S1 closed; S2, S6, S7 open; V _{DUT_} = -3.5V to +8V | -1 | | +1 | nA |
| PMUA_ Path Leakage, Enabled | I _{LEAK_PMU A_ON} | S2, S4, S6 closed; S1, S3, S5, S7 open; V _{DUT_} = -4.25V to +14.5V | -1 | | +1 | nA |
| PMUB_ Path Leakage, Enabled | I _{LEAK_PMU B_ON} | S2, S5, S7 closed; S1, S3, S4, S6 open; V _{DUT_} = -4.25V to +14.5V | -1 | | +1 | nA |
| PMUA_ Path Leakage, Disabled | I _{LEAK_PMU A_OFF} | S4, S6 open; V _{PMUFA_} = -4.25V to +14.5V; measured at PMUFA_ with PMUSA_ externally connected to PMUFA_ | -1 | | +1 | nA |
| PMUB_ Path Leakage, Disabled | I _{LEAK_PMU B_OFF} | S5, S7 open; V _{PMUFB_} = -4.25V to +14.5V; measured at PMUFB_ with PMUSB_ externally connected to PMUFB_ | -1 | | +1 | nA |
| DIGITAL INPUTS (PMUF_EN_, PMUS_EN_, PE/FV_{HH}EN_, PE/FV_{HH}SEL_) | | | | | | |
| Input High Voltage | V _{IH} | | +2.3 | | | V |
| Input Low Voltage | V _{IL} | | | | +0.4 | V |

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, VDD = +15V, VSS = -5V, VL = +3.3V, TA = +25°C, unless otherwise noted. Specifications at TA = 0°C and TA = +70°C are guaranteed by design and characterization. Typical values are at TA = +25°C, unless otherwise noted.) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|---|-------|------|-------|-------|
| Input Voltage Range | VIN | | -0.2 | | VL | V |
| Input Current | I _{IH} , I _{IL} | VIN = -0.2V to VL | -10 | | +10 | μA |
| POWER SUPPLIES | | | | | | |
| Positive Supply | VDD | | 14.5 | 15 | 16.0 | V |
| Negative Supply | VSS | | -6.00 | -5 | -4.25 | V |
| High Voltage Supply | V+ | (Note 1) | 23 | 24 | 25 | V |
| Logic Supply | VL | | 3.0 | 3.3 | 3.6 | V |
| Quiescent Positive Supply Current | Σ (IDD, I+) | V+ = +24V, VDD = +15V, VSS = -5V, VL = +3.3V, FVHHIN_ = +6.5V, FVHHREF_ = 0, all digital inputs = +2.3V, no loads | | | 10 | mA |
| Quiescent Negative Supply Current | I _{SS} | V+ = +24V, VDD = +15V, VSS = -5V, VL = +3.3V, FVHHIN_ = +6.5V, FVHHREF_ = 0, all digital inputs = +2.3V, no loads | | | 8.5 | mA |
| Quiescent Logic Supply Current | I _{VL} | V+ = +24V, VDD = +15V, VSS = -5V, VL = +3.3V, FVHHIN_ = +6.5V, FVHHREF_ = 0, all digital inputs = +2.3V, no loads | | | 2 | mA |
| Quiescent Power Dissipation | P _{DQ} | V+ = +24V, VDD = +15V, VSS = -5V, VL = +3.3V, FVHHIN_ = +6.5V, FVHHREF_ = 0, all digital inputs = +2.3V, no loads | | | 200 | mW |
| AC CHARACTERISTICS | | | | | | |
| SWITCHING TIMES BETWEEN PE_ AND FVHH_ PATHS (Note 7) (Figure 3) | | | | | | |
| Switch PE_ to FVHH_ | t _{ON_FVHH} | +5V to +7V transition | | 275 | 425 | ns |
| | | 0 to +13V transition | | 350 | 500 | |
| FVHH_ Settling Time | t _{S_FVHH} | Settling to within larger of 1% step voltage or 50mV of final value | | 500 | | ns |
| Switch FVHH_ to PE_ | t _{ON_PE} | | | 300 | 425 | ns |
| PE_ Settling Time | t _{S_PE} | Settling to within larger of 1% step voltage or 50mV of final value | | 500 | | ns |
| PE_ to FVHH_ Overshoot/Undershoot | | | | ±100 | | mV |
| PE_ to FVHH_ Preshoot | | | | ±150 | | mV |
| Minimum Switching Slew Rate | SR _{MIN} | Over 20% to 80% region | | ±10 | | V/μs |
| SWITCHING TIMES, SAME PATH (Note 8) (Figure 2) | | | | | | |
| PE_ Switch On-Time | t _{ON_1} | V _{PE_} = +5V from 47Ω source | | 150 | | ns |
| FVHH_ Switch On-Time | t _{ON_2,3} | FVHHIN_ = +2.5V, FVHHREF_ = 0 | | 350 | | ns |

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ELECTRICAL CHARACTERISTICS (continued)

(V₊ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|--|-----|-----|-----|-------|
| PMUF_ Switch On-Time | t _{ON_2,4} t _{ON_2,5} | V _{PMUF_} = +5V | | 150 | | ns |
| PMUS_ Switch On-Time | t _{ON_6} t _{ON_7} | V _{PMUS_} = +5V | | 300 | | ns |
| PE_, FVHH_, PMUF_ , PMUS_ Switch Off-Times | t _{OFF} | | | 700 | | ns |
| CAPACITANCE AND BANDWIDTH (Note 5) | | | | | | |
| Capacitance, All Paths Disconnected | C _{DUT_OFF} | All switches disconnected, for frequencies greater than 2MHz (Note 9) | | 20 | | pF |
| Capacitance, PE_ Path Connected (Note 9) | C _{DUT_PE} | Switch S1 closed, all others open, for frequencies greater than 2MHz | | 8 | | pF |
| | | Switch S1 closed, all others open, for frequencies less than 1kHz | | 50 | | |
| Unit-to-Unit Variation, PE_ Path Connected | ΔC _{DUT_PE} | Switch S1 closed, all others open, for frequencies greater than 2MHz (Note 9) | | ±2 | | pF |
| Capacitance, PMUFA_ and PMUSA_ Path Connected | C _{DUT_PMUA} | S2, S4, and S6 closed; all others open (Note 9) | | 35 | | pF |
| Capacitance, PMUFB_ and PMUSB_ Path Connected | C _{DUT_PMUB} | S2, S5, and S7 closed; all others open (Note 9) | | 35 | | pF |
| Capacitance, PMUFA_ Path Disconnected | C _{PMUFA_OFF} | S4 open, measured at PMUFA_ (Note 9) | | 10 | | pF |
| Capacitance, PMUFB_ Path Disconnected | C _{PMUFB_OFF} | S5 open, measured at PMUFB_ (Note 9) | | 10 | | pF |
| Capacitance, PMUSA_ Path Connected | C _{PMUSA_ON} | S6 closed, all others open, measured at PMUSA_ (Note 9) | | 10 | | pF |
| Capacitance, PMUSB_ Path Connected | C _{PMUSB_ON} | S7 closed, all others open, measured at PMUSB_ (Note 9) | | 10 | | pF |
| Capacitance, PMUSA_ Path Disconnected | C _{PMUSA_OFF} | S6 open, measured at PMUSA_ (Note 9) | | 5 | | pF |
| Capacitance, PMUSB_ Path Disconnected | C _{PMUSB_OFF} | S7 open, measured at PMUSB_ (Note 9) | | 5 | | pF |
| PE_ Signal Bandwidth | f _{3DB} | Only PE_ path enabled (Note 10) | | 600 | | MHz |
| FVHH_ BUFFER | | | | | | |
| Slew Rate | SRFVHH | FVHHREF_ = 0, (gain = 2), FVHHIN_ stepped from 0 to +5V and +5V to 0 | | ±5 | | V/μs |
| Settling | t _s | C _{DUT_} = 200pF to within 0.1% of step voltage, after FVHHIN_ changes | | 25 | | μs |
| | | C _{DUT_} = 4000pF to within 0.1% of step voltage, after FVHHIN_ changes (Note 11) | | 50 | | |

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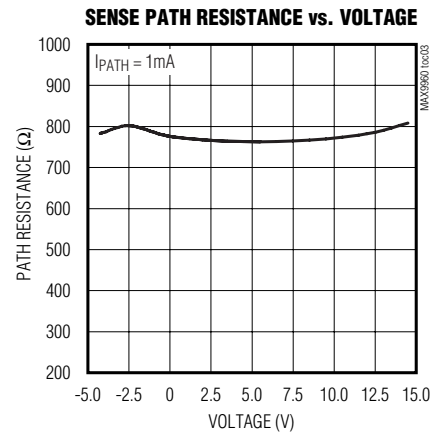
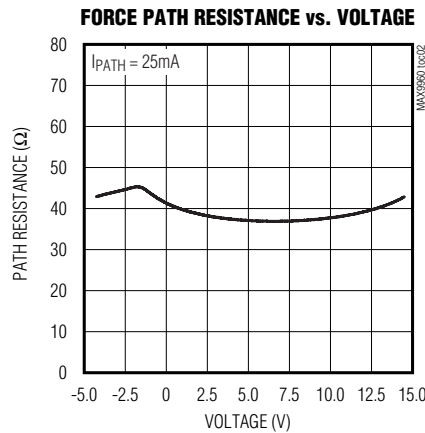
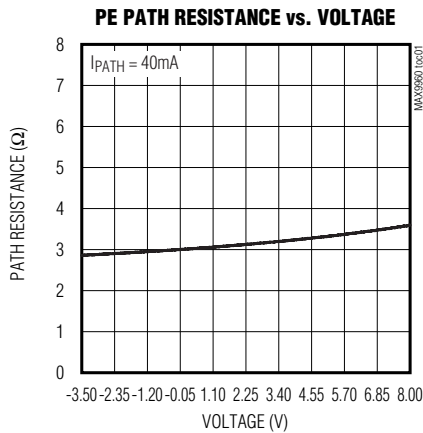
ELECTRICAL CHARACTERISTICS (continued)

($V_+ = +24V$, $V_{DD} = +15V$, $V_{SS} = -5V$, $V_L = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted. Specifications at $T_A = 0^\circ C$ and $T_A = +70^\circ C$ are guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Figure 1)

- Note 1:** V_+ should be at least 8V above V_{DD} to guarantee specified path resistance values.
- Note 2:** When the $FV_{HH_}$ buffer is configured for a gain of +1 ($FV_{HHREF_}$ open), the output voltage range is limited to -1.5V to +7.5V.
- Note 3:** $FV_{HH_}$ buffer gain is typically +1, when $FV_{HHREF_}$ is open.
- Note 4:** $FV_{HHREF_}$ is tested by repeating the $FV_{HH_}$ path resistance tests over the variation of $FV_{HHREF_}$. For each value of $FV_{HHREF_}$, $FV_{HHIN_}$ is adjusted to $FV_{HHIN_} = (FV_{HH_} + FV_{HHREF_}) / 2$.
- Note 5:** All measurements taken at $DUT_$, except where noted.
- Note 6:** These specifications are guaranteed by design and characterization. In addition, these specifications will be production tested with min/max test limits of $\pm 10nA$.
- Note 7:** Voltage source driving $PE_$ has 47Ω source resistance. $PE_ = 0$ to +5.0V, $FV_{HH_} = +7$ to +13V. Measured from 50% point of input logic to 90% of analog swing.
- Note 8:** All unused switches open, unless otherwise noted. Measured from 50% point of input logic to 90% of analog swing.
- Note 9:** Unless otherwise noted, measured at $DUT_$. No external connections to any of the switched analog pins— $PE_$, $DUT_$, $PMUFA_$, $PMUFB_$, $PMUSA_$, or $PMUSB_$ —except as needed to make measurement.
- Note 10:** $Z_{DUT_} = 50\Omega$; equivalent bandwidth calculated from measured $DUT_$ rise and fall time with $PE_$ stimulated by a 3V step with 1ns 10% to 90% rise/fall time.
- Note 11:** The maximum load for FV_{HH} buffer is 4000pF.

Typical Operating Characteristics

($V_+ = +24V$, $V_{DD} = +15V$, $V_{SS} = -5V$, $V_L = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

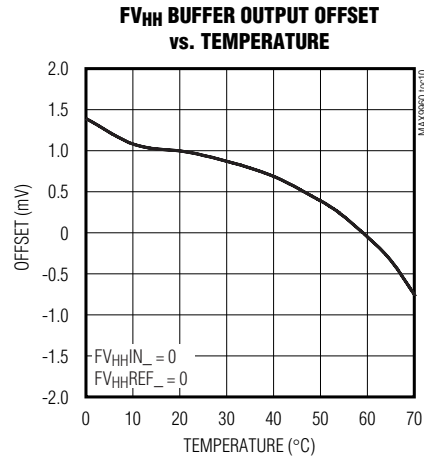
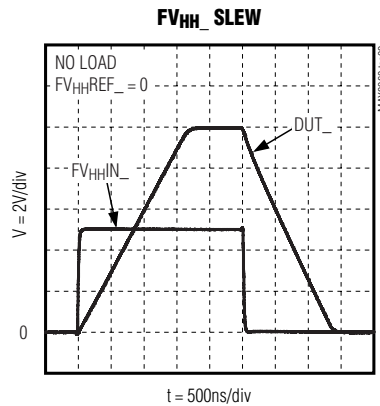
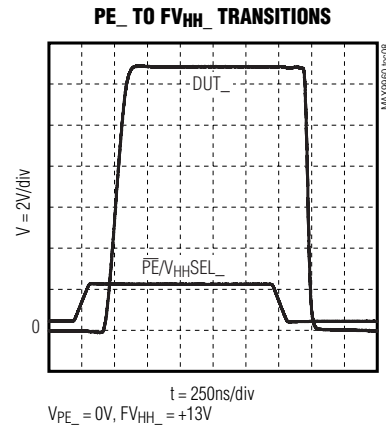
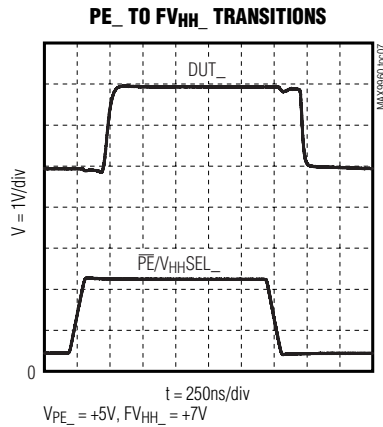
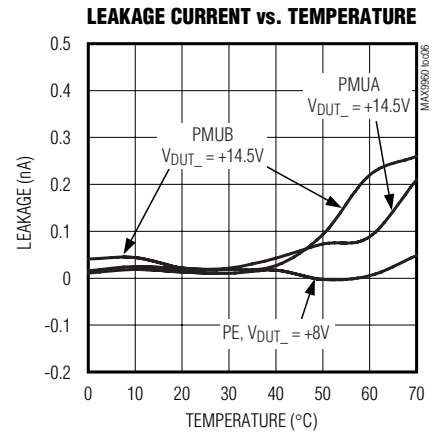
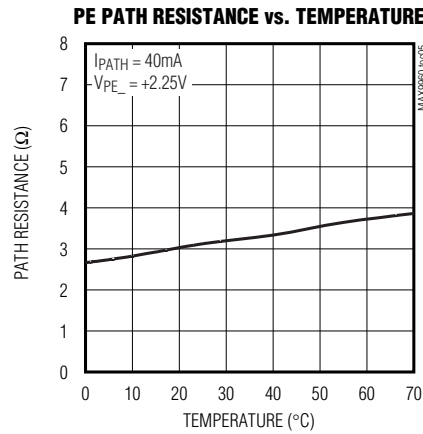
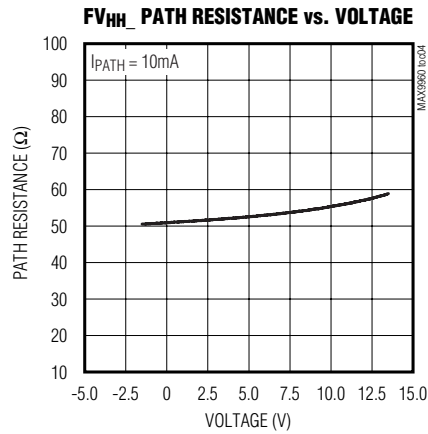


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Typical Operating Characteristics (continued)

($V_+ = +24V$, $V_{DD} = +15V$, $V_{SS} = -5V$, $V_L = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

Pin Description

| PIN | NAME | FUNCTION |
|------------------------------|---|---|
| 1 | $\overline{\text{PE}}/\text{FV}_{\text{HH}}\text{SEL1}$ | PE1 or FV _{HH} 1 Select. Selects either PE1 or FV _{HH} 1 to be connected to DUT1. Force low to select PE1, force high to select FV _{HH} 1. |
| 2, 11 | GND | Ground |
| 3, 10 | V _L | Logic Power Supply. Nominally 3.3V. |
| 4, 9 | V+ | Analog Positive Gate-Drive Power Supply. Nominally 24V. |
| 5, 8, 20, 24, 27, 34, 37, 41 | V _{SS} | Analog Negative Power Supply. Nominally -5V. |
| 6, 22, 39 | N.C. | No Connection. Make no connection to this pin. |
| 7, 30, 31 | V _{DD} | Analog Positive Power Supply. Nominally 15V. |
| 12 | $\overline{\text{PE}}/\text{FV}_{\text{HH}}\text{SEL2}$ | PE2 or FV _{HH} 2 Select. Selects either PE2 or FV _{HH} 2 to be connected to DUT2. Force low to select PE2, force high to select FV _{HH} 2. |
| 13 | $\overline{\text{PE}}/\text{FV}_{\text{HH}}\text{EN2}$ | PE2 and FV _{HH} 2 Enable. Enables PE2 and FV _{HH} 2 to be connected to DUT2, as determined by $\overline{\text{PE}}/\text{FV}_{\text{HH}}\text{SEL2}$. Force low to enable signal path, force high to disable the signal path. |
| 14 | $\overline{\text{PMUFA}}\text{EN2}$ | PMUFA2 Enable. Controls the connection of PMUFA2 to DUT2. Force low to connect PMUFA2 to DUT2, force high to disconnect PMUFA2 from DUT2. |
| 15 | $\overline{\text{PMUSA}}\text{EN2}$ | PMUSA2 Enable. Controls the connection of PMUSA2 to DUT2. Force low to connect PMUSA2 to DUT2, force high to disconnect PMUSA2 from DUT2. |
| 16 | $\overline{\text{PMUFB}}\text{EN2}$ | PMUFB2 Enable. Controls the connection of PMUFB2 to DUT2. Force low to connect PMUFB2 to DUT2, force high to disconnect PMUFB2 from DUT2. |
| 17 | $\overline{\text{PMUSB}}\text{EN2}$ | PMUSB2 Enable. Controls the connection of PMUSB2 to DUT2. Force low to connect PMUSB2 to DUT2, force high to disconnect PMUSB2 from DUT2. |
| 18 | PMUSA2 | Sense A Analog Output for Channel 2. Kelvin feedback output for the channel 2 force A path. |
| 19 | PMUSB2 | Sense B Analog Output for Channel 2. Kelvin feedback output for the channel 2 force B path. |
| 21 | DUT2 | Analog I/O for Channel 2. Connects to the DUT. |
| 23 | PE2 | Analog I/O for Channel 2. Connects to the pin electronics I/O. |
| 25 | PMUFA2 | Analog Input Force A for Channel 2. Connects to an external DC resource such as a PMU. |
| 26 | PMUFB2 | Analog Input Force B for Channel 2. Connects to an external DC resource such as a PMU. |
| 28 | FV _{HH} IN2 | Analog Supervoltage Input for Channel 2. The voltage applied to FV _{HH} IN2 is amplified as determined by FV _{HH} REF2 (see the <i>Functional Block Diagram</i>). |
| 29 | FV _{HH} REF2 | Analog Gain-Setting Input for Channel 2. Sets the gain of the FV _{HH} 2 buffer. |
| 32 | FV _{HH} REF1 | Analog Gain-Setting Input for Channel 1. Sets the gain of the FV _{HH} 1 buffer. |
| 33 | FV _{HH} IN1 | Analog Supervoltage Input for Channel 1. The voltage applied to FV _{HH} IN1 is amplified as determined by FV _{HH} REF1 (see the <i>Functional Block Diagram</i>). |
| 35 | PMUFB1 | Analog Input Force B for Channel 1. Connects to an external DC resource such as a PMU. |
| 36 | PMUFA1 | Analog Input Force A for Channel 1. Connects to an external DC resource such as a PMU. |
| 38 | PE1 | Analog I/O for Channel 1. Connects to the pin electronics I/O. |
| 40 | DUT1 | Analog I/O for Channel 1. Connects to the DUT. |
| 42 | PMUSB1 | Sense B Analog Output for Channel 1. Kelvin feedback output for the channel 1 force B path. |
| 43 | PMUSA1 | Sense A Analog Output for Channel 1. Kelvin feedback output for the channel 1 force A path. |

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

MAX9960

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|--------------------------------|---|
| 44 | $\overline{\text{PMUSBEN1}}$ | PMUSB1 Enable. Controls the connection of PMUSB1 to DUT1. Force low to connect PMUSB1 to DUT1, force high to disconnect PMUSB1 from DUT1. |
| 45 | $\overline{\text{PMUFBEN1}}$ | PMUFB1 Enable. Controls the connection of PMUFB1 to DUT1. Force low to connect PMUFB1 to DUT1, force high to disconnect PMUFB1 from DUT1. |
| 46 | $\overline{\text{PMUSAEN1}}$ | PMUSA1 Enable. Controls the connection of PMUSA1 to DUT1. Force low to connect PMUSA1 to DUT1, force high to disconnect PMUSA1 from DUT1. |
| 47 | $\overline{\text{PMUFAEN1}}$ | PMUFA1 Enable. Controls the connection of PMUFA1 to DUT1. Force low to connect PMUFA1 to DUT1, force high to disconnect PMUFA1 from DUT1. |
| 48 | $\overline{\text{PE/FVHHEN1}}$ | PE1 and FVHH1 Enable. Enables PE1 and FVHH1 to be connected to DUT1, as determined by $\overline{\text{PE/FVHHSEL1}}$. Force low to enable signal path, force high to disable the signal path. |
| — | EP | Exposed Pad for Heat Removal. Internally biased to VSS. Connect to VSS or leave floating. |

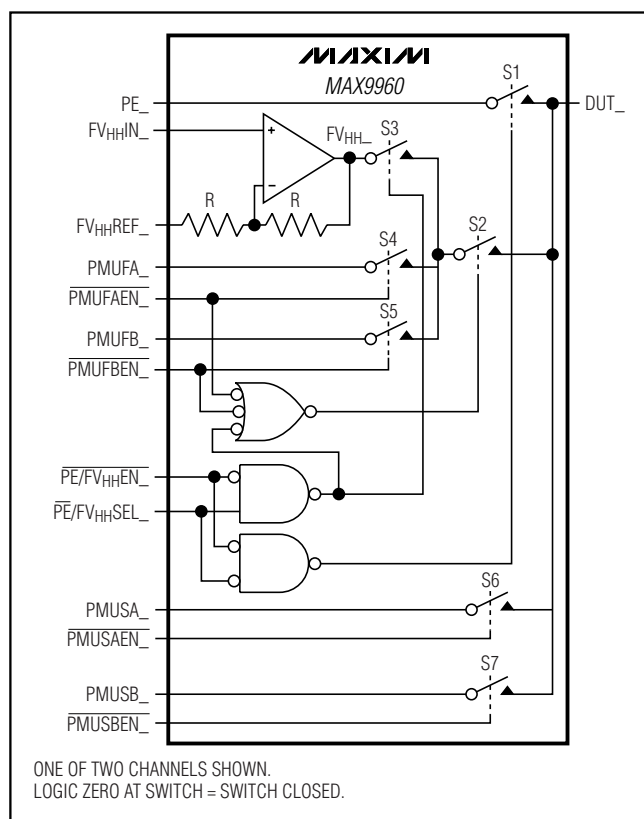


Figure 1. Functional Block Diagram

Detailed Description

The MAX9960 is a dual analog switch matrix featuring two Kelvin PMU paths, a PE path, and a flash programming supervoltage circuit that allows testing of flash memory using standard PE devices. It makes possible, without the use of relays, a fully functional pin with both AC and DC capabilities.

The signal path switches feature 600MHz bandwidth, 3Ω series resistance, and 8pF shunt capacitance over a voltage range compatible with common pin-electronics ICs. The voltage-doubling buffer, with selectable 1x or 2x gain, generates the 13V flash memory programming level from a 6.5V input. Configure the switches using digital inputs $\overline{\text{PMUFAEN}}$, $\overline{\text{PMUSAEN}}$, $\overline{\text{PMUFBEN}}$, $\overline{\text{PMUSBEN}}$, $\overline{\text{PE/FVHHEN}}$, and $\overline{\text{PE/FVHHSEL}}$ as indicated in Tables 1 and 2.

The switching speed between PE_ and FVHH_ paths is less than 350ns typical (Figure 3), and during switching, DUT_ behaves monotonically.

FVHH Buffer Load Capacitance

The maximum load capacitance for the FVHH buffer is 4000pF. While this amount of load capacitance is not expected during normal operation, an application may call for the buffer to be connected to a highly capacitive PMU path occasionally for calibration purposes. No damage to the MAX9960 will result as a consequence of this condition.

Supervoltage FVHH Buffer Gain

The FVHH buffer gain can be selected using FVHHREF_. If FVHHREF_ is grounded, the gain of the buffer is +2. If FVHHREF_ is left floating, the buffer gain is +1.

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

Table 1. Switch Control, All Possible Combinations

| PMUFAEN _– | PMUFBEN _– | PMUSAEN _– | PMUSBEN _– | PE/FV _{HH} EN _– | PE/FV _{HH} SEL _– | DUT _– |
|------------------------|----------------------|----------------------|----------------------|-------------------------------------|--------------------------------------|--|
| 0 | X | X | X | X | X | PMUFA _– path connected |
| X | 0 | X | X | X | X | PMUFB _– path connected |
| X | X | 0 | X | X | X | PMUSA _– path connected |
| X | X | X | 0 | X | X | PMUSB _– path connected |
| X | X | X | X | 0 | 1 | FV _{HH} _– path connected |
| X | X | X | X | 0 | 0 | PE _– path connected |
| All other combinations | | | | | | Every path is disconnected |

Table 2. Switch Control, Use Cases

| PMUFAEN _– | PMUFBEN _– | PMUSAEN _– | PMUSBEN _– | PE/FV _{HH} EN _– | PE/FV _{HH} SEL _– | DUT _– |
|----------------------|----------------------|----------------------|----------------------|-------------------------------------|--------------------------------------|---|
| 1 | 1 | 1 | 1 | 0 | 0 | PE _– |
| 1 | 1 | 1 | 1 | 0 | 1 | FV _{HH} _– |
| 0 | 1 | 0 | 1 | 1 | X | PMUFA _– + PMUSA _– |
| 1 | 0 | 1 | 0 | 1 | X | PMUFB _– + PMUSB _– |
| 0 | 1 | 0 | 1 | 0 | 0 | PE _– + PMUFA _– + PMUSA _– |
| 1 | 0 | 1 | 0 | 0 | 0 | PE _– + PMUFB _– + PMUSB _– |
| 0 | 1 | 0 | 1 | 0 | 1 | FV _{HH} _– + PMUFA _– + PMUSA _– |
| 1 | 0 | 1 | 0 | 0 | 1 | FV _{HH} _– + PMUFB _– + PMUSB _– |
| 0 | 0 | 0 | 0 | 0 | 0 | PE _– + PMUFA _– + PMUSA _– + PMUFB _– + PMUSB _– |

Power-Supply Considerations

The MAX9960 requires four power-supply voltages, typically V₊ = +24V, V_{DD} = +15V, V_{SS} = -5V, and V_L = +3.3V. Use a 0.1μF bypass capacitor close to each supply pin, and provide bulk bypassing where power enters the circuit board. The MAX9960 does not require any special power-up sequencing.

Chip Information

TRANSISTOR COUNT: 2020

PROCESS: BiCMOS

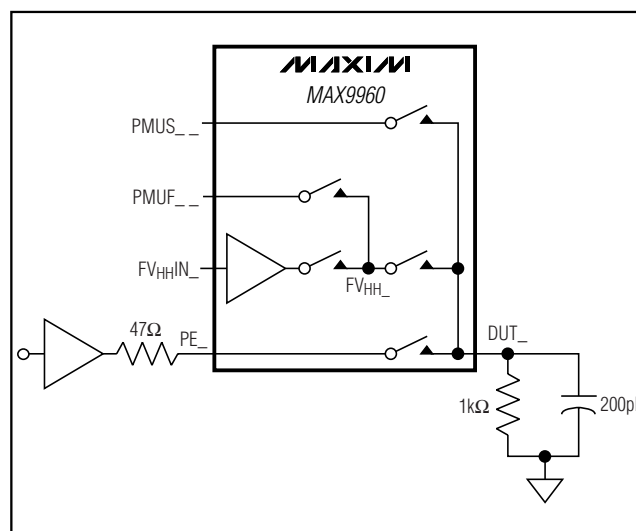


Figure 2. Switching Time Test Circuit

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

MAX9960

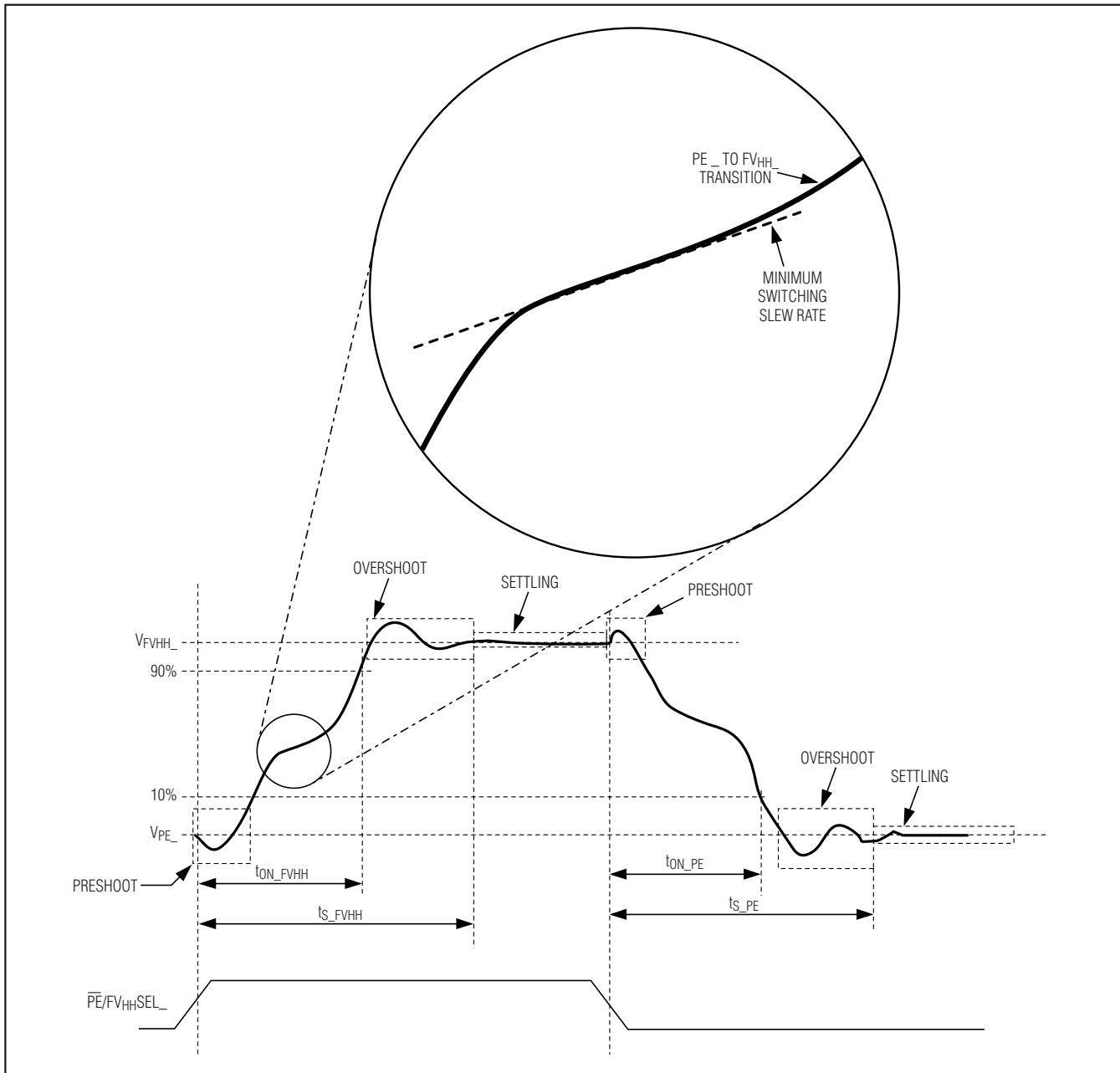


Figure 3. PE_ - FVHH_ and FVHH_ - PE_ Transition and Settling Timing

Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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Part Number Table

Notes:

1. See the [MAX9960 QuickView Data Sheet](#) for further information on this product family or download the [MAX9960 full data sheet](#) (PDF, 632kB).
2. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
3. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [full data sheet](#) or [Part Naming Conventions](#).
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

| Part Number | Free Sample | Buy Direct | Package: TYPE PINS SIZE DRAWING CODE/VAR * | Temp | RoHS/Lead-Free? Materials Analysis |
|----------------|----------------------|----------------------|---|------------|--|
| MAX9960BCTM-TD | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: No |
| MAX9960BCTM+D | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: Yes |
| MAX9960BCTM+TD | <input type="text"/> | <input type="text"/> | | 0C to +70C | RoHS/Lead-Free: Yes |
| MAX9960BCTM-D | <input type="text"/> | <input type="text"/> | THIN QFN;48 pin;7x7x0.8mm Dwg: 21-0144F (PDF) Use pkgcode/variation: T4877-6* | 0C to +70C | RoHS/Lead-Free: No Materials Analysis |

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