LX1668

PROGRAMMABLE MULTIPLE OUTPUT DC:DC CONTROLLER

THE INFINITE POWER OF INNOVATION

PRODUCTION DATA SHEET

DESCRIPTION

The LX1668 is a Monolithic Switching Regulator Controller IC designed to provide a low cost, high performance adjustable power supply for advanced microprocessors and other applications requiring a very fast transient response and a high degree of accuracy. It provides a programmable switching regulator output, together with one internal linear low dropout regulator and one adjustable linear regulator driver. The LX1668 offers a triple-output single-chip power supply for Pentium® II and other processors.

Programmable Synchronous Rectifier Driver for CPU Core. The main output is adjustable from 1.3 to 3.5V using a TTL-compatible 5-bit digital code to meet Intel specifications. The IC can read the signal from a DIP-switch, hardwired to Pentium II processor's pins or from software. The 5-bit code adjusts the output voltage between 1.30 and 2.05V in 50mV increments, and between 2.0 and 3.5V in 100mV increments. The device can drive dual MOSFET's resulting in typical efficiencies of 85 – 90%, even with loads in excess of 10A.

Internal Low Dropout [LDO] Regulator provides a fixed 2.5V output for powering the clock circuit at up to 250mA.

External Linear Regulator Driver output can be connected to a MOSFET to provide a high-current adjustable LDO function suitable for supplying the GTL+ bus circuitry on a Pentium II processor motherboard at 1.5V.

Short-circuit Current Limiting without Expensive Current Sense Resistors. The current sensing mechanism can use a PCB trace resistance or the parasitic resistance of the main inductor. For applications requiring a high degree of accuracy, a conventional sense resistor can be used.

Ultra-Fast Transient Response Reduces System Cost. The fixed frequency modulated off-time architecture results in the fastest transient response for a given inductor.

Small Package Size. The LX1668 is available in an economical 20-pin wide body SOIC or a space-saving 20-pin TSSOP package.

NOTE: For current data & package dimensions, visit our web site: **http://www.linfinity.com.**

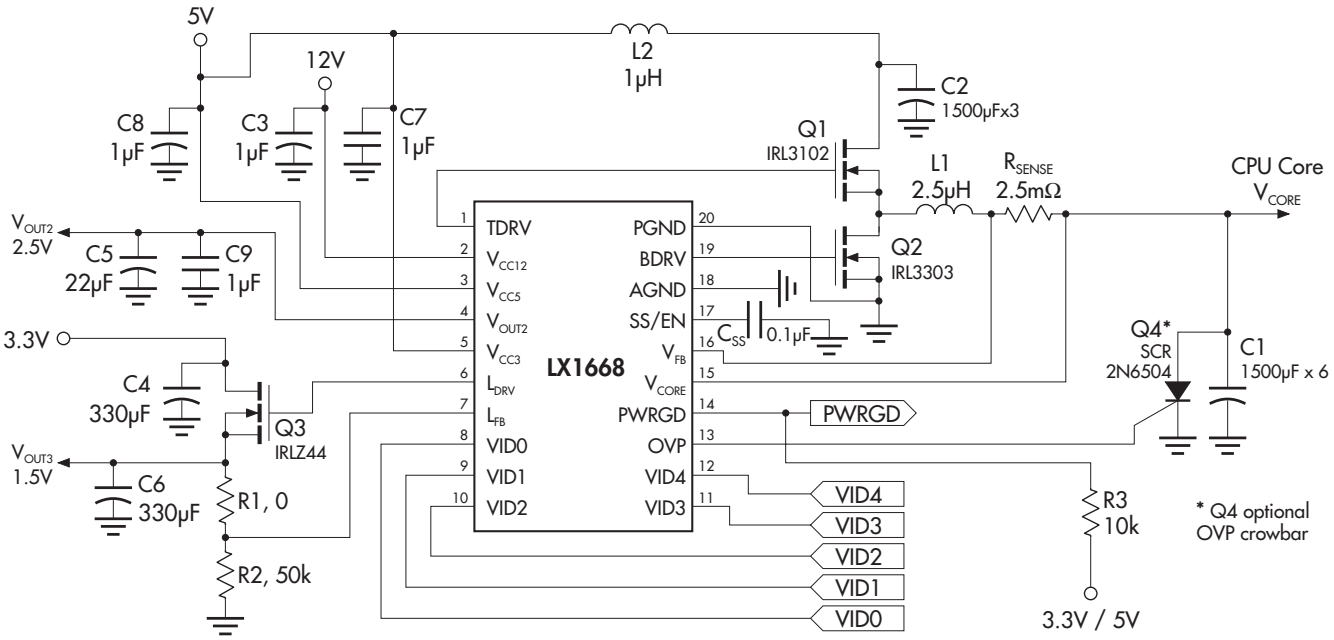
KEY FEATURES

- 5-Bit Programmable Output For CPU Core Supply
- Internal Fixed 2.5V Low Dropout Regulator
- Adjustable Linear Regulator Driver
- Complete Single-Chip Power Solution For Pentium II Processors
- No Sense Resistor Required For Short-Circuit Current Limiting
- Soft-Start And Hiccup-Mode Current Limiting Functions
- Modulated Constant Off-Time Control Mechanism For Fast Transient Response And Simple System Design
- Power Good Flag
- Over-Voltage Pin & SCR
- Digital-Compatible Inputs (Including VID Pins)
- Output Disable Function Shuts Off PWM While Keeping 2.5V LDO Active - Compatible With "Green PC" And "Instant On" Requirements
- Compatible to VRM8.2 - 8.4 Specifications

APPLICATIONS

- Pentium II & Pentium III Processor Supplies
- Voltage Regulator Modules
- General Purpose And Microprocessor DC:DC Supplies

PRODUCT HIGHLIGHT



PACKAGE ORDER INFORMATION

T_A (°C)	DW Plastic SOWB 20-pin	PW Plastic TSSOP 20-pin
0 to 70	LX1668CDW	LX1668CPW

Note: All surface-mount packages are available in Tape & Reel, append the letter "T" to part number. (i.e. LX1668CPWT)

LINFINITY MICROELECTRONICS INC.
11861 WESTERN AVENUE, GARDEN GROVE, CA. 92841, 714-898-8121, FAX: 714-893-2570

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

12V Supply Voltage (V_{CC12}) 18V
5V Supply Voltage (V_{CC5}) 7V
Supply Voltage (Internal LDO)/(V_{CC3}) 7V
Output Drive Peak Current Source (500ns) 1.0A
Output Drive Peak Current Sink (500ns) 1.0A
Input Voltage (SS, VID[0:4]) ..... -0.3V to 6V
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Note 2. V_{CC3} supply is used as input to internal low dropout regulator. Voltages above 3.3V will cause increased thermal dissipation in the package. Power dissipation should be limited to keep junction temperature below maximum rating.

THERMAL DATA

DW PACKAGE:

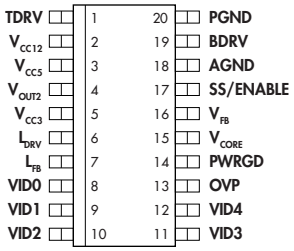
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	**85°C/W**

PW PACKAGE:

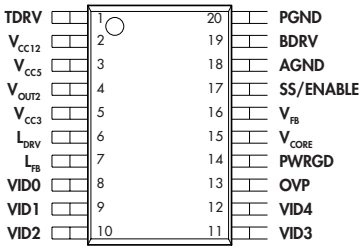
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	**110°C/W**

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUTS



DW PACKAGE — 20-Pin
(Top View)



PW PACKAGE — 20-Pin
(Top View)

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, 4.75V < V_{CC5} < 5.25V and 10.8V < V_{CC12} < 13.2V, 0°C ≤ T_A ≤ 70°C. Test conditions: V_{CC3} = V_{CC5}, V_{CC5} = 5V, V_{CC12} = 12V, T = 25°C.)

Parameter		Symbol	Test Conditions	LX1668 Min.	LX1668 Typ.	LX1668 Max.	Units
Reference & DAC							
Initial Accuracy		V_{CORE}	(Less 40mV output adaptive positioning), 1.3V ≤ V_{CORE} ≤ 35V, T = 25°C	-1		+1	%
Cumulative Regulation Accuracy			1.3V ≤ V_{CORE} ≤ 3.5V	-1.5		1.5	%
Timing							
Off Time		OT	V_{CORE} = 2.0V		2.4		µs
Swicthing Frequency		Freq	V_{CORE} = 1.3V to 3.5V		250		kHz
Error Comparator / CS-							
Input Bias Current		I_{FB}	1.0V < V_{SS} = V_{FB} < 3.5V		-0.3	-1	µA
E_C Delay to Output			Overdrive ≤ 5mV		100		ns
Current Sense +							
Input Resistance		R_{CORE}	0V < V_{FB} = V_{CORE} < 3.5V		12		kΩ
Pulse By Pulse Current Limit		V_{CLP}		45	60		mV
Current Sense Delay To Output			Overdrive ≤ 5mV		100		ns
Output Drivers							
Drive Rise Time, Fall Time		T_{RF}	C_L = 3000pF		100		ns
Drive High		V_{DH}	I_{SOURCE} = 20mA	10	11		V
Drive Low		V_{DL}	I_{SINK} = 20mA		0.1		V
UVLO and Soft-Start (SS)							
V_{CC5} Start-Up Threshold		V_{ST}	V_{CC12} > 3.9V	3.9	4.2	4.6	V
Hysteresis					0.10		V
SS Resistor		R_{SS}			18		kΩ
SS Output Enable		V_{EN}		0.4	0.5		V
Hiccup Duty Cycle		DC_{HIC}	C_{SS} = 0.1µF, V_{DAC} = 2.00V, F_{REQ} = 100Hz		10		%
Supply Current							
V_{CC12} Dynamic Supply Current		I_{CD}	Out Freq = 200kHz, C_L = 3000pF, Synch., V_{SS} > 0.5V		24		mA
Static Supply Current	12V	I_{VCC12}	V_{SS} < 0.5V		6	9	mA
	5V	I_{VCC5}	V_{SS} < 0.5V		13	18	mA
	3.3V	I_{VCC3}	V_{SS} < 0.5V		0.4	2	mA
Power Good / Over-Voltage Protection (OVP)							
Threshold			(V_{CORE} / V_{SET}) V_{CORE} rising, V_{OUT2} ≥ 2.0V	108	110	111	%
			(V_{CORE} / V_{SET}) V_{CORE} falling, V_{OUT2} ≥ 2.0V	90	91	92	%
Hysteresis					2		%
Power Good Voltage Low			I_{PWRGD} = 4mA		0.5	0.7	V
Over-Voltage Threshold			(V_{CORE} / V_{SET}), V_{CORE} rising	110	117	125	%
OVP Sourcing Current			V_{OVP} = 2.0V	35	60		mA
Fixed Linear Regulator (V_{OUT2})							
Voltage Reference Tolerance			V_{OUT2} = 2.5V, C_{OUT} = 220µF	-2.3		+2.0	%
Regulation			-10mA ≤ I_{OUT2} ≤ -150mA	-1		+1	%
Current Limit			V_{OUT2} ≤ 2V	250			mA
Linear Regulator Controller							
Voltage Reference Tolerance			V_{LFB} = 1.5V, C_{OUT} = 330µF	-2.3		+1.5	%
Source Current		I_{LDRV}	I_{LDRV} flows from V_{CC12}	30			mA
Sink Current		I_{LDRV}			0.2		mA
VID Pins							
Low Input		V_{IL}	Internally pulled up to V_{CC5} thru 30k			0.8	V
High Input		V_{IH}		2.0			V

ELECTRICAL CHARACTERISTICS

Table 1 - Adaptive Transient Voltage Output (Output Voltage Setpoint — Typical)

Processor Pins 0 = Low, 1 = High					Output Voltage (V_{SET})	
VID4	VID3	VID2	VID1	VID0	0.0A	Nominal Output* (V_{SET})
0	1	1	1	1	1.34V	1.30V
0	1	1	1	0	1.39V	1.35V
0	1	1	0	1	1.44V	1.40V
0	1	1	0	0	1.49V	1.45V
0	1	0	1	1	1.54V	1.50V
0	1	0	1	0	1.59V	1.55V
0	1	0	0	1	1.64V	1.60V
0	1	0	0	0	1.69V	1.65V
0	0	1	1	1	1.74V	1.70V
0	0	1	1	0	1.79V	1.75V
0	0	1	0	1	1.84V	1.80V
0	0	1	0	0	1.89V	1.85V
0	0	0	1	1	1.94V	1.90V
0	0	0	1	0	1.99V	1.95V
0	0	0	0	1	2.04V	2.00V
0	0	0	0	0	2.09V	2.05V
1	1	1	1	1	2.04V	2.00V
1	1	1	1	0	2.14V	2.10V
1	1	1	0	1	2.24V	2.20V
1	1	1	0	0	2.34V	2.30V
1	1	0	1	1	2.44V	2.40V
1	1	0	1	0	2.54V	2.50V
1	1	0	0	1	2.64V	2.60V
1	1	0	0	0	2.74V	2.70V
1	0	1	1	1	2.84V	2.80V
1	0	1	1	0	2.94V	2.90V
1	0	1	0	1	3.04V	3.00V
1	0	1	0	0	3.14V	3.10V
1	0	0	1	1	3.24V	3.20V
1	0	0	1	0	3.34V	3.30V
1	0	0	0	1	3.44V	3.40V
1	0	0	0	0	3.54V	3.50V

* Nominal = DAC setpoint voltage with no adaptive output voltage positioning.

Note:

Adaptive Transient Voltage Output

In order to improve transient response a 40mV offset is built into the voltage comparator. At high currents, the peak output voltage will be lower than the nominal set point , as shown in Figure 4. The actual output voltage will be a function of the sense resistor, output current and output ripple.

CHARACTERISTICS CURVES

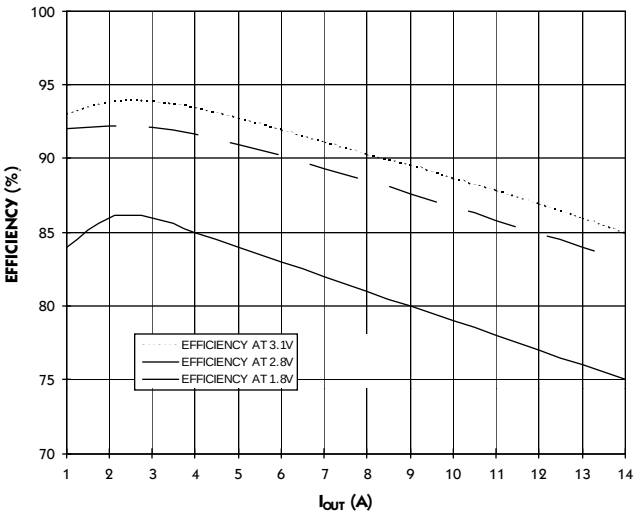


FIGURE 1 — Efficiency Test Results: Non-Synchronous Operation, V_{IN} = 5V

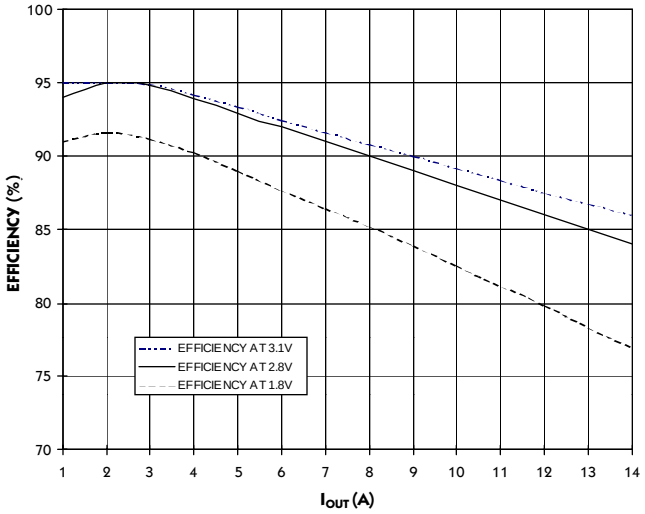


FIGURE 2 — Efficiency Test Results: Synchronous Operation, V_{IN} = 5V

BLOCK DIAGRAM

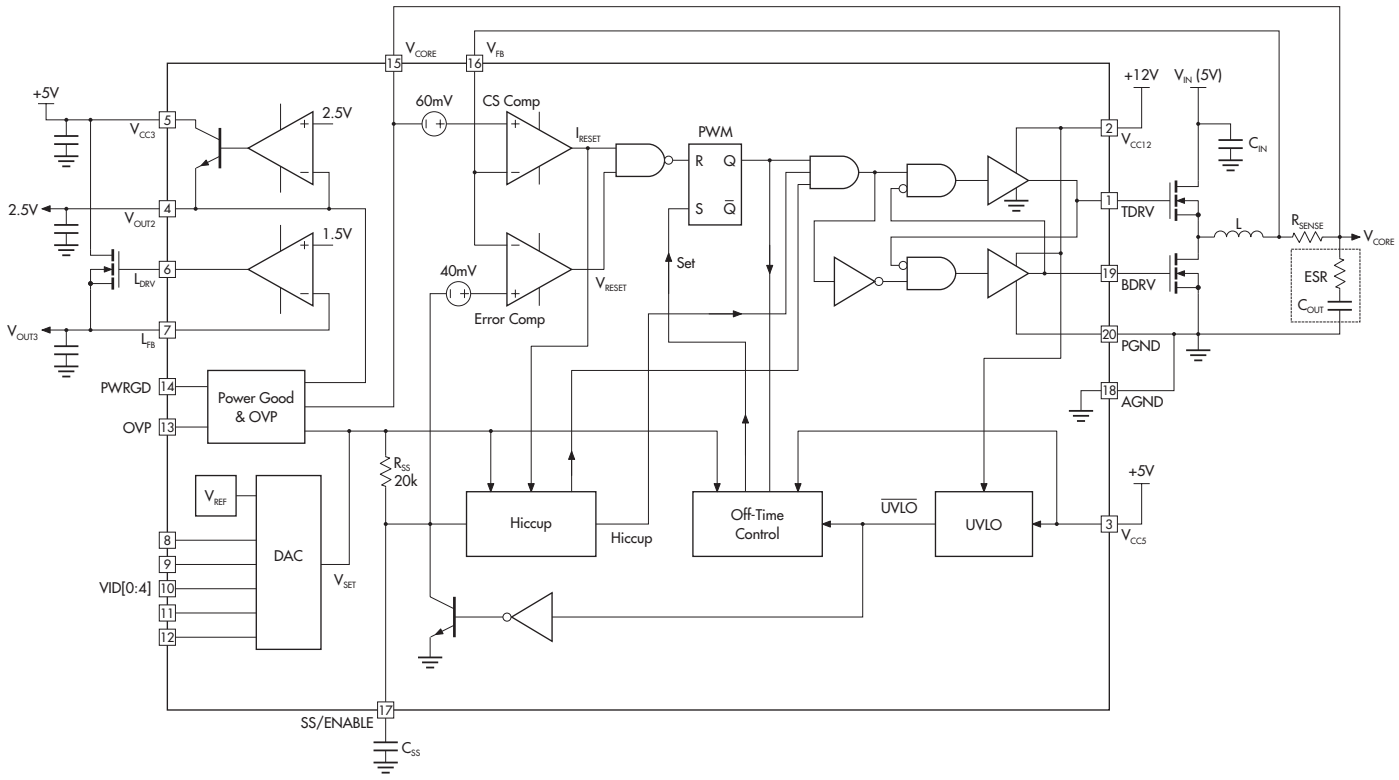


FIGURE 3 — Block Diagram

FUNCTIONAL PIN DESCRIPTION

Pin Number	Pin Designator	Description
1	TDRV	Gate drive to the top FET.
2	V_{CC12}	+12V supply for the gate drivers. If 12V is not available in the application, a bootstrap circuit is required to create the biasing voltage for the FET gate drivers.
3	V_{CC5}	+5V supply for internal biasing and power to the IC.
4	V_{OUT2}	Fixed 2.5V internal LDO regulator output.
5	V_{CC3}	Input for the 2.5V internal LDO regulator — Recommended to be connected to 5V.
6	L_{DRV}	Adjustable LDO driver output. Connect to gate of MOSFET.
7	L_{FB}	Voltage feedback pin of the adjustable LDO regulator (1.5V).
8 9 10 11 12	VID0 VID1 VID2 VID3 VID4	Input pins to the DAC. The output of the DAC sets the nominal voltage of the PWM output (see Table 1). These inputs are TTL-compatible.
13	OVP	Over-voltage protection: this pin is pulled to above 2V when the switcher output is above 17% of its set voltage. This pin is capable of sourcing 40mA current, and can be used to drive an SCR crowbar or as a signal to turn off the main power supply.
14	PWRGD	Open collector output, pulled down when the core voltage is not within ±10% of the DAC output or the fixed 2.5V LDO output is below 2.0V.
15	V_{CORE}	Output (CPU core) voltage, connected to the output of the regulator (after the sense resistor). This pin is also connected to the power good and the over current comparators in the IC.
16	V_{FB}	Dual function pin for feedback and current sensing. The peak voltage of this is set 40mV above the nominal set-point (VID) voltage. When the voltage difference between this pin and V_{OUT} (pin 15) exceeds 60mV, the over current comparator will be tripped. The over current tripping level can be set as $I = 60mV/R_{SENSE}$ where R_{SENSE} is the sensing resistance (see Application Note section).
17	SS/ENABLE	Soft-startup and hiccup capacitor pin. During startup, the voltage of this pin controls the core voltage. An internal 20kΩ resistor and the external capacitor set the time constant for the soft-startup. Soft-start does not begin until the supply voltage exceeds the UVLO threshold. When over-current occurs, this capacitor is used for timing the hiccup. See Application Information for more detail. The PWM output can be disabled by pulling the SS/ENABLE pin below 0.5V.
18	AGND	Analog ground.
19	BDRV	Bottom FET drive.
20	PGND	Power ground. Ground return for FET drivers.

THEORY OF OPERATION

SWITCHER OUTPUT VOLTAGE REGULATION

Refer to the IC Block Diagram and the Product Highlight circuit. When the top MOSFET turns ON, the inductor current increases. The voltage at V_{FB} pin increases due to the ESR of the output capacitor and the current-sensing resistor. When the V_{FB} pin voltage reaches the threshold voltage of the error comparator, V_{SET} (the DAC output set-point voltage) plus 40mV offset, the PWM latch is reset. Consequently, the top MOSFET turns OFF and the bottom (synchronous) MOSFET turns ON. The off-time control block controls the off-time of the top MOSFET. During the off-time, the inductor current and the V_{FB} pin voltage decrease. As the off-time finishes, the synchronous MOSFET turns OFF and the top MOSFET turns ON again, repeating the previous cycle. A break-before-make circuit prevents simultaneous conduction of the two MOSFET's.

The 40mV offset to the set voltage enhances the transient response of the output voltage, as shown in Figure 4 below.

- The peak voltage at the V_{FB} pin is 40mV higher than the set voltage and its average is the peak voltage minus the ripple voltage at V_{FB} pin.
- The output voltage is the voltage at the V_{FB} pin minus the voltage drop across the current sensing resistor ($I * R_{SENSE}$).
- At light loads, the voltage drop across the sensing resistor is small; hence, the output voltage is approximately the voltage at the V_{FB} pin (approximately 40mV higher than the set voltage, V_{SET}).
- At heavy loads, larger current flows in the sense resistor, therefore, the voltage drop is higher and the output voltage is lower.

This adaptive positioning of the output voltage as the load changes allows a greater output voltage excursion during a fast step-load transient and requires fewer output capacitors to meet the transient-response specification.

POWER UP and INITIALIZATION

At power up, the LX1668 monitors the supply voltage to both the +5V and the +12V pins (there is no special requirement for the sequence of the two supplies). Before both supplies reach their under-voltage lock-out (UVLO) thresholds, the soft-start (SS) pin is held low to prevent soft-start from beginning; the off-time control is disabled and the top MOSFET is kept OFF. The two LDO regulators are designed not to over-voltage regardless of supply voltages. After both supplies pass the UVLO thresholds, the circuit begins soft-start.

SOFT-START

Once the supplies are above the UVLO threshold, the soft-start capacitor begins to be charged up by the set voltage (DAC output) through a 20kΩ internal resistor. The capacitor voltage at the SS pin rises as a simple RC circuit. The SS pin plus a 40mV offset is connected to the error comparator's non-inverting input that controls the output peak voltage. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor.

The simple RC soft-start allows the output to rise faster at the beginning and slower at the end of the soft-start interval. Thus, the required charging current into the output capacitor is less at the end of the soft-start interval so decreasing the possibility of an over-current. A comparator monitors the SS pin voltage and indicates the end of soft-start when SS pin voltage reaches 95% of V_{SET}. See Application Information section for further details.

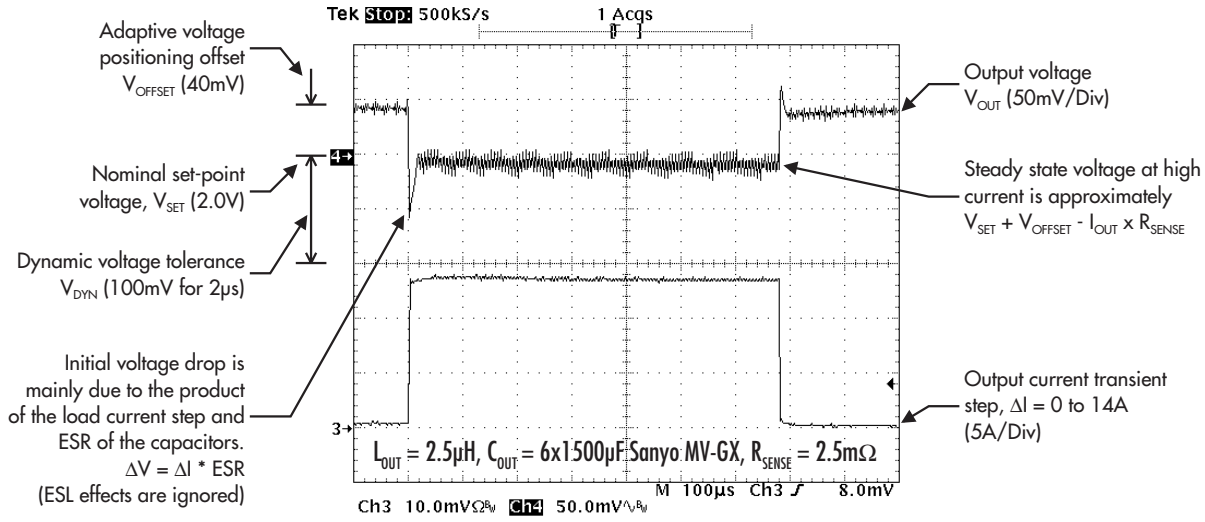


FIGURE 4 — Adaptive Voltage Positioning

THEORY OF OPERATION

OVER-CURRENT PROTECTION (OCP) and HICCUP

The over-current protection function is tripped when the inductor current exceeds its maximum limit. The current is sensed with a resistor in series with the inductor. When the voltage across the sensing resistor exceeds the 60mV threshold, the OCP comparator outputs a signal to reset the PWM latch and to start hiccup mode. The soft-start capacitor, C_{SS}, is discharged slowly (10 times slower than when being charged up by R_{SS}). When the voltage on the SS/ENABLE pin reaches a 0.3V threshold, hiccup finishes and the circuit soft-starts again. During hiccup, the top MOSFET is OFF and the bottom MOSFET remains ON.

Hiccup is disabled during the soft-start interval, allowing the circuit to start up with the maximum current. If the rise speed of the output voltage is too fast, the required charging current to the output capacitor may be higher than the limit-current. In this case, the peak inductor current is regulated to the limit-current by the current-sense comparator. The top MOSFET is turned on at the end of the controlled off-time and is turned off when the inductor current reaches the limit. If the inductor current still reaches its limit after the soft-start finishes, the hiccup is triggered again. The hiccup ensures the average heat generation on both MOSFET's and the average current to be much less than that in normal operation, if the output has a short circuit.

OVER-VOLTAGE PROTECTION (OVP)

The output voltage is inherently protected from an over-voltage situation because of the peak-voltage control mechanism. Whenever the V_{FB} pin voltage is higher than the set voltage by 40mV, the top MOSFET is turned off and the bottom MOSFET is turned on. In the case that a fault condition occurs where the output voltage exceeds the 117% V_{SET} threshold, the OVP comparator will pull up the OVP pin to 2 volts. The OVP pin has a 40mA source current capability, so it can be used to trigger an SCR crowbar or shut off the main power supply.

OFF-TIME CONTROL and SWITCHING FREQUENCY

An internal timer controls the off-time of the top MOSFET so that the switching frequency is constant at 200 kHz under steady-state operation. The timer begins timing once the PWM latch is reset and set the PWM flip-flop again when the off-time finishes. The off-time is controlled to be:

$$T_{OFF} = 5\mu s(1-V_{OUT}/V_{CC5})$$

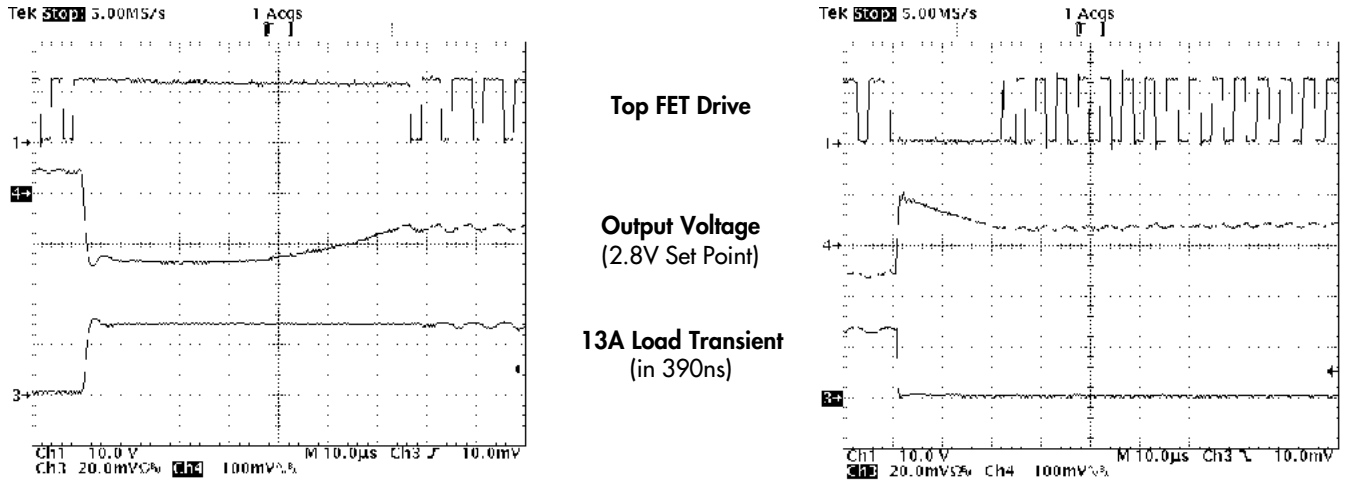
For a buck converter, the switching frequency is

$$f_{SW} = (1- V_{OUT}/V_{CC5})/T_{OFF}$$

Therefore, the switching frequency is nearly constant in steady state operation. During transient loading, the top drive can remain switched on or off until the output voltage is within specification (see Figure 5) in order to reduce transient response time.

POWER GOOD OUTPUT

An open-collector output, PWRGD, is provided to indicate the status of the output voltages. PWRGD presents high impedance when the switcher output voltage is within ±10% of its set voltage and the fixed 2.5V internal LDO regulator output is above 2.0V. Otherwise, PWRGD presents a low impedance path to ground.



V_{IN} = 5V, V_{OUT} = 2.8V, L_{OUT} = 5µH, C_{OUT} = 3 x 1500µF, f = 200kHz

FIGURE 5 — Top FET Drive During Transient Load Conditions

BILL OF MATERIALS

LX1668 Bill of Materials (Refer to Product Highlight)

Ref	Description	Part Number / Manufacturer	Qty.
U1	Controller IC	LX1668 - LinFinity	1
C1	Capacitor, 1500µF, 6.3V, 44mΩ ESR	MV-GX Sanyo	6
C2	Capacitor, 1500µF, 6.3V, 44mΩ ESR	MV-GX Sanyo	3
C4, C6	Capacitor, 330µF, Electrolytic	MV-GX Sanyo	2
C5	Capacitor, 22µF, Electrolytic	MV-GX Sanyo	2
C7, C8, C9	Capacitor, 1µF, SMD		2
C3	Capacitor, 1µF, SMD, 16V		1
CSS	Capacitor, 0.1µF, SMD		1
Q1	MOSFET (low $R_{DS(ON)}$)	IRL3102/3103, International Rectifier	1
Q2	MOSFET (low $R_{DS(ON)}$)	IRL3303/3103, International Rectifier	1
Q3	MOSFET	IRLZ44N, International Rectifier	1
R_{SENSE}	Sense Resistor, 2.5mΩ	PCB trace	1
R1	Resistor, 0Ω (see Table 6)	SMD	1
R2	Resistor, 2.5mΩ (see Table 6)	SMD	1
L1	Inductor, 2 - 3µH	HM00-97713 or HM00-98637, BI Technologies	1
L2	Inductor, 1µH		1
Total Number of Components			**26**
Optional Components for Over-Voltage Protection and Power Good Signal			
Q4	SCR	2N6504	1
R3	Resistor, 10kΩ	SMD	1

APPLICATION CIRCUIT

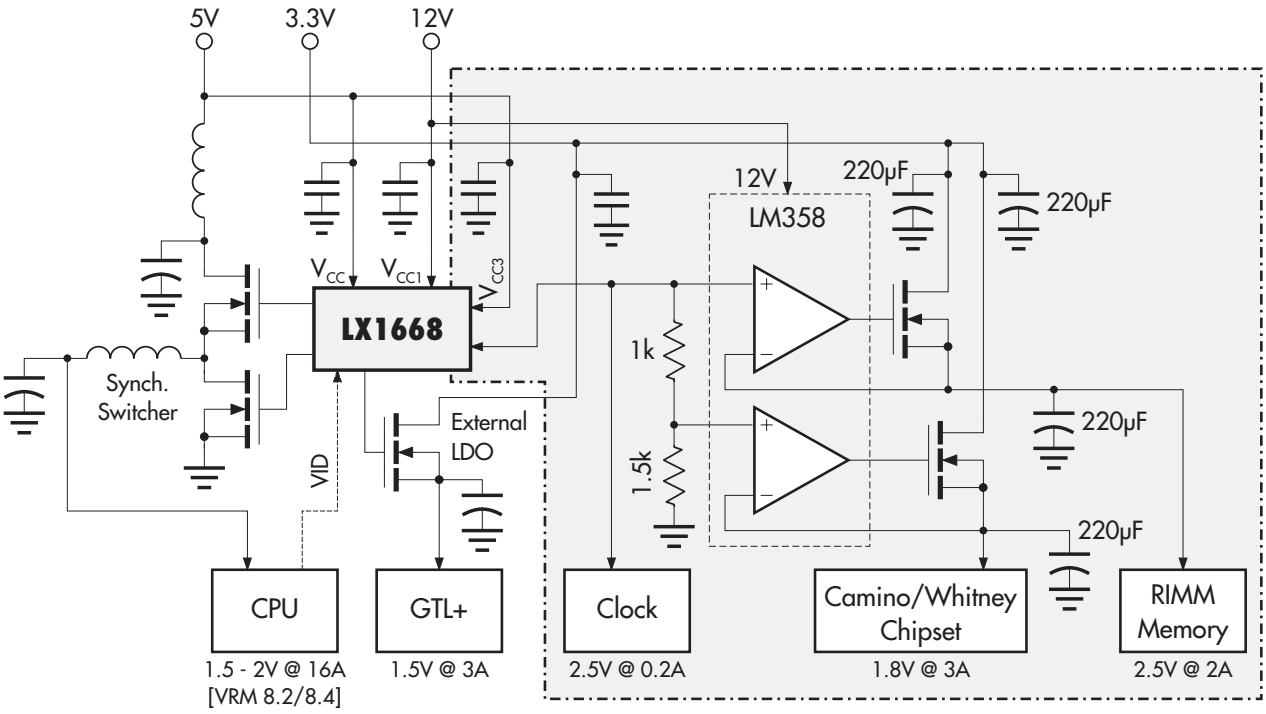


FIGURE 6 — Pentium III Processor Power Supply (Whitney / Camino Chipsets)

APPLICATION INFORMATION

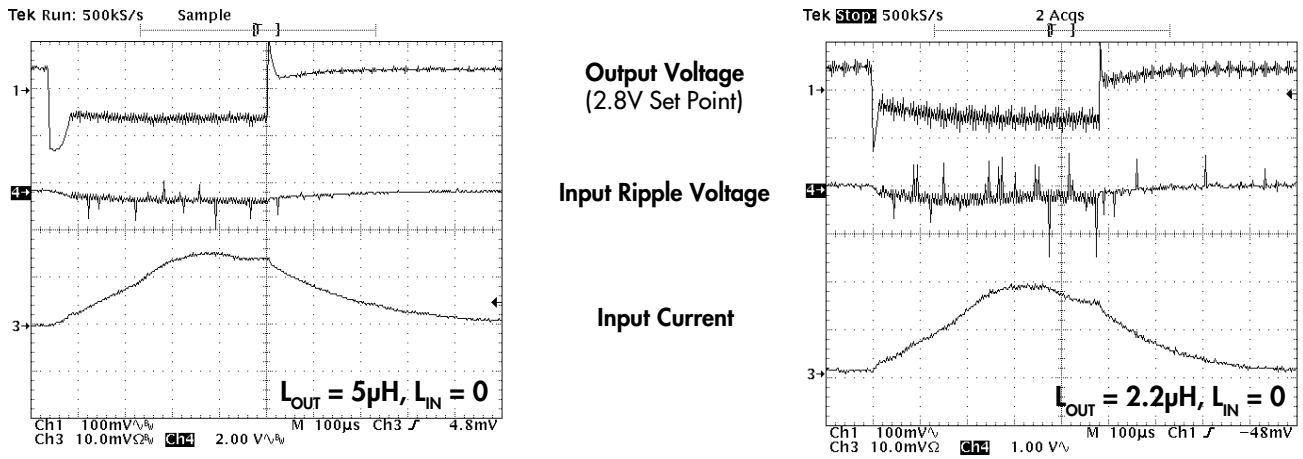


FIGURE 7 — Effect Of Different Inductor Values

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient.

The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR * I_{RIPPLE}$$

where

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{f_{SW} * L} * \frac{V_{OUT}}{V_{IN}}$$

I_{RIPPLE} is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

I_{RIPPLE} should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. The inductor-current rise and fall times are:

$$T_{RISE} = L * \Delta I/(V_{IN} - V_{OUT})$$

and

$$T_{FALL} = L * \Delta I/V_{OUT}$$

When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance.

For higher current applications, such as Pentium II processors, a 2.5µH inductor is recommended for the best combination of fast response and manageable ripple voltage. For lower current applications, such as Pentium and other Socket 7 processors, a 5µH inductor is sufficient. The effect of different inductor values is shown in Figure 7 above.

Notice how, with a smaller inductor, transient response time is improved, but at the expense of much greater ripple.

INPUT INDUCTOR

In order to supply faster transient load changes, a smaller output inductor is needed. However, reducing the size of the output inductor will result in a higher ripple voltage on the input supply, as shown in Figure 8 above. This noise on the 5V rail can affect other system components, such as graphics cards. It is recommended that a 1 – 1.5µH inductor, L2, is used on input to the regulator, to filter the ripple on the 5V supply. Ensure that this inductor has the same current rating as the output inductor.

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirement usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR * (I_{RIPPLE} + \Delta I) < V_{EX}$$

where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage

APPLICATION INFORMATION

OUTPUT CAPACITOR (continued)

excursion in the transient. Adaptive voltage positioning increases the value of V_{EX}, allowing a higher ESR value and reducing the cost of the output capacitor. Typically, the positioning voltage is 40mV (peak), using the LX1668, and the transient tolerance is 100mV, resulting in a V_{EX} of 140mV (see Figure 4).

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increases with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible, however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Linfinity's demonstration boards use Sanyo MV-GX filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The Oscon series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The MV-GX series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

INPUT CAPACITOR

The input capacitor and the input inductor are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling the buck converter. The capacitor should be rated to handle the RMS current requirement. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

where I_L is the inductor current and the d is the duty cycle. The maximum value, when d = 50%, $I_{RMS} = 0.5I_L$. For 5V input and output in the range of 2 to 3V, the required RMS current is very close to $0.5I_L$.

A high-frequency (ceramic) capacitor should be placed across the drain of the top MOSFET and the source of the bottom one to avoid ringing due to the parasitic inductor being switched ON and OFF. See capacitor C7 in the Product Highlight.

SOFT-START CAPACITOR

The value of the soft-start capacitor determines how fast the output voltage rises and how large the inductor current is required to charge the output capacitor. The output voltage will follow the voltage at SS pin if the required inductor current does not exceed the maximum current in the inductor.

SOFT-START CAPACITOR (continued)

The SS pin voltage can be expressed as:

$$V_{SS} = V_{SET}(1-e^{-t/R_{SS}C_{SS}})$$

where V_{SET} is the output of the DAC. R_{SS} and C_{SS} are soft start resistor and capacitor, as shown in Figure 4. The required inductor current for the output capacitor to follow the SS-pin voltage equals the required capacitor current plus the load current. The soft-start capacitor should be selected so that the overall inductor current does not exceed it maximum.

The capacitor current to follow the SS-pin voltage is:

$$I_{Cout} = C_{OUT}\frac{dV}{dt} = \frac{C_{OUT}}{C_{SS}} * e^{(t/R_{SS}C_{SS})}$$

where C_{OUT} is the output capacitance. The typical value of C_{SS} should be in the range of 0.1 to 0.2µF.

During the soft-start interval, before the PWRGD signal becomes valid, the load current from a microprocessor is negligible; therefore, the capacitor current is approximately the required inductor current.

CURRENT LIMIT

Current limiting occurs when a sensed voltage, proportional to load current, exceeds the current-sense comparator threshold value. The current can be sensed either by using a fixed sense resistor in series with the inductor to cause a voltage drop proportional to current, or by using a resistor and capacitor in parallel with the inductor to sense the voltage drop across the parasitic resistance of the inductor. The LX1668 has a threshold of 60mV.

Sense Resistor

The current sense resistor, R_{SENSE}, is selected according to the formula:

$$R_{SENSE} = V_{TRIP} / I_{TRIP}$$

Where V_{TRIP} is the current sense comparator threshold (60mV) and I_{TRIP} is the desired current limit. Typical choices are shown below.

TABLE 2 - Current Sense Resistor Selection Guide

Load	Sense Resistor Value
Pentium-Class Processor (<10A)	5mΩ
Pentium II Class (>10A)	2.5mΩ

A smaller sense resistor will result in lower heat dissipation (I^2R) and also a smaller output voltage droop at higher currents.

APPLICATION INFORMATION

CURRENT LIMIT (continued)

There are several alternative types of sense resistor. The surface-mount metal "staple" form of resistor has the advantage of exposure to free air to dissipate heat and its value can be controlled very tightly. Its main drawback, however, is cost. An alternative is to construct the sense resistor using a copper PCB trace. Although the resistance cannot be controlled as tightly, the PCB trace is very low cost.

PCB Sense Resistor

A PCB sense resistor should be constructed as shown in Figure 8. By attaching directly to the large pads for the capacitor and inductor, heat is dissipated efficiently by the larger copper masses. Connect the current sense lines as shown to avoid any errors.

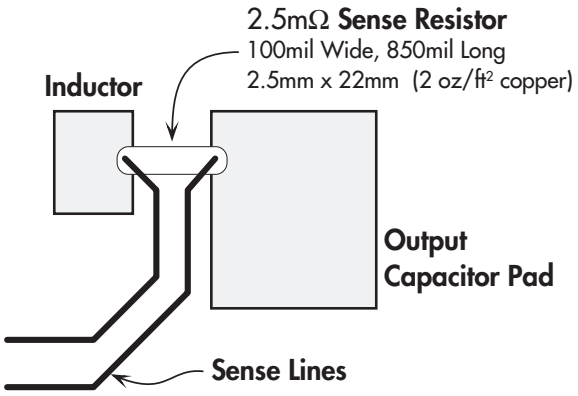


FIGURE 8 — Sense Resistor Construction Diagram

Recommended sense resistor sizes are given in the following table:

TABLE 3 - PCB Sense Resistor Selection Guide

Copper Weight	Copper Thickness	Desired Resistor Value	Dimensions (w x l) mm	Dimensions (w x l) inches
2 oz/ft²	68µm	2.5mΩ	2.5 x 22	0.1 x 0.85
		5mΩ	2.5 x 43	0.1 x 1.7

Loss-Less Current Sensing Using Resistance of Inductor

Any inductor has a parasitic resistance (R_L) which causes a DC voltage drop when current flows through the inductor. Figure 9 shows a sensor circuit comprising of a surface mount resistor, R_S, and capacitor, C_S, in parallel with the inductor, eliminating the current sense resistor.

The current flowing through the inductor is a triangle wave. If the sensor components are selected such that:

$$L/R_L = R_S * C_S$$

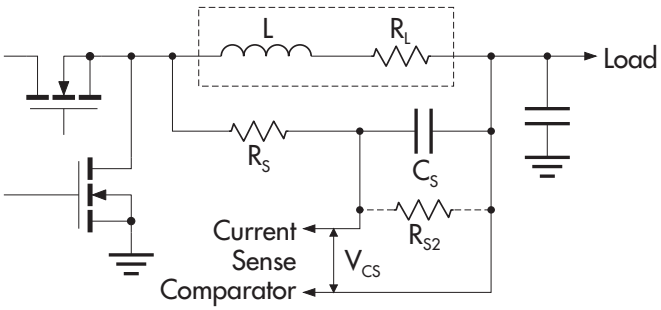


FIGURE 9 — Current Sense Circuit

The voltage across the capacitor will be equal to the current flowing through the resistor, i.e.

$$V_{CS} = I_L R_L$$

Since V_{CS} reflects the inductor current, by selecting the appropriate R_S and C_S, V_{CS} can used to sense current.

Design Example

(Pentium II circuit, with a maximum static current of 14.2A)

The gain of the sensor can be characterized as:

The dc/static tripping current $I_{trip,S}$ satisfies:

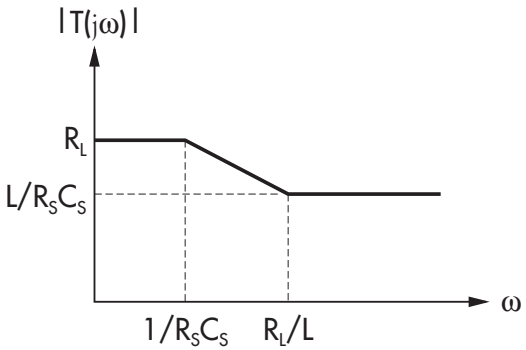


FIGURE 10 — Sensor Gain

$$I_{trip,S} = \frac{V_{trip}}{R_L}$$

Select $L/R_S C_S \leq R_L$ to have higher dynamic tripping current than the static one. The dynamic tripping current $I_{trip,d}$ satisfies:

$$I_{trip,d} = \frac{V_{trip}}{L/(R_S C_S)}$$

APPLICATION INFORMATION

CURRENT LIMIT (continued)

General Guidelines for Selecting R_S, C_S, and R_L

$$R_L = \frac{V_{trip}}{I_{trip,S}} \qquad \text{Select: } R_S \le 10\ k\Omega$$

and C_S according to: $$C_{S\,n} = \frac{L_n}{R_L R_S}$$

The above equation has taken into account the current-dependency of the inductance.

Typical values are: R_L = 3mΩ, R_S = 9kΩ, C_S = 0.1µF, and L is 2.5µH at 0A current.

In cases where R_L is so large that the trip point current would be lower than the desired short-circuit current limit, a resistor (R_{S2}) can be put in parallel with C_S, as shown in Figure 10. The selection of components is as follows:

$$\frac{R_{L\,(Required)}}{R_{L\,(Actual)}} = \frac{R_{S2}}{R_{S2} + R_S}$$

$$C_S = \frac{L}{R_{L\,(Actual)} * (R_{S2} // R_S)} = \frac{L}{R_{L\,(Actual)}} * \frac{R_S + R_{S2}}{R_{S2} * R_S}$$

Again, select (R_{S2}//R_S) < 10kΩ. See Application Note AN-7 for more information.

OUTPUT ENABLE

The LX1668 FET driver outputs are driven to ground by pulling the soft-start pin below 0.5V.

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage is set by the DAC with a 5-bit digital voltage-identification (VID) code input (see Table 1). The DAC input is designed to be compatible with digital circuits. The VID code may be hard-wired into the package of the processor [as in the case of a Pentium II or Pentium Pro processor]. If the processor does not have a VID code, the output voltage can be set by means of a DIP-switch, jumpers or TTL-compatible digital circuits. When using a DIP-switch or jumpers, connect the VID pin to ground (DIP-switch ON) for a low or "0" signal and leave the VID pin open (DIP-switch OFF) for a high or "1" signal.

FET SELECTION

To insure reliable operation, the operating junction temperature of the FET switches must be kept below certain limits. The Intel specification states that 115°C maximum junction temperature should be maintained with an ambient of 50°C. This is achieved by properly derating the part, and by adequate heat sinking. One of the most critical parameters for FET selection is the $R_{DS(ON)}$ resistance. This parameter directly contributes to the power dissipation of the FET devices, and thus impacts heat sink design, mechanical layout, and reliability. In general, the larger the current handling capability of the FET, the lower the $R_{DS(ON)}$ will be, since more die area is available.

FET SELECTION (continued)

TABLE 4 - FET Selection Guide

This table gives selection of suitable FETs from International Rectifier.

Device	$R_{DS(ON)}$ @ 10V (mΩ)	I_D @ T_C = 100°C	Max. Break-down Voltage
IRL3803	6	83	30
IRL22203N	7	71	30
IRL3103	14	40	30
IRL3102	13	56	20
IRL3303	26	24	30
IRL2703	40	17	30

All devices in TO-220 package. For surface mount devices (TO-263 / D^2-Pak), add 'S' to part number, e.g. IRL3103S.

The recommended solution is to use IRL3102 for the high side and IRL3303 for the low side FET, for the best combination of cost and performance. Alternative FET's from any manufacturer could be used, provided they meet the same criteria for $R_{DS(ON)}$.

Heat Dissipated In Upper MOSFET

The heat dissipated in the top MOSFET will be:

$$P_D = (I^2 * R_{DS(ON)} * Duty\ Cycle) + (0.5 * I * V_{IN} * t_{SW} * f_S)$$

Where t_{SW} is switching transition line for body diode (~100ns) and f_S is the switching frequency.

For the IRL3102 (13mΩ $R_{DS(ON)}$), converting 5V to 2.0V at 15A will result in typical heat dissipation of 1.92W.

Synchronous Rectification – Lower MOSFET

The lower pass element can be either a MOSFET or a Schottky diode. The use of a MOSFET (synchronous rectification) will result in higher efficiency, but at higher cost than using a Schottky diode (non-synchronous).

Power dissipated in the bottom MOSFET will be:

$$P_D = I^2 * R_{DS(ON)} * [1 - Duty\ Cycle] = 3.51W$$

[IRL3303 or 1.76W for the IRL3102]

Non-Synchronous Operation - Schottky Diode

A typical Schottky diode, with a forward drop of 0.6V will dissipate 0.6 * 15 * [1 – 2/5] = 5.4W (compared to the 1.8 to 3.5W dissipated by a MOSFET under the same conditions). This power loss becomes much more significant at lower duty cycles. The use of a dual Schottky diode in a single TO-220 package (e.g. the MBR2535) helps improve thermal dissipation.

APPLICATION INFORMATION

LINEAR REGULATOR

Capcitor Selection

The internal LDO regulator and the external linear regulator driver are both designed to be insensitive to selection of capacitors. Most Aluminum or Tantalum electrolytic capacitor will make for suitable operation. Capacitors should be chosen so that the voltage drop during a load transient does not exceed the relevant specifications.

Internal LDO

A 22µF aluminum electrolytic is recommended for optimal performance for power clock circuits at 2.5V.

External LDO

A 330µF aluminum electrolytic is recommended for powering V_{TT} at 1.5V. This will provide sufficient voltage hold-up for any expected transients on the GTL+ Bus.

Internal Fixed-Voltage LDO Regulator

The internal LDO regulator has a fixed 2.5V output voltage and is intended for powering the clock circuit. Its current is limited to 250mA. The limitation for using this LDO regulator is heat dissipation. Power dissipation should not exceed the limit of 400mW on average for SOIC package and 300mW for TSSOP package.

The power dissipated in the internal LDO is as follows:

$$P_D = (V_{CC3} - V_{OUT2}) * I_{OUT2}$$

where I_{OUT2} is the output current from the linear regulator.

V_{CC3} can be connected to 5V or 3.3V, but 5V is recommended for optimal performance.

Adjustable External LDO Regulator

The LX1668 has a linear regulator driver function. A low dropout linear regulator can be constructed by connecting an external MOSFET to the L_{DRV} and L_{FB} pins. The MOSFET can provide an output with a minimum voltage of 1.5V. The dropout voltage across the regulator is the product of $R_{DS(ON)}$ and current – this limits the upper voltage.

The linear regulator output, V_{OUT3}, can be used to power GTL+ Bus circuits in a Pentium II processor application at 1.5V. In this case, the output can be connected directly to the L_{FB} pin without the use of resistors to set the output voltage. If an alternative output voltage is required, a resistor divider sets the output as follows:

$$V_{OUT3} = 1.5V * (1+R_1/R_2)$$

TABLE 6 -
Resistors Settings for Linear Regulator Output Voltage

Nominal Set Point (V)	R1 (kΩ)	R2 (kΩ)	V_{OUT} (V)
3.3	12	10	3.30
3.2	11.3	10	3.20
3.1	11.3	10.7	3.08
3.0	11	11	3.00
2.9	10.3	11	2.90
2.8	10	11.5	2.80
2.7	10	12.4	2.71
2.6	10	13.7	2.59
2.5	9.76	14.7	2.50
2.4	8.87	14.7	2.41
2.3	8.87	16.5	2.31
2.2	8.87	18.7	2.21
2.1	8.87	22.1	2.10
2.0	8.87	26.7	2.00
1.9	8.87	21	2.13
1.8	7.15	35.7	1.80
1.7	7.15	53.6	1.70
1.6	7.15	100	1.61
1.5	0	50	1.50

The maximum output current from the linear regulator section is around 5 - 7A, and is limited only by the MOSFET's thermal dissipation performance (Power dissipation is equal to the voltage drop across the MOSFET multiplied by the current; $P_D = [V_{IN} - V_{OUT3}] * I_{OUT3}$). For this reason, it is preferable to use a 3.3V supply when powering a 1.5V GTL+ Bus using the external LDO.

For example, the heat dissipated in converting 3.3V to 1.5V at 3A would be:

$$P_D = (3.3 - 1.5) * 3 = 5.4W$$

Note that the MOSFET requires the same heatsink as would be necessary for a monolithic LDO such as the LX8384.

The dropout voltage of the linear regulator will be determined by the $R_{DS(ON)}$ of the MOSFET ($V_{DO} = R_{DS(ON)} * I_{I/O}$). Using a 2SK1388 at 5A, the worst case dropout voltage will be 37mΩ * 5A = 185mV. Note that the $R_{DS(ON)}$ does not affect the power dissipation, only dropout voltage. For reasons of economy, choose a FET with higher $R_{DS(ON)}$ than that used for the PWM output stages.

Disabling Linear Output

Linear regulator output can be disabled by pulling feedback pin (L_{FB}) up to 3.3V or 5V as shown in Figure 11. This pin should not be pulled higher than 5V.

TABLE 7 - Linear Enable (LIN EN) Function Table

LIN EN	LIN OUTPUT
H	Disabled
L	Enabled

APPLICATION INFORMATION

LINEAR REGULATOR (continued)

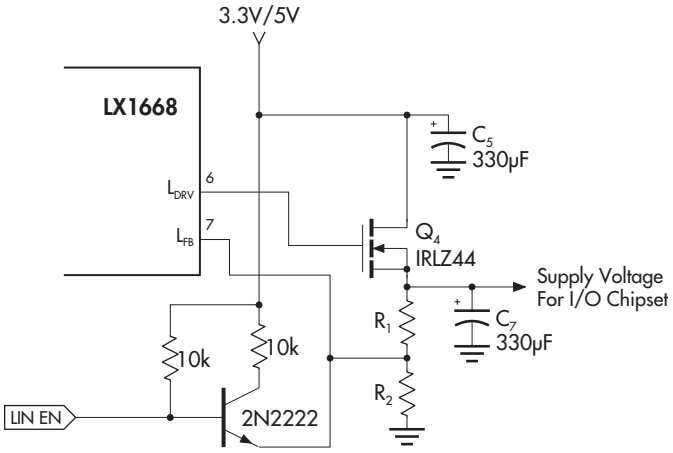


FIGURE 11 — Enabling Linear Regulator

LAYOUT GUIDELINES - THERMAL DESIGN

A great deal of time and effort were spent optimizing the thermal design of the demonstration boards. Any user who intends to implement an embedded motherboard would be well advised to carefully read and follow these guidelines. If the FET switches have been carefully selected, external heatsinking is generally not required. However, this means that copper trace on the PC board must now be used. This is a potential trouble spot; as much copper area as possible must be dedicated to heatsinking the FET switches, and the diode as well if a non-synchronous solution is used.

In our demonstration board, heatsink area was taken from internal ground and V_{CC} planes which were actually split and connected with VIAS to the power device tabs. The TO-220 and TO-263 cases are well suited for this application, and are the preferred packages. Remember to remove any conformal coating from all exposed PC traces which are involved in heatsinking.

General Notes

As always, be sure to provide local capacitive decoupling close to the chip. Be sure use ground plane construction for all high-frequency work. Use low ESR capacitors where justified, but be alert for damping and ringing problems. High-frequency designs demand careful routing and layout, and may require several iterations to achieve desired performance levels.

LAYOUT GUIDELINES - THERMAL DESIGN (continued)

Power Traces

To reduce power losses due to ohmic resistance, careful consideration should be given to the layout of traces that carry high currents. The main paths to consider are:

- Input power from 5V supply to drain of top MOSFET.
- Trace between top MOSFET and lower MOSFET or Schottky diode.
- Trace between lower MOSFET or Schottky diode and ground.
- Trace between source of top MOSFET and inductor, sense resistor and load.
- Current traces on both LDO sections

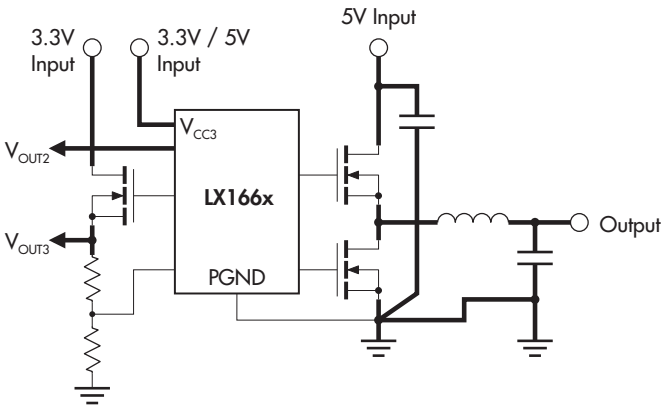


FIGURE 12 — Power Traces

All of these traces should be made as wide and thick as possible, in order to minimize resistance and hence power losses. It is also recommended that, whenever possible, the ground, input and output power signals should be on separate planes (PCB layers). See Figure 12 – bold traces are power traces.

Input Decoupling Capacitors

Ensure that capacitors C8 and C3 are placed as close to the IC as possible to minimize the effects of noise on the device.

Layout Assistance

Please contact Linfinity's Applications Engineers for assistance with any layout or component selection issues. A Gerber file with layout for the most popular devices is available upon request.

Evaluation boards are also available upon request. Please check Linfinity's web site for further application notes.