

74LVT125; 74LVTH125

3.3 V quad buffer; 3-state

Rev. 7 — 31 May 2016

Product data sheet

1. General description

The 74LVT125; 74LVTH125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125; 74LVTH125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$ and $\overline{4OE}$), each controlling one of the 3-state outputs.

2. Features and benefits

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883 method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

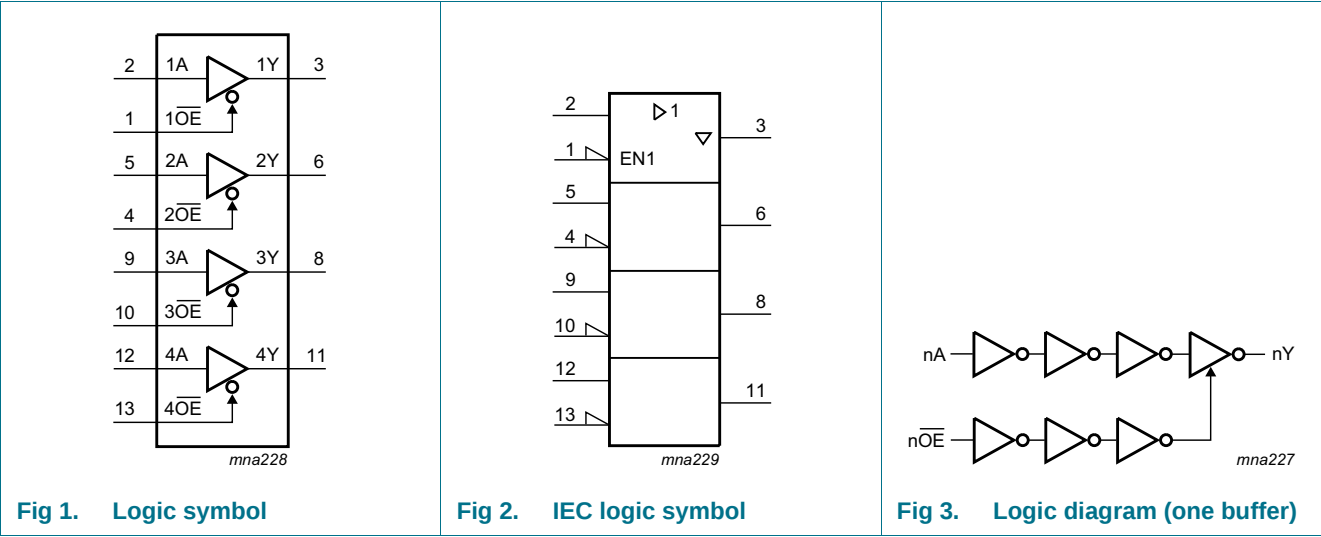


3. Ordering information

Table 1. Ordering information

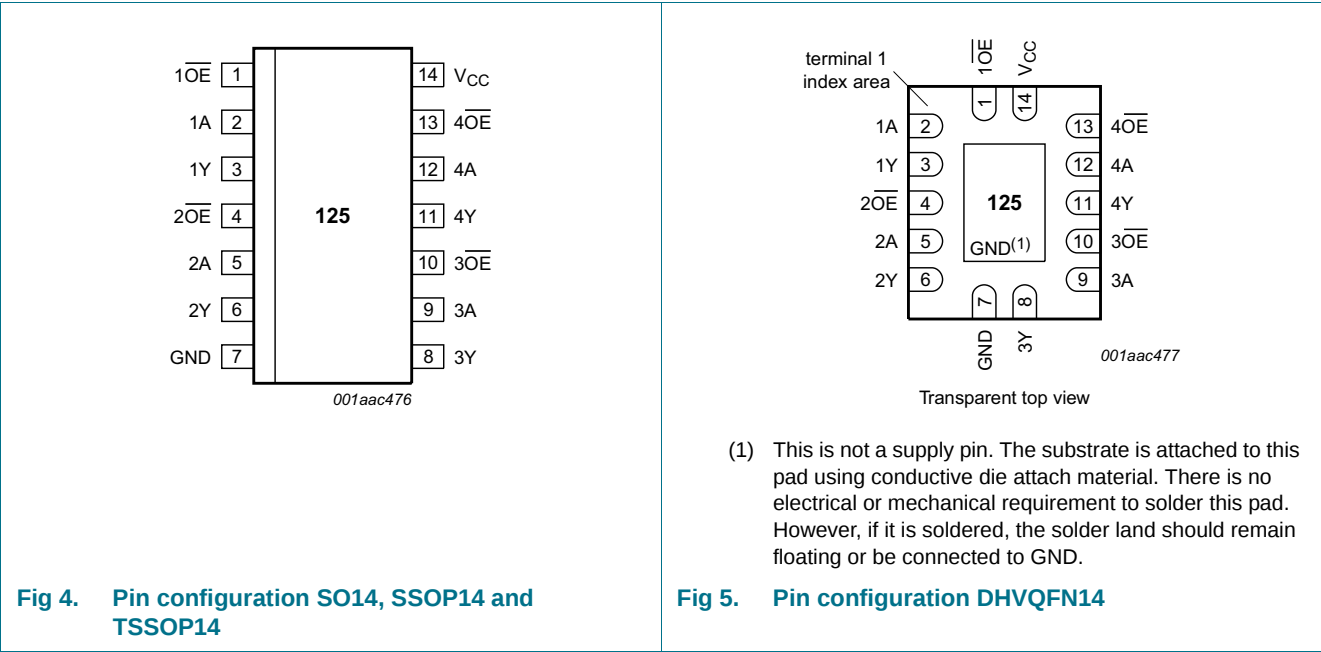
Type number	Package			
	Temperature range	Name	Description	Version
74LVT125D	−40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVTH125D				
74LVT125DB	−40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVTH125DB				
74LVT125PW	−40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVTH125PW				
74LVT125BQ	−40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74LVTH125BQ				

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	1 output enable input (active LOW)
1A	2	1 data input
1Y	3	1 data output
2OE	4	2 output enable input (active LOW)
2A	5	2 data input
2Y	6	2 data output
GND	7	ground (0 V)
3Y	8	3 data output
3A	9	3 data input
3OE	10	3 output enable input (active LOW)
4Y	11	4 data output
4A	12	4 data input
4OE	13	4 output enable input (active LOW)
V _{CC}	14	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+4.6	V
V _I	input voltage		−0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	−0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-	−50	mA
I _{OK}	output clamping current	V _O < 0 V	-	−50	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	−64	mA
T _{stg}	storage temperature		−65	+150	°C
T _j	junction temperature		-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-	-	−32	mA
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
Δt/ΔV	input transition rise and fall rate		0	-	10	ns/V
T _{amb}	ambient temperature	in free air	−40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C^[1]						
V _{IK}	input clamping voltage	I _{IK} = –18 mA; V _{CC} = 2.7 V	-	–0.9	–1.2	V
V _{OH}	HIGH-level output voltage	I _{OH} = –100 µA; V _{CC} = 2.7 V to 3.6 V	V _{CC} – 0.2	V _{CC} – 0.1	-	V
		I _{OH} = –8 mA; V _{CC} = 2.7 V	2.4	2.5	-	V
		I _{OH} = –32 mA; V _{CC} = 3.0 V	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V				
		I _{OL} = 100 µA	-	0.1	0.2	V
		I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V				
		I _{OL} = 16 mA	-	0.25	0.4	V
		I _{OL} = 32 mA	-	0.3	0.5	V
		I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	all input pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	µA
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	µA
		data pins ^[2]				
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	µA
		I _{BHL} bus hold LOW current	V _{CC} = 3 V; V _I = 0.8 V ^[3]	75	150	µA
		I _{BHH} bus hold HIGH current	V _{CC} = 3 V; V _I = 2.0 V	-	–150	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V	-	-	–500	µA
I _{LO}	output leakage current	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	60	125	µA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care ^[4]	-	±1	±100	µA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}				
		output HIGH: V _O = 3.0 V	-	1	5	µA
		output LOW: V _O = 0.5 V	-	–1	–5	µA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND or } V_{CC}$; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	2	7	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3\text{ V to } 3.6\text{ V}$; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA
C_I	input capacitance	$V_I = 0\text{ V or } 3.0\text{ V}$	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V or } 3.0\text{ V}$	-	8	-	pF

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.0\text{ V}$ to 3.6 V a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

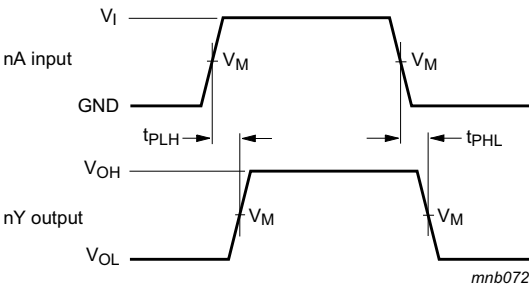
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ [1]						
t_{PLH}	LOW to HIGH propagation delay	nAn to nY; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.7	4.0	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nY; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.9	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.9	3.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{\text{nOE}}$ to nY; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.0	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	3.4	4.7	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{\text{nOE}}$ to nY; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.1	3.4	4.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{\text{nOE}}$ to nY; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	5.7	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.8	3.7	5.1	ns

Table 7. Dynamic characteristics ...continued
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PLZ}	LOW to OFF-state propagation delay	nOE to nY; see Figure 7				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	2.6	4.5	ns

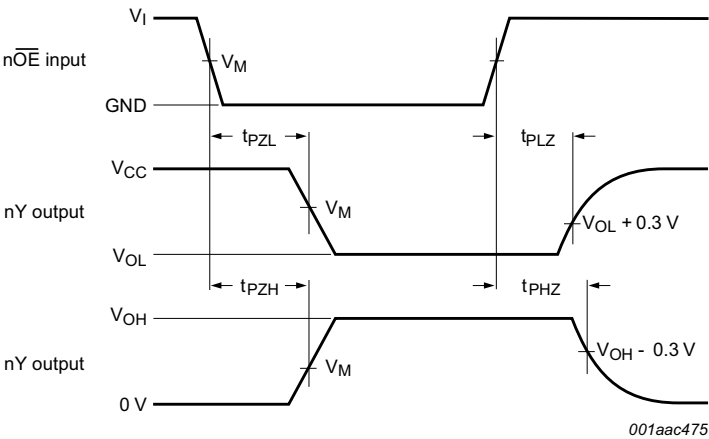
[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Waveforms



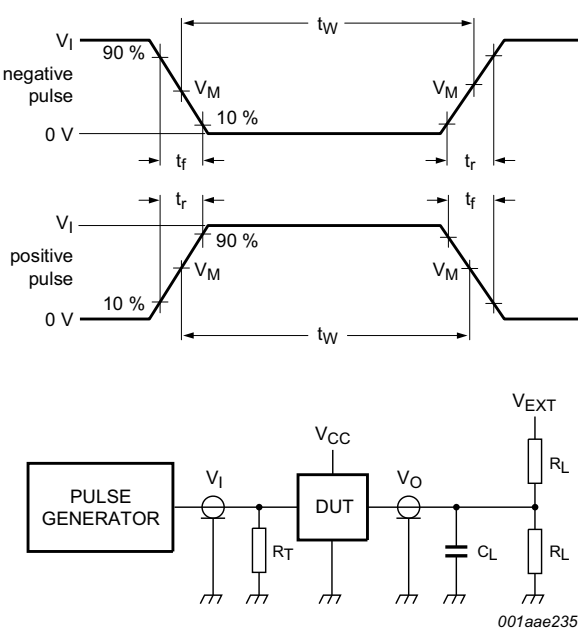
V_M = 1.5 V.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (nA) to output (nY)



V_M = 1.5 V.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Enable and disable times of 3-state outputs



Test data is given in [Table 8](#).
Definitions test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = Test voltage for switching times.

Fig 8. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

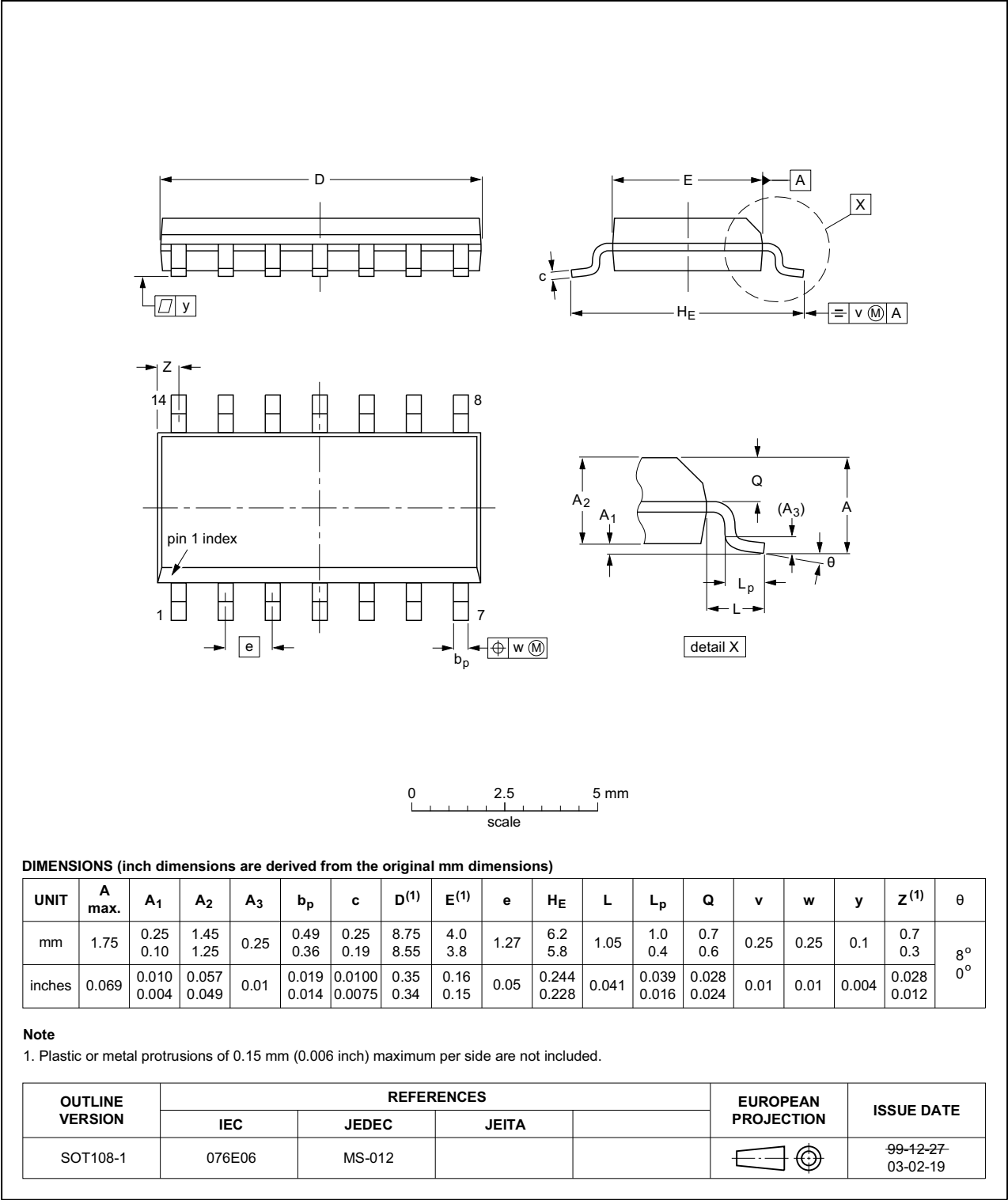


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

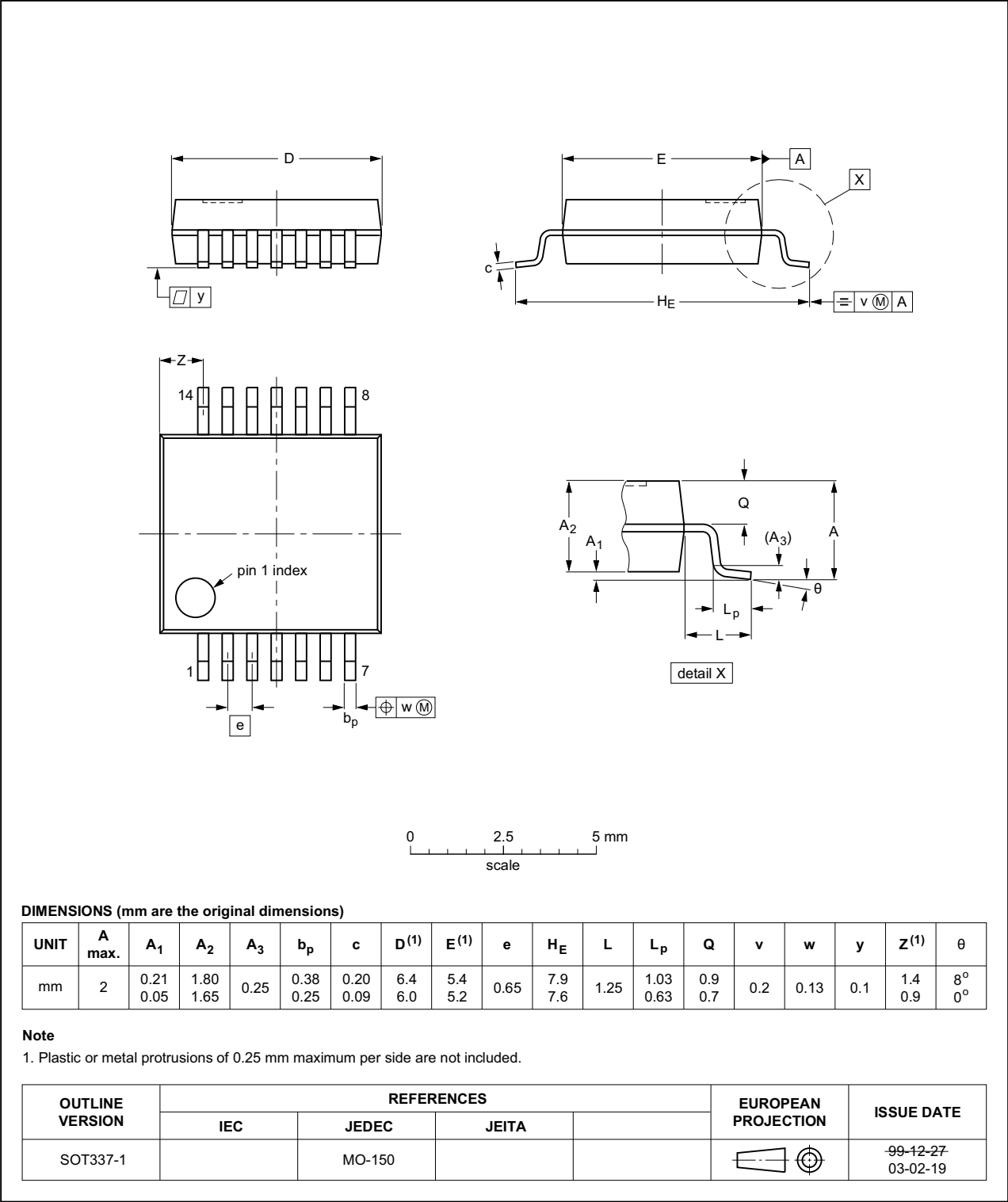


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

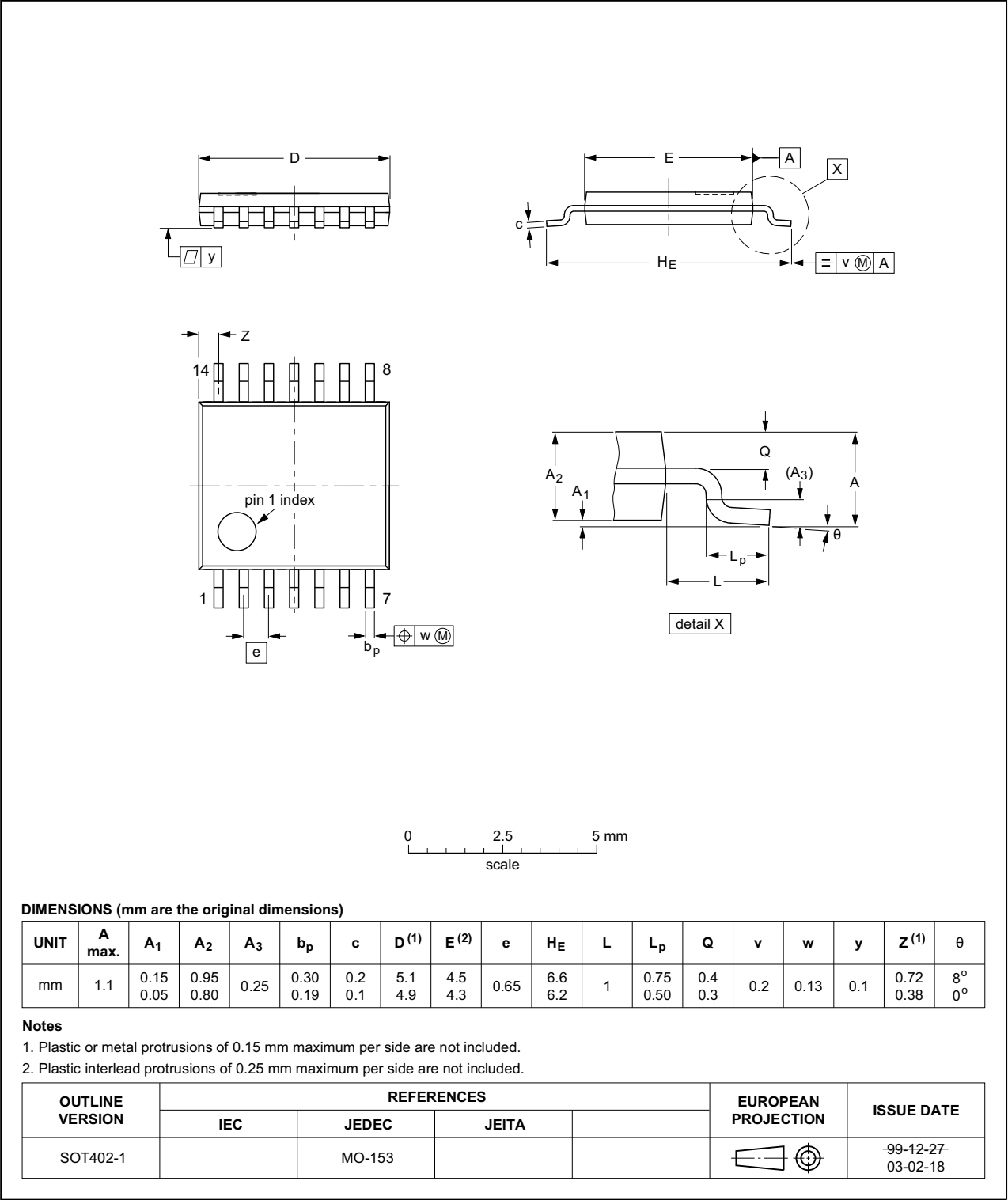


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

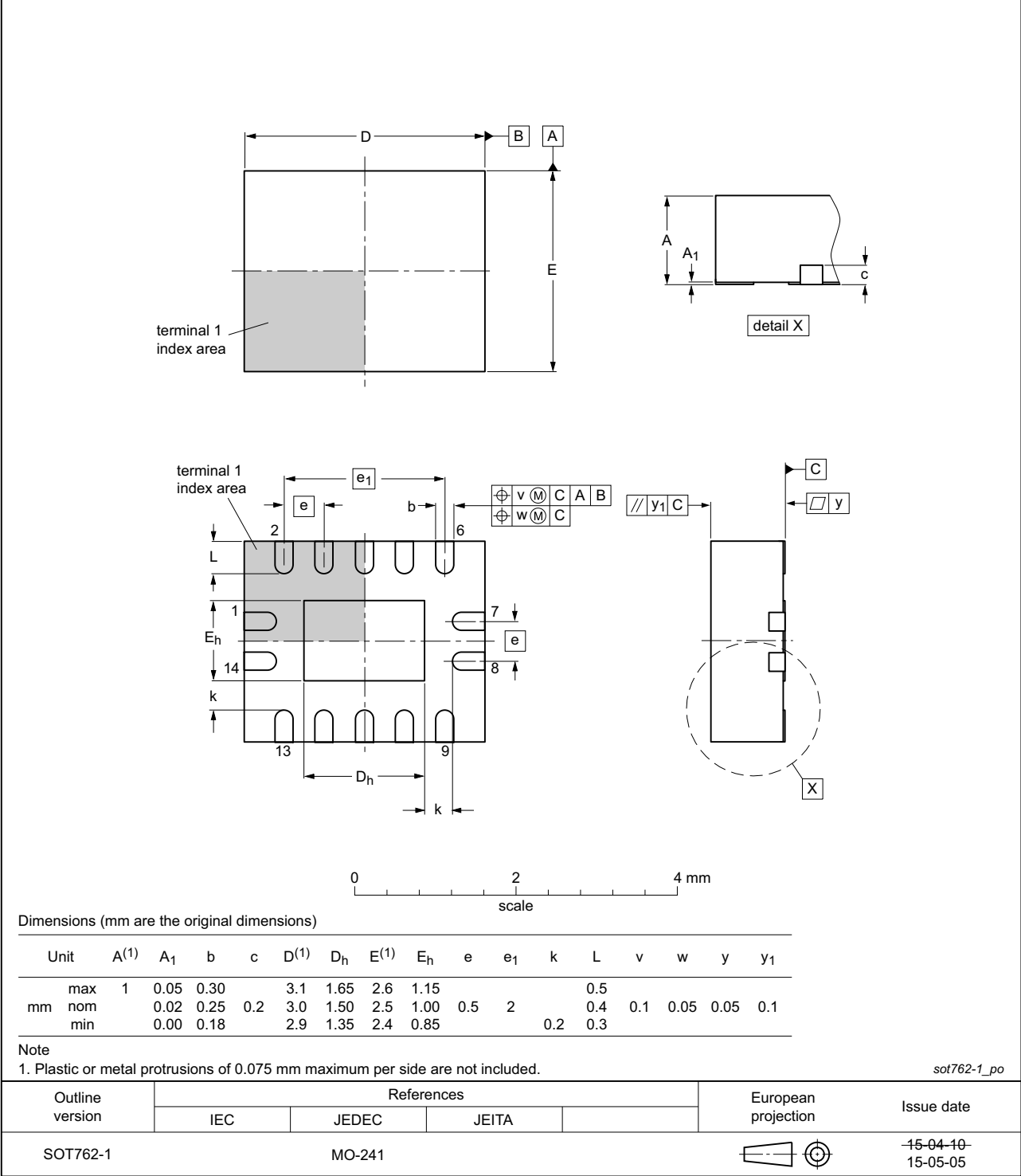


Fig 12. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH125 v.7	20160531	Product data sheet	-	74LVT125 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74LVT_LVTH125 v.6	20060306	Product data sheet	-	74LVT125 v.5
Modifications:	Section 3: Added type numbers 74LVTH125D, 74LVTH125DB, 74LVTH125PW and 74LVTH125BQ.			
74LVT125 v.5	20050210	Product data sheet	-	74LVT125 v.4
74LVT125 v.4	20050207	Product data sheet	-	74LVT125 v.3
74LVT125 v.3	20040624	Product data sheet	-	74LVT125 v.2
74LVT125 v.2	19980219	Product specification	-	74LVT125 v.1
74LVT125 v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
6.1	Function table	4
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	7
12	Package outline	9
13	Abbreviations	13
14	Revision history	13
15	Legal information	14
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	15
16	Contact information	15
17	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 31 May 2016

Document identifier: 74LVT_LVTH125